### IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

**WG 2nd recirculation ballot**

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<td>14</td>
<td>T</td>
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<td>Anslow, Peter Nortel Networks</td>
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<td><strong>Comment Type</strong></td>
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<tr>
<td><strong>The draft is inconsistent on how it defines the frequency break points in equations. For some multi-segment limit lines, there is a small discontinuity at the break point, so it should be clear which limit applies to the exact break frequency.</strong></td>
<td>D</td>
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<tr>
<td>In equations 85-39, 85-40, 85-41, 85-42 change &quot;&lt;10&quot; to &quot;&lt;=10&quot;. In equation 86A-1, 86A-2, 86A-3, 86A-7, 86A-8, 86A-9, 86A-10, 86A-11, 86A-12, 86A-13, 86A-14, 86A-15, 86A-20 for all the frequency segments except the highest segment, change the second inequality from &lt;= to &lt;. E.g. for equation 86A-8 change 0.01 &lt;= f &lt;= 2.5 to 0.01 &lt;= f &lt; 2.5 and change 2.5 &lt;= f &lt;= 5 to 2.5 &lt;= f &lt; 5.</td>
<td><strong>PROPOSED ACCEPT IN PRINCIPLE.</strong></td>
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</table>

| 42         | TR   | D              | PROPOSED ACCEPT IN PRINCIPLE. |
| Anslow, Peter Nortel Networks | | | |
| **Comment Type** | **Comment Status** | **Suggested Remedy** | **Proposed Response** |
| **The test fixture (85-16) and the HCB (86A-4) loss formulas must be IDENTICAL. In D2.2 losses just cross at same value @ 5.165GHz (see page 5 of mazzini_01_0909).** | D | Harmonize the loss. |單位 ACCEPT IN PRINCIPLE. |

| 43         | TR   | D              | PROPOSED ACCEPT IN PRINCIPLE. |
| Mark, Gustlin Cisco | | | |
| **Comment Type** | **Comment Status** | **Suggested Remedy** | **Proposed Response** |
| **The cable assembly test fixture (85-35) and the MCB (86A-5) loss formulas must be IDENTICAL. In D2.2 losses just cross at same value @ 5.165GHz (see page 5 of mazzini_01_0909).** | D | Harmonize the loss. | PROPOSED ACCEPT IN PRINCIPLE. |

| 44         | T    | D              | PROPOSED ACCEPT IN PRINCIPLE. |
| Anslow, Peter Nortel Networks | | | |
| **Comment Type** | **Comment Status** | **Suggested Remedy** | **Proposed Response** |
| **The draft is not consistent in its use of parameter names and figures illustrating limit lines. For example "Return loss" and "Reflection response, SDD22" are used for the same parameter.** | D | Harmonize the loss. | PROPOSED ACCEPT IN PRINCIPLE. |

See response to comment #43
Several illustrations of MDI Connectors have provided greater detail than is necessary for illustration. Readers of the draft are provided with the reference document numbers for normative details regarding the connector.

Drawings include Fig 85-16, 85-17, 85-20, 85-21, 86-6

Suggested Remedy
Simplified illustrative drawings to be provided.

PROPOSED ACCEPT IN PRINCIPLE.
Reference document numbers to normative details have been provided in the associated subclauses. Substitute Figures 85-16, 85-17, 85-20, 85-21 with simpler schematic diagrams that show connector pin positions.

Figure 86-6 is already very simple. However, Figure 86-8 contains more detail than necessary (reference documents for normative specs have been provided in 86.10.3.3), so replace Figure 86-8 with a simpler diagram or delete the figure if a simpler version is not available.

The recommended maximum loss for the PCB only (without connector) (Draft 2.2, page 446, row 51), should be aligned with formula 85A-2 (Transmitter and receiver differential printed circuit board trace loss) that gives maximum PCB loss @5.156GHz = 3.5dB (see page 4 of mazzini_01_0909).

Suggested Remedy
Harmonize the curves as above.

PROPOSED ACCEPT IN PRINCIPLE.
Change equation (85-14)
From:
\[
0.114 + 0.8914 \times \sqrt{f} + 0.846 \times f
\]
\[
- 35.91 + 6.3291 \times f
\]
\[
14.72 \quad \leq f < 8
\]
To:
\[
0.682 \leq f < 0.2
\]
\[
0.114 + 0.8914 \times \sqrt{f} + 0.846 \times f
\]
\[
- 35.91 + 6.3291 \times f
\]
\[
14.72 \quad \leq f < 10
\]

Harmonize the PCB only (without connector) loss between Annex 85A and Annex 86A.

See diminisho_03_0909.pdf for a proposal

Discuss in BRC
In the equations within the draft, the use of “x” to signify multiplication is inconsistent. According to the style manual, a multiplication sign “x” should only be used to indicate multiplication of two numbers (e.g., “1 x 10” or “3 cm x 4 cm”). Some equations do not use “x” e.g. “10log” or “2f” and others use “10 x log” or “2 x f”.

**Suggested Remedy**
Remove all of the “x”s from equations:

Note there is another comment against equation 85A-4
Remove all but the first “x” from equation 85-16
Change equation 85-23 from “*= -0.7 - 0.2x10-9(fx10^6)” to “*= -0.7 - 0.2x10^{-3}f”
Change equation 85-24 from “*= -0.7 + 0.2x10-9(fx10^6)” to “*= -0.7 + 0.2x10^{-3}f”
Remove the first two “x”s from equations 85-31 and 85-32
Remove the “x” between “20” and “log” in equations 85-35, 85A-1 and 85A-2

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.

Also see comment #54 regarding style
Some of the suggested equations may be modified by other comments.

Discuss in BRC

In relation to the presentation of equations in the draft, consult the IEEE style guide 17.3 for instructions on the use of italic and upright text in mathematical expressions.

**Suggested Remedy**
Update equations to be consistent with the format prescribed by the style guide.

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.

The English is strange. "...can have a minimum value ..... due to .....requirements".

**Suggested Remedy**
Option 1 Replace "can" with "may"
Option 2 Replace "clock tolerance and lane alignment requirements" with "clock and lane alignment allowed variations"

Do the same in Annex 4A page 369 line 24

**Proposed Response**
PROPOSED REJECT.

The existing sentence provides better clarity than the suggested remedy.

The use of "can have" is consistent with rest of the notes in 4.4.2 of base document
Comment Type: E  Comment Status: D

**Suggested Remedy**

As above

**Proposed Response**

PROPOSED ACCEPT.

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Cl: 45  SC: 45.2.1.98  P: 66  L: 6  #: 216

Nickoll, Gary  Cisco

**Comment Type:** T  **Comment Status:** D

This section defines a 20 bit BER counter. It was my understanding that we agreed to increase the size of the BER counter to at least 24 bits as defined in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf.

Reading through the proposed implementation in this section I can understand the reluctance to increase the counter to the full 24 bits, as this would require assigning another full 16 bit register. However given this an aggregate BER counter (i.e. one single count for the interface) then adding one extra register would not appear to be a huge overhead.

**Suggested Remedy**

Consider increasing the size of the BER counter to 24 bits as recommeded in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf, or as a minimum use all 16 bits in the higher order register for the BER count, resulting in a 22 bit aggregate counter (lower 6 bits in reg 3.33 and the upper 16 bits in reg 3.44).

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Increase the total counter size to 22 bits.

---

Cl: 45  SC: 45.2.1.88  P: 60  L: 41  #: 8

Marris, Arthur  Cadence

**Comment Type:** T  **Comment Status:** D

**Suggested Remedy**

Hang 'Register_1.174' to 'Register 1.174'

**Proposed Response**

PROPOSED ACCEPT.

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Cl: 45  SC: 45.2.3.16a  P: 74  L: 49  #: 217

Nicholl, Gary  Cisco

**Comment Type:** T  **Comment Status:** D

This section defines a 20 bit BER counter. It was my understanding that we agreed to increase the size of the BER counter to at least 24 bits as defined in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf.

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Consider increasing the size of the BER counter to 24 bits as recommeded in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf, or as a minimum use all 16 bits in the higher order register for the BER count, resulting in a 22 bit aggregate counter (lower 6 bits in reg 3.33 and the upper 16 bits in reg 3.44).

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Increase the total counter size to 22 bits.

---

Cl: 45  SC: 45.2.3.16a  P: 74  L: 49  #: 217

Nicholl, Gary  Cisco

**Comment Type:** T  **Comment Status:** D

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**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Increase the total counter size to 22 bits.

---

Cl: 45  SC: 45.2.3.16a  P: 74  L: 49  #: 217

Nicholl, Gary  Cisco

**Comment Type:** T  **Comment Status:** D

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Reading through the proposed implementation in this section I can understand the reluctance to increase the counter to the full 24 bits, as this would require assigning another full 16 bit register. However given this an aggregate BER counter (i.e. one single count for the interface) then adding one extra register would not appear to be a huge overhead.

**Suggested Remedy**

Consider increasing the size of the BER counter to 24 bits as recommeded in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf, or as a minimum use all 16 bits in the higher order register for the BER count, resulting in a 22 bit aggregate counter (lower 6 bits in reg 3.33 and the upper 16 bits in reg 3.44).

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Increase the total counter size to 22 bits.
Comment Type TR  Comment Status D

I think the following sentence on line 51 is incorrect:

"The 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset."

This means the upper 14 bits in register 3.44 would immediately be cleared when software reads the lower 6 bits in register 3.33. This means that software would likely always read all zeros from register 3.44.

Suggested Remedy

I think the sentence should say:

"The lower 6 bits of the 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset and the upper 14 bits of the 20 counter shall be reset to all zeros when register 3.44 is read or upon PCS reset."

Also is the assumption that while the upper 14 bits of register 3.44 are in a latched state (due to a software read of the lower 6 bits in register 3.33) that errors continue to be accumulated in the background and are not simply ignored? I guess what I am getting at here is if there is any time requirement or constraint between software reading 3.33 and subsequently reading 3.44 to ensure that no errors are missed? For example if after reading 3.33 software has to read 3.44 before 3.33 overflows at a count of 2^6=64 errors, then this would place a constraint that software would have to read 3.44 no later than 21.1us after reading 3.33... this seems fairly tight. Perhaps we need a note to clarify the behavior or expectations a little more clearly?

Proposed Response  Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

[Editor's note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]

Change "3.33" to "3.44" on line 53.

The commenter is invited to re-read the paragraph to understand the correct method to read the 20 bit counter value.
Cl 45 SC 45.2.3.37 P84 L 8 # 210
Nicholl, Gary Cisco

Comment Type TR Comment Status D

Table 45-114a defines an 8 bit BIT counter for each PCS lane.

Slide 6 in http://www.ieee802.org/3/ba/public/jan09/nicholl_01_0109.pdf, recommended that:

"A suitably sized counter shall be allocated in the MDIO memory space for each PCS lane, to ensure that the counter will not saturate (overflow) even if polled at a rate of once per second."

This proposal was accepted by the group as documented in the response to comment #374 in http://www.ieee802.org/3/ba/public/jan09/P8023ba-D11_Final_Resolution_byClause.pdf.

An 8 bit counter is not a 'suitably size' counter. A suitably sized counter would be 14 bits.

Suggested Remedy
Update all PCS lane BIP counters to be at least 14 bits. The simplest approach would be to assign a full 16 bit register to each PCS lane BIP counter.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.

[Editor's note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]

Change all PCS BIP counters to 16 bit.

Cl 74 SC 74.5 P113 L 4 # 143
D'Ambrosia, John Force10 Networks

Comment Type ER Comment Status D

IEEE P802.3az is making changes Clause 74 IEEE Std 802.3-2008. These changes are specific to 10GBASE-R PHYs. IEEE P802.3ba has changed Clause 74 to address 10GBASE-R and 40/100GBASE-R PHYs. Therefore, coordination between the two projects is needed to manage the changes in that project to only the 10GBASE-R PHY section.

Suggested Remedy
Coordinate modifications of Clause 74 with IEEE P802.3az editorial team.

Proposed Response Response Status W
PROPOSED REJECT.

This is a reject because no changes will be made to the 802.3ba draft as a result of this comment.

The P802.3ba editorial team recognizes that the P802.3az project is also proposing changes to Clauses 74, 45 and 69. The relevant 802.3ba editors will co-ordinate with 802.3az editors regarding this issue.

The current expectation is that 802.3ba will be published before 802.3az so it will be 802.3az that will need to take into account the changes made by 802.3ba rather than the other way round.

Cl 74 SC 74.8.4.1 P124 L 40 # 9
Marris, Arthur Cadence

Comment Type T Comment Status D

74.8.4.1 and 74.8.4.2 need to be updated for multi-lane operation

Suggested Remedy
Change to:

FEC_corrected_blocks_counter and FEC_corrected_blocks_counter_i count once for each corrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.87 (1.172, 1.173) and 45.2.1.89 (1.176 to 1.215).

FEC_uncorrected_blocks_counter and FEC_uncorrected_blocks_counter_i count once for each uncorrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.88 (1.174, 1.175) and 45.2.1.90 (1.216 to 1.255).

Proposed Response Response Status W
PROPOSED ACCEPT.
Comment Type: E  Comment Status: D  

The optical interfaces listed in the table give their respective reaches while the electrical interfaces do not.

Suggested Remedy:
For 40GBASE-KR4, add "with reach up to at least 1m"
For 40GBASE-CR4 and 100GBASE-KR4, add "with reach up to at least 7m"

Proposed Response:  
PROPOSED REJECT.

There is only one reach objective for these PMDs. So additional distinction is not necessary.

Comment Type: E  Comment Status: D  

Runon sentence (too many "ands")

Suggested Remedy:
Replace
"The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers and is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."
with
"The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers, is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."

Proposed Response:  
PROPOSED ACCEPT.

Comment Type: T  Comment Status: D  

The definition of Skew Variation is not correct.
Consider a link with relative delays on 4 lanes of 0, 20, 20, 20 UI.

The definition of Skew is:
Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits.

So the skew of the above example is 20 UI.

Now change the delay in the second lane so that the relative delays become: 0, 0, 20, 20 UI. The Skew is still 20 UI

Skew Variation is defined as:
Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation.

So the Skew Variation after the change is 0 UI. However, the delay on the second lane has changed by 20 UI so you need 20 bits in the gearbox buffer.

Suggested Remedy:
Change:
"Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation."
to:
"Skew Variation is defined as the change in skew between any PCS lane and any other PCS lane over the entire time that the link is in operation."

Proposed Response:  
PROPOSED ACCEPT.
Comment Type T  Comment Status D
Column heading state maximum skew but the values have approximate symbol~

Suggested Remedy
Please replace~with max value of skew

Proposed Response  Response Status W
PROPOSED ACCEPT IN PRINCIPLE. [Editor's note: Please do not use special character "tilde" or approximate symbol in comments since this is used as delimiter by the comment tool] Also see related comment #95

Clarify the use of approximate symbol for PCS lane skew in a table footnote.

Comment Type TR  Comment Status D
No test method is defined for measuring dynamic skew

Suggested Remedy
Transmitter lane under test transmits suitably long PRBS pattern with length at least twice as long as the maximum skew variation and based on the scope capability while other lanes transmit PRBS31. Transmitter lane under test output is split in to two. One set of output goes to the golden PLL as defined by the specific PMDS to provide triggering to oscilloscope. The second output goes to the to the oscilloscope inputs which can lock to the PRBS pattern. Skew variation on the first lane is recorded, the measurement is then repeated for the remaining lanes to determine maximum skew variation.

Proposed Response  Response Status W
PROPOSED REJECT.
Also see related comment #104

Clause 80 is not the right place to define measurement methods. Measurement methods are defined in relevant clauses as appropriate.
<table>
<thead>
<tr>
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<th>SuggestedRemedy</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
</thead>
</table>
| E            | The use of the term "scalable" could be misconstrued. There are two distinct interfaces - one that supports 40Gb/s and another that supports 100 Gb/s | Change:  
   a) It is scalable and capable of supporting speeds of 40 Gb/s and 100 Gb/s.  
   b) Data and delimiters are synchronous to a clock reference.  
   c) It provides independent 64-bit-wide transmit and receive data paths.  
   d) It provides for full duplex operation only.  
   to  
   a) The XLGMII interface supports speeds of 40 Gb/s.  
   b) The CGMII interface supports speeds of 100 Gb/s.  
   c) Data and delimiters are synchronous to a clock reference.  
   d) It provides independent 64-bit-wide transmit and receive data paths.  
   e) It provides for full duplex operation only. | W |
| T            | The specification of which sequence ordered set values is reserved is not specified clearly. It appears that lane one or lane two can be anything (>=0x00) but that lane 3 must be >=0x03 for it to be a reserved value. But a value like 0x01 0x00, 0x00 in lanes 1-2-3 are probably also in the group that are considered to be reserved even though it doesn't meet the lane 3 inequality. | Consider showing three rows for reserved: 
   lane 1 >=0x01, lane 2 >=0x00, lane 3=0x00 
   lane 1>=0x00, lane 2 >=0x01, lane 3>=0x00 
   lane 1>=0x00, lane 2 >0x00, lane 3>=0x03 (the existing one) 
   Lane 3 can be 0x01 or 0x02 if lane 1 or lane 2 is >=0x01 and it is still reserved | W |
| T            | Avoid listing of PMDs in the PCS clause that will create a maintainence issue in future. So rephrase sentence as suggested. | The 40GBASE-R PMA(s) can support any of the 40 Gb/s PMD as specified in Table 80-1. Change: 
   "The 40GBASE-R PCS is a sublayer of the following Physical Layers: 40GBASE-SR4, 40GBASE-LR4, 40GBASE-CR4 and 40GBASE-KR4. The 100GBASE-R PCS is a sublayer of the following Physical Layers: 100GBASE-SR10, 100GBASE-LR4, 100GBASE-ER4 and 100GBASE-CR10." To: 
   "The 40GBASE-R PCS is a sublayer of the 40 Gb/s PHYs listed in Table 80-1. The 100GBASE-R PCS is a sublayer of the 100 Gb/s PHYs listed in Table 80-1." | W |

**SuggestedRemedy**

- Change:  
  a) It is scalable and capable of supporting speeds of 40 Gb/s and 100 Gb/s.  
  b) Data and delimiters are synchronous to a clock reference.  
  c) It provides independent 64-bit-wide transmit and receive data paths.  
  d) It provides for full duplex operation only.  
  to  
  a) The XLGMII interface supports speeds of 40 Gb/s.  
  b) The CGMII interface supports speeds of 100 Gb/s.  
  c) Data and delimiters are synchronous to a clock reference.  
  d) It provides independent 64-bit-wide transmit and receive data paths.  
  e) It provides for full duplex operation only.

**Proposed Response**  
PROPOSED ACCEPT IN PRINCIPLE.  
- The XLGMII interface supports speeds of 40 Gb/s.  
- The CGMII interface supports speeds of 100 Gb/s.  
- Data and delimiters are synchronous to a clock reference.  
- It provides independent 64-bit-wide transmit and receive data paths.  
- It provides for full duplex operation only.

**Response Status**  
W  
PROPOSED ACCEPT IN PRINCIPLE.
Comment Type: E  Comment Status: D

Figure 82-2 does not show any indication of the PCS lane BIP error check (although it does show the BER monitor based on sync header errors)

Suggested Remedy
Update Figure 82-2 to show BIP error monitoring.

Proposed Response  Response Status: W
PROPOSED ACCEPT.

Comment Type: T  Comment Status: D

Clariﬁng D2.1 comment 32:  There are two error counting mechanisms that can be used on 64B/66B signals: errored blocks and BIP errors. For isolated errors at error rates of interest, they will give near-identical results. But if burst errors are involved, the errored block counter will typically count 1 per burst while the BIP error counters will typically count the number of errors in the burst.

We should be unambiguous which is meant by BER for the purposes of compliance. As the errored block counter is not very good in service at good BERs, we expect in-service monitoring to use BIP (that’s why it was introduced). It is HIGHLY desirable that the same deﬁnition of BER apply in compliance testing with the scrambled idle signal as in service. Also, as MTTFPA is so important and burst errors are a threat to it, BIP counting is preferable for another reason.

The response to D2.1 comment 32 points out that BIP counting saturates too low for the current hi_ber threshold. So continue with block counting (as is) for the BER monitor state diagram, but…

Suggested Remedy
Say that BER for 64B/66B signals (including the scrambled idle signal) is deﬁned by BIP error counting (rather than by the BER monitor state diagram). Although the count from the BER monitor state diagram may be useful for diagnostics at very bad BER.

Proposed Response  Response Status: W
PROPOSED REJECT.

The proposal is not a complete solution and is proposing a signiﬁcant change to the PCS test pattern operation. Please propose a complete solution to be considered in the future.
Comment Type: TR
Comment Status: D

There is no limit to the potential increment rate of the PRBS31 checker referenced in 49.2.12.
The checker implementation is difficult to match at high increment rates or in the presence of burst errors (the source synchronous descrambler implementation error multiplication factor depends on burst pattern).
There will be less scope for a complex implementation in a PMA device versus a PCS.

For most practical purposes stringent matching of the 49.2.12 implementation is not necessary. It would be sufficient to match the result of a 49.2.12 implementation only for isolated single bit errors and at error rates less than 1 in a thousand.

Proposed Response

Replace:

(see 49.2.12)

With:

The PRBS31 checker shall match the results of the checker implementation in 49.1.12 for isolated single bit errors and at error rates less than 1 in a thousand.

There will be a contribution at the September interim to support this comment.

Suggested Remedy:

Work offline with the commenter to find language that permits appropriate flexibility in implementations without creating gaps that will invite sponsor ballot comments (e.g., why would the clause 49.2.8 PRBS31 generator be used but not the clause 49.2.12 PRBS31 checker?). Attempt to find a method that avoids the error multiplication effect of the clause 49.2.12 checker.

Comment Type: E
Comment Status: D

See the following note under Figure 83-5:

"inst PMD, PMA, or FEC, depending on which sublayer is below this PMA SIL Signal."

The parameter 'inst' appears to be there to address the fact that the sublayer below the PMA can be either a PMD, PMA or FEC.

No such convention appears to be adopted on the same figure for the interface above the PMA. In this case the service interface primitives are 'hard coded' with the name PMA, even though the sublayer above the PMA can be either a PMA, FEC or PCS.

Suggested Remedy:

Suggest adopting a similar naming convention for the service interface primitives for the interface above the PMA (i.e. at the top of the figure), to reflect that the sublayer above the PMA can be either a PMA, FEC or PCS.

Proposed Response

PROPOSED ACCEPT.

The service interface is named according to the sublayer that provides the service. The problem with the sublayer below is that you know that the sublayer provides the generic service interface, but you don't know which sublayer it is (PMD, PMA, or FEC) that is providing it. To describe the PMA service interface, the sublayer providing the service is always the PMA, so you can name the primitives, e.g., PMA:IS_UNITDATA_i.request(tx_bit) without having to know whether it is the PCS, FEC, or another PMA invoking that primitive.
If supported, when send TX PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_TX_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive.

Suggest adding a reference to Figure 83-5 to make it clear in which direction the PRBS signal is being generated.

Suggested Remedy
Change sentence to read:

"If supported, when send TX PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_TX_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive (see Figure 83-5)."

PROPOSED ACCEPT IN PRINCIPLE. [Editor’s note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]

I have some doubts as to how useful it is to reference a figure so far removed from the text, but if that figure is to be referenced, it would be more precise to say:

"If supported, when send TX PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_TX_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive (see Figure 83-5)."

Then you would want to make the same change for all other test pattern generators and checkers:

"If supported, when send RX PRBS9 test pattern mode (see 68.6.1) is enabled by the PRBS9_enable and PRBS_RX_gen_enable control variables, the PMA shall generate a PRBS9 pattern on each of the output lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive (see Figure 83-5)."

"If supported, when check TX PRBS31 test pattern mode is enabled by the PRBS31_enable and PRBS_TX_check_enable control variables, the PMA shall check for the PRBS31 pattern (see 49.2.12) on each of the input lanes received from the service interface below the PMA via the inst:IS_UNITDATA_i.indication primitive (see Figure 83-5)."

"If supported, when send RX PRBS9 test pattern mode (see 68.6.1) is enabled by the PRBS9_enable and PRBS_RX_gen_enable control variables, the PMA shall generate a PRBS9 pattern on each of the output lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive (see Figure 83-5)."

"When enabled, the PMA shall generate a square wave test pattern (8 ones followed by 8 zeros) on the square wave enabled output lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive (see Figure 83-5)."

Again, not sure this is helpful enough to warrant the change, but if implemented, it should be consistent and not for one isolated case.
Following up on D2.1 comment 33. anslow_05_0709 showed that for two scenarios with an almost-minimum 32 UI delay between lanes, the peak baseline wander was about 50% more than for a single PRBS31. I believe that if the delay is substantially increased, that 50% will substantially reduce. Maybe I'll get the simulation done by the meeting. The larger delay could be generated by choosing appropriate seeds for each lane's PRBS generator and starting the generators together, but that's implementation.

**Suggested Remedy**

The first part of the remedy is similar to last time:

Change "on each of the lanes" to "on each of the PCS lanes" here and at line 30. Change "one lane and any other lane" to "one PCS lane and any other PCS lane". In the paragraphs beginning line 38 and line 50, change "lane" or "lanes" to "PCS lane" or "PCS lanes".

Delete "Note that bit multiplexing of per-lane PRBS31 may produce a signal which is not meaningful for downstream sublayers."

Provide 20 PRBS31 error counters in each direction, one per PCS lane. Another solution which would take a few more words would be to generate by 10G lanes and check by 20G PCS lanes, for 100G. Do we have a name for a 10G lane? For 40G, because we have a binary series of lane speeds, generating per lane (whatever that is) and checking per (10G) PCS lane is ideal, but generating by 10G lanes with offset would still work. Increase the 31 bits (UI) minimum delay between generator lanes to a number TBD, around 2000 UI.

**Proposed Response**

PROPOSED REJECT.

D2.1 comment 33 was rejected based on the analysis in anslow_05_0709. The decision should not be reconsidered unless:

1) simulation results can be provided to show that larger offsets do not significantly increase the baseline wander over PRBS31;
2) it can be shown that it is not unduly onerous to be required to generate 20 PRBS31 sequences that are offset by 2000 UI; and
3) a specific offset value can be provided which meets the necessary requirements.

Draft says "There shall be at least 31 bits delay between the PRBS31 patterns generated on one lane and any other lane.". This was to stop the lanes being highly correlated and hence the lane-to-lane crosstalk being unrealistic. However, Skew Variation, not necessarily in the generating PMA, could reduce these relative delays.

**Suggested Remedy**

Increase 31 by the appropriate Skew Variation or say "a delay of 31 UI plus the allowance for Skew Variation for the downstream sublayers as given in Table 80-5. " But see another comment.

**Proposed Response**

PROPOSED REJECT.

As presently defined, the PRBS31 pattern cannot be guaranteed to traverse a gearbox, and hence is applicable only to adjacent layer testing or from the lowest PMA to external test gear. The skew variation budget is based on up to 4 PMAs, FEC, and the link between Tx and Rx. The amount of skew variation between adjacent layers has not been shown to consume a substantial portion of the 31UI, which was an arbitrarily chosen number anyway (big enough to avoid crosstalk issues but small enough not to be onerous to implement).

D2.1 comment 33 was rejected based on the analysis in anslow_05_0709. The decision should not be reconsidered unless:

1) simulation results can be provided to show that larger offsets do not significantly increase the baseline wander over PRBS31;
2) it can be shown that it is not unduly onerous to be required to generate 20 PRBS31 sequences that are offset by 2000 UI; and
3) a specific offset value can be provided which meets the necessary requirements.

**Proposed Response**

PROPOSED REJECT.

Draft says "There shall be at least 31 bits delay between the PRBS31 patterns generated on one lane and any other lane.". This was to stop the lanes being highly correlated and hence the lane-to-lane crosstalk being unrealistic. However, Skew Variation, not necessarily in the generating PMA, could reduce these relative delays.

**Suggested Remedy**

Increase 31 by the appropriate Skew Variation or say "a delay of 31 UI plus the allowance for Skew Variation for the downstream sublayers as given in Table 80-5. " But see another comment.

**Proposed Response**

PROPOSED ACCEPT.
Comment Type: T  
Comment Status: D  

Piling on to D2.1 comment 253. What is in the draft seems so impractical and unnecessarily power-hungry that it won't be obeyed fully. Draft refers to 49.2.12 which says "The test-pattern error counter shall increment once for each bit time that the PRBS31 pattern error signal is high," which could approach the lane line rate. Unlike the assertion in the response to comment 34, choosing an implementation dependent limitation would seem not to be allowed. For comparison, even a lab BERT saturates or drops sync at some point e.g. 10^-3 or 10^-2.

Suggested Remedy:
If you want to stay with the checker of 49.2.12 then write down that a .3ba version need not count error ratios above 1e-3 accurately. This will ease both the high-speed analog silicon and also the management counters.
Also, it might be desirable to define a maximum reported error rate so that the management software doesn't have to be designed to cope with ridiculous BERs. (Per response to D2.1 comment 32, the high BER state machine kicks in at a 10-4 BER, so anything much above that is hopelessly bad and we don't need an exact measurement of it.)
Also, it may ease the implementation to write down that a .3ba version need not count burst errors precisely as 49.2.12 (which isn't accurate for all bursts, anyway).

Proposed Response  
Response Status: W  
PROPOSED ACCEPT IN PRINCIPLE.  
See response to comment 245.

---

Comment Type: ER  
Comment Status: D  

There is some concern regarding the use of the term mapping and how it relates to what is illustrated in Fig 83-6. The use of the word "mapping" seems to address how input lanes are directed to output lanes, but in the commenter's opinion does not do an adequate job addressing the sequencing of bits on the output lanes, which may lead to interpretation issues.

Suggested Remedy:
Further clarifying text is needed. See presentation by dambrosia.
Note - Please discuss in Logic Sub Task Force during Sept Interim.

Proposed Response  
Response Status: W  
PROPOSED ACCEPT IN PRINCIPLE.

Awaiting presentation. There seem to be two possible avenues to address the commenter's concern:
1) to make sure that the term "mapping" is read in a broader sense of meaning how the receipt of a PCSL from a given temporal position (order, sequence) on a given input lane corresponds to which temporal position (order, sequence) that PCSL is placed on a given output lane; or
2) to introduce an additional term "sequencing", and confine the use of the term "mapping" to be the pairing of input lane to output lane for a given PCSL, and use "sequencing" to refer to the order in which PCSLs are bit mixed on input or output lanes.

Awaiting the presentation to make a final decision. Editor's preference is to make it clear that the term "mapping" includes both the input lane to output lane routing of a PCSL and the temporal position or sequence of each PCSL on the input and output lanes.

---

Comment Type: E  
Comment Status: D  

Note on Fig 83-6 is incorrect. Note reads:

"NOTE: i.k indicates bit i on PCSL k. Skew may exist between PCSLs"

The i and k are reversed from what is shown in the figure.

Suggested Remedy:
Change note to read:

NOTE: i.k indicates bit k on PCSL i. Skew may exist between PCSLs

Proposed Response  
Response Status: W  
PROPOSED ACCEPT.
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**Comment Type:** E  
**Comment Status:** D  
**Suggested Remedy:**  
Double full stop ".."  

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**Comment Type:** TR  
**Comment Status:** D  
**Suggested Remedy:**  
A number of equations related to return loss / Sxymn have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers. For Return Loss constraints the requirement should be "greater than or equal to" the equation.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct. Equations include: 83A-5, 83A-7, 83A-8, and 8A-10.

**Proposed Response:**  
PROPOSED ACCEPT.

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**Comment Type:** TR  
**Comment Status:** D  
**Suggested Remedy:**  
A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers. Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct. Equations include: 83A-1 and 83A-2.

**Proposed Response:**  
PROPOSED ACCEPT.

---

**TYPE:** TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general  
**COMMENT STATUS:** D/dispatched  A/accepted  R/rejected  
**RESPONSE STATUS:** O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn  
**SORT ORDER:** Clause, Subclause, page, line  
**Page 15 of 59**  
9/17/2009  3:35:20 PM
All of the figures in this clause follow equations, but there are no statements regarding an equation being illustrated in a figure.

**Suggested Remedy**

Add statement following equation that the equation is illustrated in Fig 83A-x.

**Proposed Response**

PROPOSED ACCEPT.

---

Section 83A.2.1

...less than the insertion loss defined in Equation (83A-1) and illustrated in Figure 83A-3.

83A.2.2

...less than the insertion loss defined in Equation (83A-2) and illustrated in Figure 83A-4.

83A.3.3.3

Differential output return loss requirement is illustrated in Figure 83A-6.

83A.3.3.4

Common mode output return loss is illustrated in Figure 83A-7.

83A.3.4.3

Differential input return loss is illustrated in Figure 83A-10.

83A.3.4.4

Differential-to-common mode input return loss is illustrated in Figure 83A-11.

83A.4

The value for insertion loss is summarized in Equation (83A-9) and illustrated in Figure 83A-13. The value for minimum return loss is summarized in Equation (83A-10) and illustrated in Figure 83A-14.

---

Following up D2.1 comment 159, According to 83.3, a PMA has TX and RX directions, each of which has an input and an output. nAUI is intended to connect PMAs, e.g. one in the host and one in a module. Therefore nAUI must connect a (host) TX (transmitter) output to a (module) transmitter input, and a (module) RX (receiver) output to a (host) receiver input. 83B and 86A use the terms host output, module input, module output, host input, which is compatible with 83. But Figure 83A-2 shows two "Transmitter"s and two "Receiver"s, one for each direction. This isn't compatible terminology.

**Suggested Remedy**

Change "Transmitter" to "output" or "driver" or "driver output" as appropriate, "Transmit Compliance Point" to "output compliance point", "Receiver" to "input", and "Receive Compliance Points" and "Receive Compliance Point" to "output compliance point", throughout 83A.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

In figure:

- Change "Transmitter" to "Driver"
- Change "Transmit Compliance Point" to "Driver Compliance Point"
- Change "Receiver" to "Input"
- Change "Receive Compliance Point" to "Input compliance point"

Change 83A.2.1 title to "Driver Compliance Point" from "Transmitter Compliance Points".

Change first line in 83A.2.1 to:

The differential insertion loss, expressed in decibels, between the Driver and the Driver Compliance Point shall be less than the insertion loss defined in Equation (83A-1).

Change 83A-3 Figure Title to: Insertion loss between Driver Compliance Point and Driver

Change 83A.2.2 title to: Input Compliance Point

Change the first line in 83A.2.2 to:

The differential insertion loss, expressed in decibels, between the Input and the Input Compliance Point shall be less than the insertion loss defined in Equation (83A-2).

Change Figure 83A-4 title to: Insertion loss between Input Compliance Point and Input
I seem to remember that there is a style guide rule that all figures must be referred to by some text. Even if it is not in the style guide rules it is good practice. There are a number of figures in this annex that do not have references. Figure 83A-3 is the first one. This also applies to figure 83A-4, 83A-6, 83A-7, 83A-10, 83A-11, 83A-13, 83A-14

Suggested Remedy
If I am correct then add "and illustrated in figure 83A-3" to the end of line 23, and a similar remedy for the other figures.

PROPOSED ACCEPT IN PRINCIPLE.

See comment 153

SDD21 does not represent loss, it represents forward gain ("through response" or just "response"; 47.4.1 calls it "transmission magnitude response"). For modules, we should stay with S-parameters, as is common industry practice in SFP+, CXP, XAUI (Clause 47) and so on, but the names need cleaning up.

Suggested Remedy
Change "differential insertion loss" to "differential response". Change "less than" to "more than or equal to". Reverse the signs and the inequality in equation 83A-1 and Figure 83A-3.

PROPOSED ACCEPT IN PRINCIPLE.

See comment 151.
IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

Draft 2.2 Comments

Cl 83A SC 83A.3.3.2 P 386 L 42 # 223
Latchman, Ryan Genum Corp

Comment Type T Comment Status D
"Rise/fall time is measured with de-emphasis off" should include a reference to 83A.5.1

SuggestedRemedy
"Rise/fall time is measured with de-emphasis off as defined in 83A.5.1"

Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 83A SC 83A.3.3.3 P 387 L 12 # 19
Anslow, Peter Nortel Networks

Comment Type E Comment Status D
The differential output return loss is required to be met from 10 MHz, but Figure 83A-6 stops at 50 MHz.
Also applies to Figures 83A-7, 83A-10, 83A-11

SuggestedRemedy
Extend Figures 83A-6, 83A-7, 83A-10, 83A-11 to 10 MHz

Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 83A SC 83A.3.3.4 P 387 L 49 # 80
Dawe, Piers Independent

Comment Type TR Comment Status D
As I pointed out in D2.1 comment 35, S-parameters define power gain, not loss. [SCC22] as a ratio must be <1, [SCC22] in dB must be negative. I'm sure our readers can cope with S-parameters and negative numbers.

SuggestedRemedy
Change the signs on the right hand side, change the direction of the inequality back to <= as in D2.1.

Proposed Response Response Status W
PROPOSED REJECT.

Current implementation should be consistent with 85A / cl 72.

Anslow, Peter Nortel Networks

Comment Type E Comment Status D
Several references in Clauses 83A and 83B that should be cross-references are not.

SuggestedRemedy
Make the following references to other places in the draft cross-references.

Page 380, line 32, "Clause 83"
Page 386, line 43, "83.5.10"
Page 388, lines 33 to 38 contain 5 instances (also "83A-1" should be "Table 83A-1")
Page 395, line 11, "Annex 48B.3" should be blue
Page 401, line 19, "Table 83B-1"

Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 83A SC 83A.3.3.5 P 388 L 32 # 201
Pettrilla, John Avago Technologies

Comment Type ER Comment Status D
Requirements for TJ and DJ are found in a subclause titled, "Transmitter eye mask definition". This can make these definitions difficult to find and seems unnecessary as a subclause can easily be added for jitter definition.

SuggestedRemedy
Create a subclause, '83A.3.3.6 Transmitter jitter definition'. Cut the sentence, "The measured jitter at the transmit compliance point shall be less than the maximum Total Jitter as defined in Table 83A-1 and a maximum Deterministic Jitter as defined in 83A-1," from 83A.3.3.5 and paste it into 83A.3.3.6 as the first sentence. From 83A.3.3.5 copy the sentence "Jitter and eye mask measurement requirements are described in 83A.5.1, and are conducted with de-emphasis off," and paste it into 83A.3.3.6 deleting the words, 'and eye mask'. Then in 83A.3.3.5, in the last sentence delete the words, 'Jitter and'. Update the references in tables 83B-3 and 83B-5 to refer to 83A.3.3.6 for TJ and DJ.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.

Modify title to "Transmitter eye mask and transmitter jitter definition"
Comment Type: T  Comment Status: D

Table 83A-2 is actually a mixture of receiver characteristics (eg return losses) and specifications of the most degraded signal the receiver has to tolerate (eg total jitter). The receiver does not have a maximum total jitter tolerance. It's characteristic is a minimum total jitter tolerance.

Suggested Remedy
Split table 83A-2 into two tables. Table A labelled "Receiver input tolerance requirements" with everything in the existing table except the return losses. Table B labelled "Receiver characteristics" with just the return loss lines.

The sentence on page 389 line 26 then becomes. "The receiver shall tolerate signals with the characteristics given in Table A. The receiver shall also have the characteristics given in Table B."

An alternative remedy keeping one table is changing the maximum values of the input signal into minimum input tolerances as done in table 86A-4

Proposed Response: PROPOSED ACCEPT IN PRINCIPLE.

Rename the following:
Maximum Total Jitter to "Minimum Total Input Jitter Tolerance"
Maximum Deterministic Jitter to: "Minimum Deterministic Input Jitter Tolerance"

Modify section 83A.3.4.6 accordingly

Comment Type: T  Comment Status: D

In figure 83A-12 the template for SJ tolerance includes the region below 40 kHz while similar templates in clauses 87 and 86A do not. Clause 87 explicitly omits this region as not specified. These low freq jitter tolerance tests all have the same objective and there seems no reason for a difference in 83A.

Suggested Remedy
Redraw the template in 83A-12 to stop below 40 kHz. For reference, see figure 87-5 or 86A-11.

Proposed Response: PROPOSED ACCEPT.
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### Comment 156

**Comment Type:** E  
**Comment Status:** D  
**Comment:** All of the figures in this clause follow equations, but there are no statements regarding an equation being illustrated in a figure.

**Suggested Remedy:**  
Add statement following equation that the equation is illustrated in Fig 83B-x.

**Proposed Response:**  
**Response Status:** W  
Proposed ACCEPT.

Add the following to 83B.1:

- Equation 83B-1 is illustrated in Figure 83B-1 and Equation 83B-2 is illustrated in Figure 83B-2.

Modify the following sentence in 83B.2:

- The differential insertion loss, expressed in decibels, for the HCB shall be less than the insertion loss defined by Equation (83B-3) and illustrated in Figure 83B-3

Modify the following sentence in 83B.2:

- The differential insertion loss, expressed in decibels, for the MCB shall be less than the insertion loss defined by Equation (83B-4) and illustrated in Figure 83B-6

### Comment 154

**Comment Type:** TR  
**Comment Status:** D  
**Comment:** A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

**Equations include:** 83B-1, 83B-2, 83B-3, and 83B-4.

**Suggested Remedy:**  
- Change 83B-1 and 83B-2 to
  - \[|SDD21| \leq 0.111 + (1.046 \times f^{(1/2)}) + (1.05 \times f)\]  
    \[0.25 \leq f \leq 7\]
  - \[|SDD21| \leq -11.95 + (3.15 \times f)\]  
    \[7 \leq f \leq 11.1\]
- Change 83B-3 to
  - \[|SDD21| \leq 0.04 + (0.33 \times f^{(1/2)}) + (0.32 \times f)\]  
    \[0.25 \leq f \leq 7\]
  - \[|SDD21| \leq -3.72 + f\]  
    \[7 \leq f \leq 11.1\]
- Change 83B-4 to
  - \[|SDD21| \leq -0.00086 + (0.2286 \times f^{(1/2)}) + (0.08386 \times f)\]

**Proposed Response:**  
**Response Status:** W  
Proposed ACCEPT.

See suggested remedy.
A number of equations related to return loss / $S_{xym}$ have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers.

The equations all result in negative numbers.

For Return Loss constraints the requirement should be "greater than or equal to" the equation.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83B-5, 83B-6, 83B-8, and 83B-9.

**SuggestedRemedy**

Change Eqs 83B-5, 83B-9 to

$$|S_{DD11}| \geq 12 - (2 \cdot f) \quad \text{for} \quad 0.01 \leq f \leq 2.19$$

$$5.56 - (8.76 \cdot \log_{10} (f/5.5)) \quad \text{for} \quad 2.19 \leq f \leq 11.1$$

Change Eqs 83B-6, 83B-8 to

$$|S_{DD22}| \geq 12 - (2 \cdot f) \quad \text{for} \quad 0.01 \leq f \leq 2.19$$

$$5.56 - (8.76 \cdot \log_{10} (f/5.5)) \quad \text{for} \quad 2.19 \leq f \leq 11.1$$

For noted equations change sign from "less than or equal to" to "greater than or equal to".

**Proposed Response**

PROPOSED ACCEPT.

---

Equation for module loss not correctly scaled

**SuggestedRemedy**

```
|SDD22| = 3.2 - 0.84f
```

**Proposed Response**

PROPOSED ACCEPT.

---

Repeating comment 159 of D2.1, Figure 83A-1 is similar to Figure 83B-3 but the names on what may be identical items are different, e.g. XLAUI/CAUI Component vs XLAUI/CAUI IC, Driver vs Transmitter, Input vs Receiver. It's not good practice where block diagrams showing the same level of detail use different names for the same item. If these block diagram elements are actually the same, please use the same terminology, otherwise this is inconsistent and can be confusing. See also Figs 83B-5 & 7.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

See comment 82.

---

The loss of the host compliance board is allowed to vary from zero to 2.1dB at Nyquist. This will significantly change the results of measurements.

**SuggestedRemedy**

Either

1. Change the sentence on line 19 to "The differential insertion loss, CPIL, expressed in decibels, for the reference HCB shall be CPIL, as defined by Equation (83B-3). Differences between this reference loss and the loss of an actual HCB shall be accounted for in the measurements.

2. Change line 19 to "The differential insertion loss, CPIL, expressed in decibels, for the reference HCB shall be CPIL, as defined by Equation (83B-3). Changes between this reference loss and the loss of an actual HCB shall be accounted for in the measurements.

**Proposed Response**

PROPOSED REJECT.

An upper limit of 2.1dB will be challenging to meet. 0 - 2.1dB is not likely to be the range of implementation.
The equation (83B-3) has an inequality sign for the |SDD21| Host Compliance Board insertion loss.

Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

Suggested Remedy
Replace the inequality sign with an equal sign ".=".

Proposed Response  Response Status  W
PROPOSED REJECT.

Flexibility around implementation of the board is likely desirable, therefore use inequality sign

The equation (83B-4) has an inequality sign for the |SDD21| Module Compliance Board insertion loss.

Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

Suggested Remedy
Replace the inequality sign with an equal sign ".=".

Proposed Response  Response Status  W
PROPOSED REJECT.

Flexibility around implementation of the board is likely desirable, therefore use inequality sign

In Table 83B-2, compliance point terms TP1, TP1a and TP4 are used without definition or reference. If these are the same points as in clause 86 or 86A, then 86 should be cited. (Clause 85 also defines a TP1 and TP4 but no TP1a) If not, there should be a figure defining these points.

Suggested Remedy
If TP1, TP1a and TP4 are the same as in clause 86, add a note to table 83B-2 citing clause 86, figure 86-3, for the definition of these points.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.

Following statement is currently present in 83B.2.1:
"Table 83B-2 also lists the equivalent test points for the XLPP/CPP (see Figure 86-3)."

Proposed Response  Response Status  W
PROPOSED ACCEPT.

In Table 83B-2 two references to equations should say "Equation 83B-x"

Proposed Response  Response Status  W
PROPOSED ACCEPT.

Table 83B-3 footnote a is redundant with the entry in the subclause column and can be deleted. This also occurs in Table 83B-5

Proposed Response  Response Status  W
PROPOSED ACCEPT.
Cl 83B SC 83B.2.1 P 407 L 27 # 185
Dudek, Mike QLogic

Comment Type: T
Comment Status: D

Vth-demph is used in equation 83B-7 however Vtx-demph is used in table 83B-3.

Suggested Remedy
Change Vth-demph to Vtx-demph in equation 83B-7.

Proposed Response: Response Status: W
PROPOSED ACCEPT.

Cl 83B SC 83B.2.3 P 409 L 42 # 130
Ghiasi, Ali Broadcom

Comment Type: TR
Comment Status: D

FR4 trace stress not clear what it is.

Suggested Remedy
Suggest either use Frequency Dependent Attenuator or PCB Trace.

Proposed Response: Response Status: W
PROPOSED ACCEPT.

Change:
FR4 trace stress is then added until 0.25 UI peak-to-peak deterministic jitter is achieved.

To:
FR4 trace stress is then added using PCB trace or Frequency Dependent Attenuation which emulates PCB loss. FR4 trace stress is added until 0.25 UI peak-to-peak deterministic jitter is achieved.

Cl 85 SC 85.10 P 260 L 10 # 164
Dudek, Mike QLogic

Comment Type: TR
Comment Status: D

The parameters in Table 85-8 do not adequately specify the cable as there are no insertion loss or insertion loss deviation specifications at frequencies other than 5.15625GHz. Resonances can occur that meet the specification at this one frequency but cause problems at other frequencies. Also the return loss specification is too relaxed.

Suggested Remedy
Change the parameter for the first row of table 85-8 to "Maximum fitted insertion loss at 5.15625 GHz"). For insertion loss deviation delete "at 5.15625GHZ and change the value to "see 85.10.3. Delete at 5.15625 GHz from the return loss specification and change the specification to "see equation 85-1", or "see 85.10.4"

Proposed Response: Response Status: W
PROPOSED REJECT. Change:
"FR4 trace stress is then added until 0.25 UI peak-to-peak deterministic jitter is achieved" to:
"FR4 trace stress is then added using PCB trace or Frequency Dependent Attenuation which emulates PCB loss. FR4 trace stress is added until 0.25 UI peak-to-peak deterministic jitter is achieved"

Cl 85 SC 85.10 P 260 L 14 # 80
Moore, Charles Avago Technologies

Comment Type: T
Comment Status: D

In Table 85-8 Minima for MDNEXT loss, MDFEXT loss and power sum crosstalk loss are listed but the references do not specify either values or equations for minima. This is because these specs have been replaced by Minimum integrated crosstalk noise. These minima are no longer needed.

Suggested Remedy
Delete unused specs from table 85-8.

Proposed Response: Response Status: W
PROPOSED ACCEPT IN PRINCIPLE. [Editor's Note: Commenter did not indicate comment type, assigned Comment Type: T, since the commenter is not part of the P802.3ba ballot group]
Response: 85.10.8 Cable assembly integrated crosstalk noise (ICN) uses MDNEXT and MDFEXT. Delete minimum Table 85-8 from "minimum MDNEXT" and "minimum FEXT".

Cl 85 SC 85.10 P 260 L 4 # 86
Moore, Charles Avago Technologies

Comment Type: T
Comment Status: D

The rest of the document uses linear frequency for plots of Insertion loss, Return Loss ect. this section does not. It has the tendency to give too much visual weight to the low frequencies.

Suggested Remedy
All plots of this nature changed to linear frequency.

Proposed Response: Response Status: W
PROPOSED REJECT. [Editor's note: Late comment for consideration by the Task Force]
Sub-clause reference not provided.
<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
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<tbody>
<tr>
<td>TR</td>
<td>D</td>
<td>The connector loss (calculated as 85-37 values minus 85-35 and 85-16) of the test fixture improves when frequency increase (see slide 5). Above formulas should be corrected to avoid this.</td>
<td>W</td>
</tr>
<tr>
<td>TR</td>
<td>D</td>
<td>As above.</td>
<td>W</td>
</tr>
<tr>
<td>TR</td>
<td>D</td>
<td>Replace: 85.8.3.7 Test fixture insertion loss equation [85-16]. With: 86A.5.1.1.1 Reference through responses (SDD21) of HCB and MCB For the HCB, equation (86A-4) using frequency range of 0.050 Ghz to 6 Ghz. (2)Replace: 85.10.9 Cable assembly test fixture equation [85-35]. With: 86A.5.1.1.1 Reference through responses (SDD21) of HCB and MCB For the MCB, equation (86A-5) using frequency range of 0.050 Ghz to 6 Ghz.</td>
<td>W</td>
</tr>
<tr>
<td>T</td>
<td>D</td>
<td>Rather than using minimum insertion loss [equation 85-36] and a maximum insertion loss [equation 85-37] to specify the mated test fixtures insertion loss in 85.10.10.1, I suggest we use a fit to the mated test fixtures and an ILD to address the IL deviations from the fit. This is consistent with 85.8.4.3.1 Test channel insertion loss and 85.10.2 Cable assembly insertion loss 85.10.10.1.</td>
<td>W</td>
</tr>
<tr>
<td>T</td>
<td>D</td>
<td>Replace minimum insertion loss [equation 85-36] and a maximum insertion loss [equation 85-37] with a specification for a fitted cable assembly insertion loss and insertion loss deviation for the mated test fixtures insertion loss in 85.10.10.1. Presentation material will be provided in support of suggested remedy.</td>
<td>W</td>
</tr>
<tr>
<td>T</td>
<td>D</td>
<td>PROPOSED ACCEPT IN PRINCIPLE. See suggested responses to comment#167, comment#177 and comment#170.</td>
<td>W</td>
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<tr>
<td>TR</td>
<td>D</td>
<td>Please copy section 86A.5.1.1 in to CL85</td>
<td>W</td>
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<tr>
<td>TR</td>
<td>D</td>
<td>PROPOSED ACCEPT IN PRINCIPLE. The 85.10.10 Mated test fixtures insertion loss as well as the test fixtures (85.8.3.7-[TP-TF]) and (85.10.9-[CA-TF]) insertion losses are specified. See response to comment#43.</td>
<td>W</td>
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<tr>
<td>T</td>
<td>D</td>
<td>Please use linear freq scale similar to fig 86A-3</td>
<td>W</td>
</tr>
<tr>
<td>TR</td>
<td>D</td>
<td>PROPOSED ACCEPT IN PRINCIPLE. For Figure 85-12 use linear scale for equation [85-36] and equation [85-37] for consistency with linear freq scale of Figure 86A-3.</td>
<td>W</td>
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<tr>
<td>T</td>
<td>D</td>
<td>Nominal mated test fixture loss not defined</td>
<td>W</td>
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<tr>
<td>T</td>
<td>D</td>
<td>Add nominal test fixture loss at Nyquist is 2.4 dB. Test fixtures with loss lower than nominal shall account for test fixture loss difference from nominal in the equation 85-19.</td>
<td>W</td>
</tr>
</tbody>
</table>
"NEXT loss" sounds wrong. We never expected all the power incident on the pair of test fixtures to appear as crosstalk, so how is it "lost"? It seems to be "lost" several times over, to NEXT, to FEXT, to regular transmission loss, and to reflection. This doesn't make sense. A better term than regular loss, which is used frequently in 802.3, is attenuation, because it focuses on the signal that's there rather than the signal that's "lost". Of course, it would be much better to specify NEXT (-ve dB) rather than "NEXT loss" or "NEXT attenuation" (you need to the right-way-up NEXT to calculate MDNEXT anyway).

Suggested Remedy
This is a defensive comment. Whatever you do, don't mess up 86A. It will take a lot of comments in probably more than one meeting cycle to repair the collateral damage.

Proposed Response
PROPOSED REJECT.
NEXT loss consistent with the use of "loss" for naming other signal impairments e.g., return loss, insertion loss, channel loss...etc...used in clause 85 and other IEEE 802.3 clauses.

Apparemly, variable names in equations are not allowed to contain spaces. I suppose this is because to a mathematician "NEXT loss" means "NEXT" multiplied by "loss".

Suggested Remedy
My preferred solution is change "NEXT loss" to "NEXT" and flip the sign.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Follow style guide; if space is to be removed then>

Changes: NEXT loss
To: NEXT with subscripted loss

Dated test fixture crosstalk loss in current draft are place holder and some of the limit specially PSFXT will impact the measurements accuracy

Suggested Remedy
For the new limits please see ghiasi_01_0909

Proposed Response
PROPOSED REJECT.
The commenter has not provided a sufficiently complete proposal in this comment that would enable the implementation of suggested remedy.
For sub-task force review ghiasi_01_0909.

Draft says "MDNEXT loss is specified as the power sum of the individual NEXT losses."
This is not correct. MDNEXT is the power sum of the individual NEXTs, but "MDNEXT loss" is the inverse of the power sum of the individual inverses of "NEXT losses".

Suggested Remedy
My preferred solution is change "NEXT loss" to "NEXT" and "MDNEXT loss" to "MDNEXT", and flip the signs.

Proposed Response
PROPOSED REJECT.
For MDNEXT and NEXT, "loss" is used to distinguish from "gain".
Comment Type: TR
Comment Status: D

Cable assembly insertion loss is not consistent with 24.4 dB total loss budget.
Suggested Remedy:
Change 17.04 to 11.

Response Status: W

PROPOSED REJECT.

The maximum channel insertion loss is determined using Equation (85A-3). The maximum channel insertion loss is 24.44 dB at 5.15625 GHz (dB) (85A-3) for 50 MHz = f = 6000 MHz.

ILCh(f) = ILChmax(f) = ILCamax(f) + (2 × ILHost(f)) - (2 × ILMatedTF(f)) (85-A3)

where:
- f is the frequency in MHz.
- ILCamax(f) (17.04 dB) >> The maximum cable assembly insertion loss using Equation (85-19) and Table 85-9 coefficients.
- ILHost(f) (6.5 dB) >> The maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (85-14).
- ILMatedTF(f) (2.8 dB) >> The maximum insertion loss of the mated test fixture using Equation (85-37).

ILCh(f) = ILChmax(f) = 17.04 + (2 × 6.5) - (2 × 2.8) = 24.44 dB.

Comment Type: T
Comment Status: D

The units are wrong.
Suggested Remedy:
Change the sentence from "The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and the maximum allowed values of a1, a2, and a4 is illustrated in Figure 85-6." to "The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and one example of the maximum allowed values of a1, a2, and a4 is illustrated in Figure 85-6." Change the title of figure 85-6 to "Example maximum cable assembly insertion loss".
Delete the duplicate sentence on page 262 line 5.

Response Status: W

PROPOSED ACCEPT.
See suggested remedy.

Comment Type: E
Comment Status: D

Figure 85-6, 85-7 and others, plot vs log frequency quantitys which can be seen more clearly if plotted versus linear frequency.
Suggested Remedy:
Convert all frequency plots to linear frequency.

Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.
Use log scale for cable assembly graphs for consistent treatment of twinaxial cable assemblies across clauses (clause 54) as well as alignment with backplane.

For test fixtures, figures should be consistent across 802.3ba clauses.
<table>
<thead>
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<tr>
<td><strong>The Cable assembly insertion loss deviation is required to be met from 50 MHz to 7.5 GHz. However, in Figure 85-7 the limits are illustrated from 50 MHz to 6 GHz only. Also applies to Figure 85-14 where the lines cannot be seen from 8 to 10 GHz Also Figure 85A-1 is plotted to 6 GHz but only applies to 5.15625 GHz</strong></td>
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<td>Make the lines visible in Figure 85-14 up to 10 GHz</td>
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<td>Stop the line in Figure 85A-1 at 5.15625 GHz</td>
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<td><strong>MDNEXTloss is defined to be computed over that range of 50 to 6000 MHz, but the calculation that uses this quantity, integrated crosstalk noise (85.10.8), requires values from 50 to 10000 MHz.</strong></td>
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<td>Correct the frequency range to be consistent with 85.10.8. Also correct the frequency range in 85.10.6 (MDNEXTloss).</td>
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<td><strong>Unnecessary left parenthesis at end of sub-clause heading</strong></td>
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<tr>
<td><strong>There are no requirements on PSXT(f) and it is not used as a parameter in any of the cable assembly specifications.</strong></td>
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<tr>
<td><strong>Equations (85-29) and (85-30) are in error. The expression &quot;sinc^2 x (f/fn)&quot; should be &quot;(sinc(f/fn))^2&quot; in both cases.</strong></td>
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<tr>
<td>Remove the superfluous &quot;x&quot; in both equations.</td>
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</table>
### Comment: Cl 85 SC 85.10.8 P 266 L 41 # 24

**Comment Type:** E  
**Comment Status:** D  
**Proposed Response:** PROPOSED ACCEPT.

This says:  
"where IL) IL denotes the value..."

**Suggested Remedy:**  
change "IL) IL denotes the value..." to * IL is the value...

**Anslow, Peter** Nortel Networks

### Comment: Cl 85 SC 85.10.8 P 267 L 1 # 147

**Comment Type:** E  
**Comment Status:** D  
**Proposed Response:** PROPOSED ACCEPT.

Other figures in the draft have shown where the pass region is in relation to a stated curve.

**Suggested Remedy:**  
add text "Pass Region" to region below the curve.

**D'Ambrosia, John** Force10 Networks

### Comment: Cl 85 SC 85.10.9 P 267 L 29 # 167

**Comment Type:** TR  
**Comment Status:** D  
**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.

Results will vary depending on the fixture insertion loss. We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86A. It would also be good to specify exactly what is included in the Test fixture loss. Also the test fixture loss is not matching what was used to derive the link budget (The link budget was derived in Healey_03a_0709 has the same PCB test fixture loss as clause 86A).

**Suggested Remedy:**

Change "The maximum test fixture insertion loss shall meet the values determined using Equation (85-35). The values for the coefficients b1 , b2, b3 b4 and e are given in Equation (85-16)" to "The reference test fixture insertion loss shall meet the values determined using Equation (85-35).

The reference test fixture insertion loss shall meet the values determined using Equation (85-35). The reference test fixture insertion loss shall meet the values determined using Equation (85-35).

Also state whether the connector loss is included in the test fixture loss or not.

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.

"The total integrated crosstalk RMS noise voltage shall be less than the value specified by Equation (85-34) illustrated in Figure 85-9."

**Dudek, Mike** QLogic

---

**Type:** TR/technical required  
**ER/editorial required**  
**GR/general required**  
**T/technical**  
**E/editorial**  
**G/general**  
**Comment Status:** D/dispatched  
**A/accepted**  
**R/rejected**  
**Response Status:** O/open  
**W/written**  
**C/closed**  
**U/unsatisfied**  
**Z/withdrawn**

**Sort Order:** Clause, Subclause, page, line
The cable assembly test fixture is not consistent with Eq 86A-5. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

Suggested Remedy
Please use Eq 86A-5

PROPOSED ACCEPT IN PRINCIPLE.
See response comment #43.

Hardware contact definitions in Table 85-12 violate the QSFP connector specification of SFF-8436: the table requires that contact 27 be open in the case of a copper module, while the QSFP spec defines this contact as module presence pin and requires it to be grounded in the module. As a result of this discrepancy, passive QSFP copper cables created for all other standards using SFF-8436 will not be interoperable with 40GE. Conversely, if the connector is pinned out per table 85.11, the cable will not as a general rule be able to be used in Infiniband and other equipment already deployed in the field. While not strictly a problem from IEEE point of view, I believe this incompatibility will have negative impact on the broad market potential and future adoption of this standard. In addition, electronic keying is also required for CR10 and is currently missing, and defining it along the lines of table 85-12 causes even more severe discrepancy with the CXP specification (see my next comment).

Suggested Remedy
The entire section 85.11.1.1.1 as currently written needs to be deleted. There does not appear to be a way to define electronic keying without violating the QSFP spec. The reasonable solution is to use the SFF-8436 management interface, which has provisions for identifying the module as a copper or an optical module. Also, it is obvious that everyone will end up using the management interface anyway, because it is de facto industry standard and it does the job. If management interface definition is beyond the scope of the project, then we could either make an informative statement referencing the SFF-8436 management interface; or we could make a statement along the lines of "Electronic keying shall be used in order to enable detection of Style-1 plug connector versus fiber module or no module present. The details of implementation of such keying are beyond the scope of this standard". This would prompt people to use the management interface without calling it out, or it would enable proprietary/custom designs along the lines of table 85-12.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
The basis for Table 85-12 requires a distinction between a module and a direct attach plug. If this distinction is clear in SFF-8436, as I had assumed when creating the table, Table 85-12 is not in conflict with SFF-8436. Given the number of similar comments the distinction is not clear or not made.

Delete: sub-clause 85.11.1.1.1
Add: 85.11.4 Electronic keying

Electronic keying can be used to enable the detection of Style-1 40GBASE-CR4 MDI connectors or 100GBASE-CR10 MDI cable assembly plugs versus fiber modules or no modules present. Specification of electronic keying is beyond the scope of this standard.
Electronic keying needs to be defined for CR10 as well, in order to enable distinction of copper from fiber modules by the host. However, there does not appear to be a way to do this via hardware keys without violating the CXP spec, particularly as it is defined in the InfiniBand Architecture Specification. The only way to do this along the lines of Table 85-12 would be to have contact C20 open, and contact C21 pulled low. But C20 is the module presence pin that is required to be grounded in all cases by the CXP spec, and C21 is a shared interrupt/reset pin, so pulling it low will disrupt the operation of InfiniBand equipment. As a result, passive cables designed for InfiniBand will not interoperate with CR10.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
See response comment #2.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
See response comment #2.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
See response comment #2.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
[Editor's Note: Commenter submitted a TR comment. Changed to comment type: T since the commenter is not in P802.3ba ballot group]
See response comment #2.
Due to overvoltage concern see comment 208 D2.1, the default peak to peak must not exceed 700 mV.

**Suggested Remedy**
Add note to 1200 mV that default output must not be greater than 700 mV to prevent overvoltage damage to XLPPI or CPPI PMD.

**Proposed Response**
PROPOSED REJECT.

Some of the contacts shown in the MDI diagram are not listed in table 85-11.

**Suggested Remedy**
Please include all contacts.

**Proposed Response**
PROPOSED REJECT. See NOTE—Although the 100GBASE-CR10 MDI supports 84 connections only the transmitter and receiver contact assignments are specified.

**Proposed Response**
PROPOSED ACCEPT.

Spelling compatibility.

**Suggested Remedy**
Change compatibility to compatibility.

**Proposed Response**
PROPOSED ACCEPT.
IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

Marris, Arthur, Cadence

Comment Type: E
Comment Status: D

unnecessary hyphen

Suggested Remedy:
Change 'The-' to 'The'

Proposed Response:

PROPOSED ACCEPT.
See suggested remedy

Anslow, Peter, Nortel Networks

Comment Type: E
Comment Status: D

Several references in Clause 85 that should be cross-references are not.

Suggested Remedy:

Make the following references to other places in the draft cross-references.

Page 240, line 44, "80.3.3"
Page 244, line 20, "85.10"
Page 246, line 39, "85.7.4"
Page 247, line 45, "45.2.1.7.4" (not blue)
Page 247, line 53, "45.2.1.7.5" (not blue)
Page 251, line 27, "85.7.12"
Page 252, line 3, "83.5.10"
Page 253, line 28, "85.10"

Proposed Response:

PROPOSED ACCEPT.
See suggested remedy

DiMinico, Christopher, MC Communications

Comment Type: E
Comment Status: D

spelling interepet

Suggested Remedy:

Change interepet to interpret

Proposed Response:

PROPOSED ACCEPT.
See suggested remedy

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Clause, Subclause, page, line

Page 32 of 59
This paragraph (85.7.1) says that TP2 is at the output end of the mated connector and defines this as TP2. Table 85-4 says that the specifications are at TP2, but 85.8.3.5 says that the measurements are at the output of the test fixture.

**Suggested Remedy**

Change "The electrical transmit signal is defined at the output end of the mated connector TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2." to "The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2.".

In Figure 85-5 Show the connector and PCB traces to the left of TP2 or TP3.

To clarify things make the Test fixture impedance 85.8.3.6 and Test fixture insertion loss 85.8.3.7 sub-sections of 85.8.3.5.

**Proposed Response**

**Response Status W**

PROPOSED ACCEPT IN PRINCIPLE.

1. In Figure 85-2 correctly illustrate TP2 and TP3 to include test fixture with dashed line.

2. Change: The electrical transmit signal is defined at the output end of the mated connector TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2.

3. Provide consistency in representation of TP test fixture of Figure 85-5 with Figure 85-11.

"Amplitude peak-to-peak" should be "Amplitude peak-to-peak (max)"

**Suggested Remedy**

Make indicated change

**Proposed Response**

**Response Status W**

PROPOSED ACCEPT.

Change from Amplitude peak-to-peak to "Amplitude peak-to-peak (max)"

Total Jitter excluding Data Dependent Jitter = TJ - DDJ

**Suggested Remedy**

A suggested method is given below:

Total jitter is measured with PRBS31 (pattern 3) at BER of 10^{-12}. Data Dependent jitter is measured with PRBS9 based on method given in 85.8.3 with following definition:

\[ DDJ = \max(d_1, d_2, ..., d_{256}) - \min(d_1, d_2, ..., d_{256}) \]

Section 85.8.3 would need to be updated or the other option is to create a standalone section.

Total Jitter excluding DDJ = TJ - DDJ

**Proposed Response**

**Response Status W**

PROPOSED ACCEPT IN PRINCIPLE. [Editor's note: Late comment for consideration by the Task Force]

Editor given license to implement suggested remedy.

Amplitude peak-to-peak (max)
Comment Type TR  Comment Status D
Tx jitter testing method and procedure is not defined.
Suggested Remedy
- Needs to give the Tx jitter testing method, including Tx equalization setting and receiver CDR condition.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
See response to comment #98

Comment Type TR  Comment Status D
Amplitude pk-to-pk (line 19) and Far-end transmit output noise (line 22-23) are max values and are not specified
Suggested Remedy
- Add (max) after those parameters.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
See suggested remedy and remedy to comment #87

Comment Type TR  Comment Status D
"Total jitter excluding DDJ" is a confusing and self-inconsistent name. Total jitter is not "total" anymore if DDJ is removed.
Suggested Remedy
- Change "Total jitter excluding DDJ" to uncorrelated total jitter (uTJ).

Proposed Response Response Status W
PROPOSED REJECT.
Total jitter excluding DDJ sufficiently characterizes the parameter.

Comment Type TR  Comment Status D
Data dependent jitter (DDJ) is not given
Suggested Remedy
- Give the data dependent jitter (DDJ) definition: DDJ is the zero-crossing time deviation referenced to the ideal bit clock timing derived from an averaged differential waveform where uncorrelated signal components have been removed.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
For committee discussion.

Comment Type TR  Comment Status D
Transmitter common mode output return loss is missing
Suggested Remedy
- The reference impedance for common mode return loss measurement shall be 25 ohms
  - Return loss >= -7 + 1.6 * f from -.05 to 2.5 GHz
  - -3  from 2.5 to 10 GHz

Proposed Response Response Status W
PROPOSED REJECT.
Common-mode return loss specified; see Table 85-4- Common-mode output return loss (min.).
Comment Type: ER  Comment Status: D
Special character
SuggestedRemedy
Please remove the special character at end of line
Proposed Response  Response Status: W
PROPOSED ACCEPT.

Comment Type: E  Comment Status: D
suggest rewording that attention is drawn to the far-end tx output noise
SuggestedRemedy
change The measured RMS deviation for the low loss cable assembly shall meet to
For the far-end transmitter output noise the measured RMS deviation for the low loss cable assembly shall meet:
change For the far-end transmitter output noise the measured RMS deviation for the high loss cable assembly
Proposed Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.

Change: The measured RMS deviation for the low loss cable assembly shall meet the values determined using Equation (85-2).

To: For the low loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85-2).

Change: The measured RMS deviation for the high loss cable assembly shall meet the values determined using Equation (85-3).

To: For the high loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85-3).
Cl 85 SC 85.8.3.2 P 250 L 4 # 144
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status D
There is a reference to the cable assembly ICN prior to its introduction.

SuggestedRemedy
add reference to 85.10.8 in first sentence of 85.8.3.2.

Proposed Response Response Status W
PROPOSED ACCEPT.
See suggested remedy

Cl 85 SC 85.8.3.3 P 251 L 36 # 51
Healey, Adam LSI Corporation

Comment Type TR Comment Status D
The transmitter output waveform requirements do not address the case where the transmitter is requested to INITIALIZE per 72.6.10.4.2.

SuggestedRemedy
Insert a new subclause under 85.8.3.3 with the heading "85.8.3.3.X Coefficient initialization" and containing the following text:

"When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72-5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be configure such that the ratio (c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1)) is 1.29 +/-10% and the ratio (c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1)) is 2.57 +/-10%. These requirements apply upon the assertion a coefficient status report of "updated" for all coefficients."

Proposed Response Response Status W
PROPOSED ACCEPT.
See suggested remedy.

Cl 85 SC 85.8.3.3 P 251 L 47 # 52
Healey, Adam LSI Corporation

Comment Type TR Comment Status D
Definitions of P2 and P3 are not correct.

SuggestedRemedy
Transpose P2 in Equation (85-11) and, in the following paragraph, define P3 to be the first Nw columns of P2.

Proposed Response Response Status W
PROPOSED ACCEPT.
See suggested remedy.

Cl 85 SC 85.8.3.3 P 252 L 14 # 60
Moore, Charles Avago Technologies

Comment Type T Comment Status D
pulse amplitude out Tx at TP2 is defined but DC gain is not. This could allow slow, high amplitude Tx, which is hard to equalize, to pass.

SuggestedRemedy
Specify Tx DC amplitude of Tx as "sum of linear fit pulse from step 3 divided by M from step 3" specify that DC amplitude is greater than 0.375 and less than 0.6 and that the peak of the linear fit pulse from step 3 shall be greater than 0.60*DC amplitude

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
For sub-task force discussion.

Cl 85 SC 85.8.3.4 P 253 L 42 # 100
Dudek, Mike QLogic

Comment Type T Comment Status D
Wrong reference (85.7.3.2.3 doesn't exist.)

SuggestedRemedy
Change 85.7.3.2.3 to 85.8.3.3.3

Proposed Response Response Status W
PROPOSED ACCEPT.
See suggested remedy.

Cl 85 SC 85.8.3.5 P 254 L 46 # 53
Healey, Adam LSI Corporation

Comment Type TR Comment Status D
Definitions of P2 and P3 are not correct.

SuggestedRemedy
Transpose P2 in Equation (85-11) and, in the following paragraph, define P3 to be the first Nw columns of P2.

Proposed Response Response Status W
PROPOSED ACCEPT.
See suggested remedy.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Clause, Subclause, page, line
<table>
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<th>Cl</th>
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<th>Response Status</th>
<th>Suggested Remedy</th>
<th>Comment Status</th>
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<th>Insertion loss spec between TP0 and TP2 and TP3 and TP5 is no longer needed</th>
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<tr>
<td>85</td>
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<td>Ghiasi, Ali Broadcom</td>
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<td>TR</td>
<td>W</td>
<td>Please follow or copy Fig 86A-12</td>
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<td>Please add min loss and follow or copy Fig 86A-12</td>
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<td>Palkert, Tom Xilinx/Luxtera</td>
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<td>T</td>
<td>W</td>
<td>Add diagrams similar to Fig 86-3 showing HCB, MCB and test points.</td>
<td>D</td>
<td>225</td>
<td>See response comment#198.</td>
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<td>Comment Type</td>
<td>Comment Status</td>
<td>PPI and CR will share a common interface when using the Type 1 connector. Therefore the test fixtures should have the same parameters.</td>
<td>Proposed Response</td>
<td>Response Status</td>
<td>W</td>
<td>PROPOSED ACCEPT IN PRINCIPLE. See response to comment #43</td>
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<td>Comment Type</td>
<td>Comment Status</td>
<td>Provide consistency with test fixture representation and labeling in Figure 85-5 with 85.10.10 Mated test fixtures Figure 85-11.</td>
<td>Proposed Response</td>
<td>Response Status</td>
<td>W</td>
<td>PROPOSED ACCEPT. See suggested remedy</td>
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<td>Comment Type</td>
<td>Comment Status</td>
<td>Figure 85-5 is not helpful and conflicts with definition in 85.8.3.7 and implies the loss include 100 nF and scope front end</td>
<td>Proposed Response</td>
<td>Response Status</td>
<td>W</td>
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<td>Comment Status</td>
<td>Some of the equations in Clause 85 introduce an extra variable name that is not used elsewhere. For example Equation 85-16 starts: ILtf(f) &lt;= ILtfmax(f) = (0.054)... The ILtfmax(f) variable is not referred to anywhere in the draft and only serves to complicate the equation. Where there are limit lines for both max and min for the same parameter (e.g., Equations 85-23 and 85-24) and the extra variables e.g. ILDmin(f) and ILDmax(f) are used elsewhere, they should be retained. Also applies to Equations 85-35, 85A-3 and 85A-4</td>
<td>Proposed Response</td>
<td>Response Status</td>
<td>W</td>
<td>PROPOSED ACCEPT. See suggested remedy</td>
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**TYPE:** TR/technical required ER/editorial required GR/general required  T/technical  E/editorial  G/general

**COMMENT STATUS:** D/dispatched  A/accepted R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn

**SORT ORDER:** Clause, Subclause, page, line
Cl 85 SC 85.8.3.7 P 256 L 3448 # 110
Ghiasi, Ali
Broadcom

Comment Type TR Comment Status D

The cable assembly test fixture is not consistent with Eq 86A-4. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

Suggested Remedy
Please use Eq 86A-4

PROPOSED ACCEPT IN PRINCIPLE.

Cl 85 SC 85.8.3.7 P 256 L 46 # 78
Dawe, Piers
Independent

Comment Type TR Comment Status D

The test fixture insertion losses aren’t maxima, they are reference losses. See text at 86A.5.1.1.

Suggested Remedy
Change “maximum” to “reference” here and in 85.10.9.

PROPOSED ACCEPT IN PRINCIPLE.

Cl 85 SC 85.8.3.7 P 256 L 46 # 177
Dudek, Mike
QLogic

Comment Type TR Comment Status D

Results will vary depending on the fixture insertion loss and 85.8.3.7 gives a maximum test fixture insertion loss (and no minimum). We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86A for commonality. Note that the PCB loss of the test fixture of clause 86A is what was used to derive the budget in Healey_03a_0709 (which doesn’t match what is here). We should also specify exactly what is included in the insertion loss.

Suggested Remedy
Change the Test Fixture insertion loss to a reference insertion loss (not just max) and use the same equations as 86A. Also add a sentence at the end of the Test Fixture insertion loss “The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements.”

State in 85.8.3.6.7 that the connector loss is not included in the test fixture insertion loss.

PROPOSED ACCEPT IN PRINCIPLE.

Delete: The maximum test fixture insertion loss shall meet the values determined using Equation (85-16).

Add: A reference test fixture loss is specified to account for differences between the insertion loss of an actual test fixture and the maximum test fixture insertion loss; this difference should be accounted for in the measurement results. The reference test fixture insertion loss shall meet the values determined using Equation (85-16).
<table>
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Dawe, Piers  
Independent  
Comment Type: T  
Comment Status: D  
85.8.3.4's "Insertion loss TP0 to TP2 or TP3 to TP5" is (above 200 MHz) consistent with the minimum SDD21 of host PCB, connector and HCB in 86A.6. The mated test fixtures insertion loss limits of 85.10.10.1 are consistent with the through response (SDD21) limits of mated HCB-MCB in 86A.5.1.1.2. Yet the test fixture insertion loss of 85.6.3.7 and the cable assembly test fixture insertion loss of 85.10.9 do not agree with the reference through responses (SDD21) of HCB and MCB in 86A.5.1.1.1. 85.8.3.7 and 85.10.9 use scaled backplane Amax while 86A.5.1.1.1 is based on experience with actual compliance boards. Because compliance boards are not backplanes (e.g. may use PTFE dielectric rather than FR4), the equations in 86A.5.1.1.1 are preferable.  
Suggested Remedy:  
Change equations 85-16 and 85-35 so they are consistent with 86A-4 and 86A-5 respectively.  
Proposed Response:  
PROPOSED ACCEPT IN PRINCIPLE.  
See response to comment #43.

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Ghiasi, Ali  
Broadcom  
Comment Type: TR  
Comment Status: D  
It is very difficult to read the graph with log scale  
Suggested Remedy:  
Please use linear freq scale  
Proposed Response:  
PROPOSED REJECT.  
No graph on page 256 line 48.

<table>
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DiMinico, Christopher  
MC Communications  
Comment Type: T  
Comment Status: D  
Comment #138 against Draft 2.1 was incorrectly implemented; a4 for test 1 values should be a4 = 0.03. See response to comment #138 Draft 2.1 -  
(2) Limits given by polynomial coefficients (low loss a1=2.15,a2=-.78,a4=.03) (high loss a1=6.04,a2=-0.94,a4=.08).  
Suggested Remedy:  
Change polynomial coefficients a4 from 0.3 to 0.03.  
Proposed Response:  
PROPOSED ACCEPT.  
See suggested remedy.

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Dudek, Mike  
QLogic  
Comment Type: TR  
Comment Status: D  
For the interference tolerance test the results will depend on the rise/fall times of the pattern generator. This section refers to clause 69A which calls out the max rise/fall times specified for the port under test, however we haven’t specified the max Tx rise/fall time in clause 85.  
Suggested Remedy:  
Insert an extra row in Table 85-7. "Pattern Generator Rise/Fall time". Value to be 47 ps for both test 1 and test 2.  
Proposed Response:  
PROPOSED ACCEPT IN PRINCIPLE.  
See suggested remedy. For committee discussion.

<table>
<thead>
<tr>
<th>CI</th>
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<th>Subclause</th>
<th>P</th>
<th>L</th>
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<tr>
<td>85</td>
<td>85.8.4.3.1</td>
<td>P258</td>
<td>38</td>
<td>178</td>
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</tr>
</tbody>
</table>

Dudek, Mike  
QLogic  
Comment Type: TR  
Comment Status: D  
We should state specifically where the test channel insertion loss is measured.  
Suggested Remedy:  
Change "The fitted test channel 1 or test channel 2 insertion loss ILTC(f)…” to "The fitted test channel 1 or test channel 2 insertion loss between the pattern generator and the output of the test fixture described in 85.10.9 ILTC(f)…”  
Proposed Response:  
PROPOSED ACCEPT IN PRINCIPLE.  
For committee discussion; see response to comment #91 and supporting material in moore_0x_0909.pdf.
Cl  85  SC  85.8.4.3.1  P  258  L  43  #  173
Dudek, Mike  QLogic

Comment Type  T  Comment Status  D

The units are wrong

SuggestedRemedy

It should state "Where f is the frequency in GHz."

Proposed Response  Response Status  W
PROPOSED ACCEPT. See suggested remedy.

Cl  85  SC  85.8.4.3.1  P  258  L  50  #  161
Dudek, Mike  QLogic

Comment Type  TR  Comment Status  D
The test cables attenuation for the interference tolerance test should have a specified value (not just a max value).

SuggestedRemedy
Delete the words "maximum allowable".

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE. For committee discussion. See response to comment#91 and supporting material in moore_0x_0909.pdf.

Cl  85  SC  85.8.4.6  P  259  L  18  #  162
Dudek, Mike  QLogic

Comment Type  T  Comment Status  D
We should be more explicit and normative about the location of the AC coupling capacitors

SuggestedRemedy
Replace "AC-coupling is considered to be part of the receive function for Style-2 40GBASE-CR4 connectors." with "AC-coupling shall be included in the receive function for Style-2 40GBASE-CR4 connectors."

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Change: AC-coupling is considered to be part of the receive function for Style-2 40GBASE-CR4 connectors.
To: AC-coupling is part of the receive function for Style-2 40GBASE-CR4 connectors.

Cl  85  SC  85.9  P  259  L  33  #  27
Anslow, Peter  Nortel Networks

Comment Type  E  Comment Status  D
spurious "."

SuggestedRemedy
Change "through.85A.7" to "through 85A.7"

Proposed Response  Response Status  W
PROPOSED ACCEPT.
See suggested remedy
Cl 85A SC 85A.2 P421 L11 # 135
DiMinico, Christopher MC Communications

Comment Type: E  Comment Status: D
Spelling voltage

Suggested Remedy:
- Change voltage to voltage

Proposed Response  Response Status: W
PROPOSED ACCEPT. See suggested remedy

Cl 85A SC 85A.2 P421 L18 # 166
Dudek, Mike QLogic

Comment Type: T  Comment Status: D
It is confusing that the sentence states that the specs are KR except for the transmitter characteristics in 85.8.3.8. 85.8.3.8 is the 10.3125G data rate specification which is the correct rate so doesn't need to be excluded.

Suggested Remedy:
- Use the same style as is used for the Rx. ie replace the sentence with: "The transmitter characteristics are summarized in Table 85A-1."

Proposed Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.

Change: The specifications at TP0 are summarized in Table 85A-1 and detailed in 72.7.1.1 through 72.7.1.11 with
the exception of the transmitter characteristics specified in 85.8.3.8.
To: The transmitter characteristics at TP0 are summarized in Table 85A-1.
Change: TP5 receiver characteristics are summarized in Table 85A-2.
To: The receiver specifications at TP5 are summarized in Table 85A-1.

The specifications at TP0 are summarized in Table 85A-1.

Cl 85A SC 85A.4 P422 L27 # 136
DiMinico, Christopher MC Communications

Comment Type: E  Comment Status: D
Spelling transmitter

Suggested Remedy:
- Change transmitter to transmitter

Proposed Response  Response Status: W
PROPOSED ACCEPT. See suggested remedy

Cl 85A SC 85A.4 P422 L31 # 180
Dudek, Mike QLogic

Comment Type: TR  Comment Status: D
The definition of TP1 has been adjusted (per Healey_03a_0709) to be at the input to the cable test fixture so it does not include all the PCB, resulting in an ambiguity. The loss specified on line 33 matches the loss we have in the budget for TP0 to TP1 (not for the complete PCB) but does not match the loss in equation 85A-1 which is only 5.18dB at Nyquist. Also Clause 86A allows a max 2x4.4dB for the total PCB loss on the assumption a host might use a lower loss connector.

Suggested Remedy:
- Either
  1. Delete "(ie the maximum insertion loss between TP0-TP1 and TP4-TP5)." and change the multiplier in equation 85A-1 from 0.3 to 0.506.
  2. Change the paragraph to "The maximum insertion loss allocation for the transmitter plus receiver differential controlled impedance printed circuit boards between each differential lane between TP0-TP1 and TP4-TP5 is determined using Equation (85A-1) and the coefficients b1 through b4 are given in Equation (85-16). The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards between these test points is 7 dB at 5.15625 GHz. Note that there is an additional 1.4dB allowance in the PCB loss for the equivalent PCB loss between TP1 and TP4 and the connectors." Change the multiplier in equation 85A-1 from 0.3 to 0.405

Proposed Response  Response Status: W
PROPOSED REJECT. Response to D2.1 comment#96 is to
use gustlin_04_0709 as reach objective guidance and subsequent input for insertion loss allocation as well as clause 85 comment resolution below. In gustlin_04_0709.pdf slide 12 “to reflect 3.5 dB (Host trace).”
The channel loss budget has been changed during D2.1 but this equation was not adjusted accordingly.

Suggested Remedy:
- Mated response loss 6.5 dB at 5.16 GHz, less 1.25 dB for HCB, less 0.5 dB for connector, leaves 4.75 dB loss per end.
- The 4.75 dB host PCB loss is based on assumption the connector has loss of 0.5 dB, higher loss connector require reducing channel PCB loss.

**PROPOSED REJECT.** The maximum channel insertion loss of 24.44 dB is consistent with D2.1 comment#96 resolution.

\[ IL(f) = IL_{max}(f) = 17.04 + (2 \times 6.5) - (2 \times 2.8) = 24.44 \text{ dB} \]

**Comment Type:** E  
**Comment Status:** D  
**Spelling insertion**

- Change insertion to insertion

**PROPOSED ACCEPT.**

See suggested remedy.

**Comment Type:** T  
**Comment Status:** D  
"is the frequency in MHz" should not be italicized.

**Suggested Remedy:**
- Correct two occurrences in this subclause, as well as an occurrence in 85A.7.

**PROPOSED ACCEPT.**

See suggested remedy.
The specified frequency range for channel insertion loss is inconsistent with the frequency range for cable assembly insertion loss in 85.10.2. It seems that they should be consistent.

This should also apply to the transmitter and receiver differential printed circuit board trace loss in 85A.4 and the channel insertion loss deviation in 85A.7.

**Suggested Remedy**
Recommend using a consistent frequency range throughout.

**Proposed Response**

**Response Status**
PROPOSED ACCEPT IN PRINCIPLE.

Specify the transmitter and receiver differential printed circuit board trace loss equations (85A-1) and (85A-2) from 50 MHz to 7500 MHz.

Specify the maximum channel insertion loss equation (85A-3) from 50 MHz to 7500 MHz.

**Comment Type**
E
**Comment Status**
D
**Comment**
For equations 85A-3, 85A-4 and 85A-5 the phrase "is the frequency in MHz" is shown in italic font. This should be normal font.

**Suggested Remedy**
For equations 85A-3, 85A-4 and 85A-5 change the phrase "is the frequency in MHz" to normal font.

**Proposed Response**

**Response Status**
PROPOSED ACCEPT IN PRINCIPLE.

See comment#58

**Comment Type**
T
**Comment Status**
D
**Comment**
Assuming my other comments are accepted to change to a reference loss for the test fixtures. The IL(mated) definition should be changed from maximum insertion loss to reference insertion loss.

**Suggested Remedy**
Change the definition of IL(mated) to "The reference insertion loss of the mated test fixture using equation (85-37)

**Proposed Response**

**Response Status**
PROPOSED ACCEPT IN PRINCIPLE.

Resolve final text with comment response comment#167 and comment#177.

For committee discussion

**Comment Type**
T
**Comment Status**
D
**Comment**
It would be very helpful to better define the test points and the losses and show where equation 85A-3 comes from.

**Suggested Remedy**
Insert at line 20. "The losses are shown diagnostically in NEW FIG"

Use slide 14 from Healey_03a_0709 as the basis of NEW FIG. Title the figure as "Illustration of loss budget" Labelling TP1 to TP4 as "IL(camax) (17.04dB)" TP0 to TP2 and TP3 to TP5 as "IL(host)(3.25dB)" and label the mated test fixture loss as "ILMatedTF (2.8dB)"

**Proposed Response**

**Response Status**
PROPOSED ACCEPT IN PRINCIPLE. Use slide 14 from Healey_03a_0709 as the basis for a figure illustrating loss budget . Title the figure as "Illustration of loss budget" Use D2.2 specified losses as well as resolution of Cl 00 comment# 40 as guidance for Tx and Rx PCB losses as basis for illustrated losses.

**Comment Type**
T
**Comment Status**
D
**Comment**
It would help understanding if IL(Camax) were better defined.

**Suggested Remedy**
Change IL(Camax) definition to "The maximum cable assembly insertion loss as measured with the cable assembly test fixtures using Equation (85-19)"

**Proposed Response**

**Response Status**
PROPOSED REJECT.

The IL(Camax) provided here is an upper bound calculated using equation (85-19) from the maximum allowed values of the polynomial coefficients a1, a2, and a4.
<table>
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<tr>
<th>Comment Type</th>
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<th>Proposed Response</th>
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</table>
| T            | D              | ILChmax(f) is a single named variable but it has been given two different curves. (equations 85A-3 and 85A-4) which is bad practice. In any case the maximum channel loss at 0.5m is not a very interesting characteristic. **Suggested Remedy**
|              |                | Delete the text between lines 21 and 35. As an alternative that would perhaps have more interest consider changing this section to minimum channel loss. **PROPOSED ACCEPT IN PRINCIPLE.**
| T            | D              | ILCh(f) = ILChmax(f) = (0.05 × ILCamax(f)) × (2 × ILHost(f)) - (2 × ILMatedTF(f))
|              |                | Equation (85A-4).
| T            | D              | Change: The maximum channel insertion loss with a cable assembly of 0.5 m between TP1 and TP4 is determined using Equation (85A-4).
| T            | D              | Note: Need to consider IL host min.
| T            | D              | Change: (85A-4)
|              |                | ILCh(f) = ILChmax(f) = (0.05 × ILCamax(f)) × (2 × ILHost(f)) - (2 × ILMatedTF(f))
| T            | D              | To: ILCh(f) = ILChmin(f) = (0.2 × ILCamax(f)) × (2 × ILHost(f)) - (2 × ILMatedTF(f))
| T            | D              | **Suggested Remedy**
|              |                | Add note the cable loss of 24.44 dB is when ILmated loss is 2.4 dB, if ILmated loss is less than 2.4 dB then ILch shall be reduced by the same amount **PROPOSED ACCEPT IN PRINCIPLE.**
| T            | D              | PROPOSED ACCEPT IN PRINCIPLE.
| T            | D              | The channel, TP0 to TP5 can not have the same ILD as the cable assymlby. If we are going to keep with the RL budgets from D2.2 then this number will need to be increased to allow for interations between the hosts and the cable. **Suggested Remedy**
|              |                | change the high frequency target from +/-1.7 to +/- 2.3 to account for this effect. **PROPOSED REJECT.** [Editor's note: Late comment for consideration by the Task Force]
| T            | D              | PROPOSED REJECT. [Editor's note: Late comment for consideration by the Task Force]
| T            | D              | The commenter has not provided a sufficiently complete proposal in this comment that would enable the implementation of suggested remedy. For sub-task force review. **Response**

**TYPE:** TR/technical required
**ER/editorial required**
**GR/general required**
**T/technical**
**E/editorial**
**G/general**

**COMMENT STATUS:** D/dispatched A/accepted R/rejected
**RESPONSE STATUS:** O/open W/written C/closed U/unsatisfied Z/withdrawn

**SORT ORDER:** Clause, Subclause, page, line

---

**Notes:**

- **Comment Type:** T/technical required
- **Comment Status:** D/dispatched
- **Proposed Response:** **PROPOSED ACCEPT IN PRINCIPLE.**
- **Response Status:** W/written
- **Comment:** The channel, TP0 to TP5 can not have the same ILD as the cable assembly. If we are going to keep with the RL budgets from D2.2 then this number will need to be increased to allow for interactions between the hosts and the cable.
- **Suggested Remedy:** change the high frequency target from +/-1.7 to +/- 2.3 to account for this effect.
- **Response:** The commenter has not provided a sufficiently complete proposal in this comment that would enable the implementation of suggested remedy. For sub-task force review.
For the cable assembly, specifications for insertion loss to crosstalk ratio were replaced with integrated crosstalk noise requirements. It seems that the channel requirements should follow suit.

**Suggested Remedy**
Refer to healey_01_0909.pdf for proposed text for channel integrated crosstalk noise recommendations.

**Proposed Response**
PROPOSED REJECT. The commenter has not provided a sufficiently complete proposal in this comment that would enable the implementation of suggested remedy.

For committee discussion see healey_01_0909.pdf.

This whole section seems to be not in sync with methods agreed to in the last meeting and should be expressed in ICN vs channel loss to be consistent with the way the cable is being described and tested.

**Suggested Remedy**
Convert to ICN like was done for section 85.10.8

"(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)" is unclear and does not conform with the style manual.

**Suggested Remedy**
Change "(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)" to "(i.e., the maximum insertion loss between TP0 and TP1 and between TP4 and TP5)"

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE. See response to comment#168.

The PMD electrical definition XLPPI and CPPI has no MDI definition

**Suggested Remedy**
Please MDI definition from CL 85.11

"Optical power at TP3 => stressed receiver sensitivity (max) in OMA in Table 86.8" This is -5.4 dBm (OMA). However, in Table 86-7 "Characteristics of signal within, and at the receiving end of, a compliant optical channel" we see that the OMA, each lane can be -7.9 dBm. Consequently, a fully compliant link can have SIGNAL_DETECT = FAIL

**Suggested Remedy**
In Table 86-5 change:
"Optical power at TP3 => stressed receiver sensitivity (max) in OMA in Table 86.8" to "Optical power at TP3 => Optical Modulation Amplitude (OMA), each lane in Table 86.7"

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.
In Table 86-5 change:
"Optical power at TP3 => stressed receiver sensitivity (max) in OMA in Table 86.8" to "Optical power at TP3 => Minimum OMA, each lane, in Table 86.7"
In table 86-8, the attribute, "Receiver jitter tolerance signal level in OMA, each lane" is really a test condition and as such should be included with the other jitter tolerance test conditions.

**Suggested Remedy**
In table 86-8, move the attribute, "Receiver jitter tolerance signal level in OMA, each lane" so that it is included with the other jitter tolerance test conditions.

**Proposed Response**

**Response Status**: W

PROPOSED REJECT.

The "Receiver jitter tolerance signal level in OMA, each lane" is the test in the same way as "Stressed receiver sensitivity in OMA, each lane" is a test. If the optical power required to give $10^{-12}$ BER in the presence of the specified jitter is above this limit, the device fails.

---

In table 86-8, unlike the case for Stressed receiver sensitivity which has an explicit entry for the attribute, there is no entry for a receiver tolerance attribute, only conditions for such. Further, there is no explicit link to the test definition in 86.8.4.8 which may compound the confusion of the missing test entry. Finally, since this is a test of the ability of a system to track low frequency jitter, it would be helpful to note (similar helpful information are included in footnotes a & c) that the test is not intended for subsystems where CDR and/or bit-error-detector functions is/are not included. See figure 86-14 which shows a System under test, SUT, comprising a PCS, PMA and PMD. Without the CDR and bit-error-detector of the PMA and/or PCS, equipment external to the SUT would be needed and the test would become, primarily, a test of this external equipment.

**Suggested Remedy**
In Table 86-8, insert an entry, "Receiver jitter tolerance in BER, each lane" above the "Conditions of receiver tolerance test". Append a footnote indicator at the end of the entry.

**Proposed Response**

**Response Status**: W

PROPOSED ACCEPT.

The stressed receiver test refers to 52.9.9 for the test method which explicitly calls for a BER of $10^{-12}$.

---

This says "an ideal 4th order Bessel Thompson response". However all other occurrences use "fourth" rather than "4th" and the style manual also states that "In general text, isolated numbers less than 10 should be spelled out."

**Suggested Remedy**

Change "an ideal 4th order" to "an ideal fourth order".

**Proposed Response**

**Response Status**: W

PROPOSED ACCEPT IN PRINCIPLE.

Change "an ideal 4th order Bessel Thompson" to "an ideal fourth-order Bessel-Thomson"
<table>
<thead>
<tr>
<th>Page 48 of 59</th>
<th>9/17/2009 3:35:21 PM</th>
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<td><strong>CI</strong> 86A  <strong>SC</strong> 86A.1  <strong>P</strong> 427  <strong>L</strong> 6  # 63</td>
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<td>Pettrilla, John Avago Technologies</td>
<td>Dawe, Piers Independent</td>
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**IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments**

**WG 2nd recirculation ballot**

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<th>Comment Status</th>
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<tbody>
<tr>
<td><strong>Clause 68.6.11</strong> is referenced with exceptions. There is no exception declared for the requirement in 68.6.11, &quot;The optical waveform is connected ... and mode-conditioning patch cord suitable for 62.5/125 um fiber&quot;. The &quot;mode-conditioning patch cord suitable for 62.5/125 um fiber&quot; does not seem necessary for SR and, if not, is an unnecessary burden. If such a mode-conditioning patch cord is required, then further definition of its characteristics and use are required.</td>
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<td><strong>Proposed Response</strong></td>
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<tr>
<td><strong>In 68.6.11 add another exception, f), to the list that states, 'the mode-conditioning patch cord suitable for 62.5/125 um fiber is not used'.</strong></td>
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<td><strong>Response Status</strong></td>
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**Petrilla, John Avago Technologies**

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<tbody>
<tr>
<td>In the overview it's said about PPI that, &quot;It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside.&quot; As PPI can similarly support 40GBASE-LR4 modules, the overview should make that visible. Further PPI does not preclude use of CDRs within a module.</td>
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<tr>
<td><strong>Proposed Response</strong></td>
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<tr>
<td><strong>Change from, &quot;It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside.&quot; to &quot;It allows the construction of compact optical transceiver modules for 40GBASE-SR4, 40GBASE-LR4 or 100GBASE-SR10 with no clock and data recovery circuits required inside.&quot;</strong></td>
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**Dawe, Piers Independent**

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<th>Comment Status</th>
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<tr>
<td>In D2.2, &quot;Parallel Physical Interface&quot; is abbreviated to nPPI. As we have decided not to use nAUI in the document, this would be the only such nSomething abbreviation in 802.3. The word &quot;Parallel&quot; implies multiple lanes so &quot;n&quot; has no purpose any more. Other multi-lane things e.g. PMD types put the multiple number at the end not the beginning.</td>
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<tr>
<td><strong>Proposed Response</strong></td>
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**Dawe, Piers Independent**

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<tr>
<td><strong>In the overview it's said about PPI that, &quot;It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside.&quot; As PPI can similarly support 40GBASE-LR4 modules, the overview should make that visible. Further PPI does not preclude use of CDRs within a module.</strong></td>
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</tr>
<tr>
<td><strong>Change from, &quot;It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside.&quot; to &quot;It allows the construction of compact optical transceiver modules for 40GBASE-SR4, 40GBASE-LR4 or 100GBASE-SR10 with no clock and data recovery circuits required inside.&quot;</strong></td>
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**Dawe, Piers Independent**

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<td><strong>D/dispatched A/accepted R/rejected</strong></td>
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<td><strong>RESPONSE STATUS:</strong></td>
<td><strong>O/open  W/written  C/closed  U/unsatisfied Z/withdrawn</strong></td>
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<tr>
<td><strong>SORT ORDER:</strong></td>
<td><strong>Clause, Subclause, page, line</strong></td>
</tr>
</tbody>
</table>
Cl 86A  SC 86A.4  P431  L27  # 231
Misek, Brian  Avago Technologies

Comment Type T  Comment Status D
The inclusion of DDPWS for host Rx testing makes no sense at all to me. I have tried to find the reason behind this inclusion and can not find the rational. In fact I can find no comment or comment reponse that calls for this in the comments on 2.0 which led to this being inserted as a TBD. The only comment resolution I can find for the value has no technical backing for the number.
This type of jitter, is no more difficult to deal with for an electrical host Rx in a limiting application then jitter induced by ISI behind the limiter function. The inclusion in the spec only serves to make the test harder to create. The test system must have a second Sine generator and wideband noise source, to modulate the amplitude of a signal only to have it clipped with a limiter. I think that burdening the host vendors with this test for no proven benefit is not in the best interest of this group. If there is some proven benefit to this test parameter I would like to see it, which should of been in the record for why it was included. Simultaneous meeting of J2 and J9 can be done in a more straght forward manner with edge modulation by random interference for J9 control(if needed) and the existing ISI for J2 control.

SuggestedRemedy
Remove DDPWS from Table 86A-4
Remove line 48 components dealing with this "sinusoidal interference (SI), and random interference (RI), all" Remove line 51 on page 442 "The test signal at TP4 has DDPWS as defined by Table 86A-4."
Remove Voltage stress block from Figure 86A-9
Remove paragraph at line 11 page 443 "A voltage stress is to be applied before the limiter function. This stress is composed of a single tone sinusoidal interferer (SI) in the frequency range 100 MHz to 2 GHz and a broadband noise source (RI) with a minimum power spectrum -3 dB point of 6 GHz and minimum crest factor of 7. It is the intent that this combination of voltage stress and limiting function introduce pulse-shrinkage jitter behavior. However no more than 20% of the J2 Jitter is created by the sinusoidal interferer."
Change line 5 page 444 from 80% to 100% and remove the following 2 lines.
"The sinusoidal interferer amplitude is then turned on and adjusted until the required level of J2 Jitter is achieved. If necessary the sine interferer is readjusted to obtain the required level of J2 Jitter and if the sinusoidal interferer is changed then the random interferer is readjusted to obtain the required level of J9 Jitter. Iterative adjustments of the sinusoidal interferer and random interferer are made until the required values of both J2 Jitter and J9 Jitter are achieved."

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
The DDPWS spec constrains the variety of test stressor eyes that would be allowed if just J2 and J9 specs were in place.
The test configuration shown in figure 86A-9 is an example of a test configuration that could be used to generate a test signal conforming to table 86A-4. In order to make this clearer, change title of 86A-9 to "Example jitter tolerance test configuration"

[Editor's note: Late comment for consideration by the Task Force]

Cl 86A  SC 86A.4.1  P428  L21  # 72
Dawe, Piers  Independent

Comment Type T  Comment Status D
If Table 86A-3, nPPI module electrical output specifications at TP4, has a termination mismatch spec, why doesn’t Table 86A-1, nPPI host electrical output specifications at TP1a? I don’t believe that a 1 MHz measurement will be affected by the few inches of PCB trace in the host, as was alleged.

SuggestedRemedy
Add row, Termination mismatch at 1 MHz, max 5%.

Proposed Response Response Status W
PROPOSED ACCEPT.
<table>
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<tr>
<th>Comment Type</th>
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<td>D</td>
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<td>ghiasi_03_0909</td>
<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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Comment 131: With current set of specifications the SerDes transmitter may have very large amount of de-emphasis 3-5 dB resulting in significant distortion at TP1a and also see comment 216/218 on D2.1

Suggested Remedy:
The options here are either limit max DDJ to about 0.125 UI or max 3 dB de-emphasis, see ghiasi_03_0909

**Proposed Response**

**Response Status**

**PROPOSED REJECT.**

J2 spec constrains DDJ and eye mask constrains excessive emphasis. Although ghiasi_03_0909 shows an example module/host combination with a near failing Tx eye mask at TP2, there is insufficient information to determine the corrective action required in the spec to avoid a potential eye-mask issue. Further work is invited.

Comment 35: In the equations of clause 86A, the phrase "f is the frequency in gigahertz" is used. In the rest of the draft (27 instances) this is "f is the frequency in GHz". In the base document the words "gigahertz", "megahertz" or "kilohertz" do not occur at all.

**Suggested Remedy**

Change "gigahertz" to "GHz" throughout clause 86A (14 instances)

**Proposed Response**

**Response Status**

**PROPOSED ACCEPT.**

Comment 191: Figure 86A-1 does not declare the units for the y-axis. While the units may be inferred from the associated equations, the y-axis title lists SDD11 and similar terms but the equations are '20 log [...] = ...', so there's not a one-to-one match. For consistency, if the 20 log [...] remains in the equation it should be in the axis title. Otherwise we appear to be saying that 20log10(|SDD11|) = SDD11. Further, while the units for the x-axis could also be inferred from the equations they are explicit in the x-axis title. Similar cases occur for figures 86A-2, 3, 4, 5 & 6.

**Suggested Remedy**

1. If the 20 log(...) terms remain in the reflection and response equations, then they should be included in the associated y-axis titles for figures 86A-1, 2, 3, 4, 5 & 6.

2. dB should be included as the y-axis units for figures 86A-1, 2, 3 & 4.

**Proposed Response**

**Response Status**

**PROPOSED ACCEPT IN PRINCIPLE.**

Needs to be consistent with response to comment 15

Comment 199: The title for figure 86A-1 is, "Reflection specifications" but is more properly, 'Reflection specifications illustrations' as the specifications are in the associated table and equations. Even the text, see page 428, line 44 states, "the limit given in Equation 86A-2 and illustrated in Figure 86A-1." Similar issues exist with Figures 86A-2, 3, 4, 5 & 6.

**Suggested Remedy**

Change the title for figure 86A-1 from, "Reflection specifications", to 'Reflection specifications illustrations'. Do likewise for figures 86A-2, 3, 4, 5 & 6.

**Proposed Response**

**Response Status**

**PROPOSED REJECT.**

The title follows the precedent set in the rest of the document and in clause 52.
<table>
<thead>
<tr>
<th>Cl</th>
<th>86A</th>
<th>SC 86A.4.2</th>
<th>P 430</th>
<th>L 14</th>
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<td>PROPOSED REJECT. see also response to comment 131</td>
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<td>In Table 86A-4, unlike table 86-8, there is no explicit indication of a low frequency SJ jitter tolerance requirement, although there is much detail in the associated 86A.5.3.8, specifically the template in 86A.5.3.8.6. It doesn't seem good practice where a table of requirements is available not to indentify all significant attributes.</td>
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<td>In Table 86A-4, add a row, 'Applied sinusoidal jitter', for low frequency SJ to the receiver signal tolerance test conditions. Enter 'TP4' in the Test Point column, 'See 86A.5.3.8' in the Spec.values column, and leave the Units and Conditions columns blank.</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE. Response to comment 194, if adopted, gives pointer to 86A.5.3.8. However, there is no need to add all of the test details to the table. This type of added jitter is not called out in the table in several other places in the draft and also in the base standard.</td>
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<td>In Table 86A-4, the value for the Transition time value is shown as, &quot;34 TBC&quot;. A predetermined transition time value may preclude generating a stressed signal that reaches all of the eye mask coordinates, J2, J9 and DDPWS simultaneously. Since there appears to be more value having an input signal that simultaneously stresses min and max signal levels, eye mask corners, J2, J9 and DDPWS, a transition time spec may be redundant.</td>
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<td>Delete the Transition time requirement from Table 86A-4 and in 86A.5.3.8.5 append to the end of the sentence, &quot;The vertical opening and peak level specifications are verified.&quot; such that eye mask coordinates X1, X2, Y1, Y2, and jitter values DDPWS, J2, J9 are all simultaneously met! In 86A.5.3.8.5 page 444, line 12, change the phrase, &quot;... the amplitude and the transition time are as given in Table 86A-4.&quot; to &quot;... and the amplitude are as given in Table 86A-4.&quot;</td>
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<td>PROPOSED REJECT. Commenter invited to submit material which justifies removing the Transition time spec.</td>
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Comment Type: T  Comment Status: D

Transition time is given as 34 ps TBC.

Suggested Remedy:
Confirm it or change it to a better number. Delete "TBC".

Proposal Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Delete TBC

Comment Type: T  Comment Status: D
The MCB SDD21 is expected to be approximately half the loss of the HCB, but the frequency independent term ratio is far larger.

Suggested Remedy:
Change MCB frequency independent term from -0.0006 to -0.006

Proposal Response  Response Status: W
PROPOSED ACCEPT.

Comment Type: T  Comment Status: D
While adjusting the cosmetics of equation 86A-7, a sign error has crept in.

Suggested Remedy:
Change +0.861 back to -0.861.

Proposal Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.

In equation 86A-7 change "+0.861" to "-0.861"
In equation 86A-8 change "-28.85" to "+28.85"

See also comments 44, 68 and 232

Comment Type: TR  Comment Status: D
Mated test fixture crosstalk loss in current draft are place holder and some of the limit specially PSFXT will impact the measurements accuracy

Suggested Remedy:
For the new limits please see ghiasi_01_0909

Proposal Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
see also 74 Task Force to discuss following presentation of ghiasi_01_0909

Comment Type: T  Comment Status: D
Is the position of bit 1 in PRBS9 defined in 802.3? If so please cite a reference? If not delete, "These are bits 10 to 18 and 1 to 14, respectively." or create a definition for bit 1.

Suggested Remedy:
Unless a definition that permits locating bit 1 exists, delete the sentence, "These are bits 10 to 18 and 1 to 14, respectively." Otherwise cite the definition.

Proposal Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Change "These are bits 10 to 18 and 1 to 14, respectively." to "These are positions 10 to 18 and 1 to 14, respectively, where positions 1 to 9 are the run of nine zeros."
The 'shall' in "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." seems more an instruction to the editors than to implementers.

**Suggested Remedy**

Change, "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." to "A compliant host electrical receiver signal tolerance shall satisfy the requirements defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6."

**Proposed Response** Proposed Accept in Principle.

Mark, Gustlin Cisco

**Comment Type** TR

**Comment Status** D

Formula 86A-19 seems incorrect from in the range from 0.2 to 7GHz, should be = -0.114-0.8914*f-0.846*f

**Suggested Remedy** Change the + to a -.

**Proposed Response** Proposed Accept.

see comments 44, 68, and 232

---

The term LB in figure 86A-11 is not defined. Assuming it's the same LB as in 87 and 88, the definition in 88.8.10, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested." can be referenced or copied and pasted below figure 86A-11.

**Suggested Remedy** Insert after figure 86A-11, the definition for LB, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

**Proposed Response** Proposed Accept in Principle.

Mark, Gustlin Cisco

**Comment Type** T

**Comment Status** D

Sign error in equation 86A-19

"+ 0.846f" should be "+ 0.846f"

**Suggested Remedy** Change

"+ 0.846f" should be "+ 0.846f"

**Proposed Response** Proposed Accept in Principle.

see comments 44, 68, and 232

[Editor's note: Late comment for consideration by the Task Force]

**Comment Type** T

**Comment Status** D

Sign error in equation 86A-19. It should be a scaled version of D2.1 86A-20.

**Suggested Remedy** Change + 0.846f to - 0.846f.

**Proposed Response** Proposed Accept in Principle.

see comments 44, 68, and 232

---

The term LB in figure 86A-11 is not defined. Assuming it's the same LB as in 87 and 88, the definition in 88.8.10, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

**Suggested Remedy** Insert after figure 86A-11, the definition for LB, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

**Proposed Response** Proposed Accept in Principle.

Piers Dawe, Independent

**Comment Type** T

**Comment Status** D

Sign error in equation 86A-19. It should be a scaled version of D2.1 86A-20.

**Suggested Remedy** Change + 0.846f to - 0.846f.

**Proposed Response** Proposed Accept in Principle.

see comments 44, 68, and 232

---

See king_01_0909 for example table and text.
Comment Type: T  Comment Status: D

The minimum loss at Nyquist from TP0 to TP2 is only 2.08dB based on equation 86A-20. The PCB loss is 1.26dB without the connector (equation 86A-4) leaving only 0.82dB for the connector and host PCB. ie this minimum recommended loss is not really doing anything.

Suggested Remedy

PROPOSED REJECT.

No change to document proposed.

Comment Type: TR  Comment Status: D

Equation 86A-20 is wrong. (requires gain at high frequency and has a discontinuity) and doesn't match Figure 86-12

Also with the correction the minimum loss at Nyquist from TP0 to TP2 is only 2.08dB based on equation 86A-20. The PCB loss is 1.26dB without the connector (equation 86A-4) leaving only 0.82dB for the connector and host PCB. ie this minimum recommended loss is not really doing anything.

Suggested Remedy

Add a row to the equation
0.01<f<1  value 0
Change the existing first row to +0.5 - 0.5*f

Consider also increasing the minimum loss at Nyquist by approx 0.5dB by changing this existing first row to 0.6 - 0.6*f and changing the second row to -3.7

Proposed Response  Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.
change sign to make the first row +0.5 - 0.5*f

No justification provided or concensus for changing other values.
Stressed receiver sensitivity shall be within the limits given in Table 87-8 for 40GBASE-LR4 if measured using the method described in 87.8.11.1 and 87.8.11.5 with the conformance test signal at TP3 as described in 87.8.11.2.

Stressed receiver sensitivity compliance is a normative requirement, but the test setup has a number of variable parameters: BT filter parameters, sinusoidal jitter frequency, sinusoidal amplitude interferer frequency and amplitude, etc.

Given the wide range of alternative configurations that could meet the stressed eye VECP and SEJ values, is it the intention of the committee that all such test setups be tested against the Stressed receiver sensitivity requirement?

i.e. In order to be compliant is it sufficient to demonstrate compliance at just one such configuration, or does failure at any such configuration mean an implementation is non-compliant?

I see hazards in either position.
A single pass might allow an implementation to select a set of parameters particularly favorable in order to pass.
Conversely demonstrating that there is no single combination of parameters that does not cause a failure would cause testing to take an impracticable amount of time.

Suggested Remedy
Add some text indicating the committee's intention.

There will be a contribution at the September interim to support this comment

**Proposed Response**

**Response Status**: W

PROPOSED REJECT. (Editor's note Subclause changed from 8.11.1 to 87.8.11.1)

If all such test setups needed to be tested against the Stressed receiver sensitivity requirement, then the test definition would say so.

With any of the tests defined in the draft there is the possibility that one arrangement for measurement may pass a device while another fails it.

The stressed signal for SRS testing is tightly constrained: the calibration reference receiver filter parameters are exact, and the results of sinusoidal amplitude and jitter interferers is precisely defined.

"The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz"

Providing such a wide range of frequency (in addition to amplitude) makes compliance testing difficult.

Suggested Remedy
Select a single sinusoidal amplitude interferer frequency of 1GHz.

There will be a contribution at the September interim to support this comment

**Proposed Response**

**Response Status**: W

PROPOSED REJECT. (Editor's note Subclause changed from 8.11.1 to 87.8.11.1)

The added sinusoidal jitter frequency is constrained to be at least a factor of ten higher than the loop bandwidth of the receiver CDR used, making it a specific frequency is an unnecessary constraint on test equipment manufacturers. This variation is the same as was used in subclause 52.9.9.1.
Comment Type: TR
Comment Status: D

87.8.11.2 has a definition of VECP that contradicts the rest of 802.3. Detail follows:
In 52.9.9.2, VECP is defined as 10 log(OMA/AO). Applies to 10G, scrambled, including 10GEPON. Also applies in 86.8.4.7.
In 58.7.11.2, VECP is defined as 10 log10(AN/AO), where AN is the normal amplitude without ISI, as measured in Figure 53-12. Applies to 10GBASE-LX4 (3.125 GBd, block coded).
10GBASE-LRM doesn't use VECP.
In D2.2 87.8.11.2, VECP is defined as 10 log(AN/AO) (sign error), where "AN is the normal amplitude without ISI, as shown in Figure 87-4." Unlike Figure 53-12, Figure 87-4 shows AN as a difference of means of histograms at crossing time, which is not exactly OMA nor the "normal amplitude without ISI". (52.9.9.2 says "OMA is the normal amplitude without ISI, as shown in Figure 52-11" but 52.9.5 gives a precise definition.) D2.2 88.8.5.1 uses the 52.9.9.2 definition of VECP while 88.8.10 uses 87.8.11.

Suggested Remedy:
Definitions and stressed eye generators will be shared across 40GBASE-LR4, 10GBASE-LR, 10GBASE-ER and 10GEPON, so 87.8.11.2 should conform.
Change the definition of VECP to 10 log10(OMA/AO).
To avoid confusion, modify Figure 87-4 to remove "AN" (which is the "Approximate OMA" of Fig 52-11 and "Approximate AN" of Fig 58-9, and it's not relevant) and remove the histograms at the crossing time.
If wished, add pointers to illustrate where OMA would be, at the settled one and zero levels (this would be better done with the waveform of Figure 53-12 or 58-9).

Proposed Response: PROPOSED ACCEPT IN PRINCIPLE.
In equation 87-1 change "10xlog(AN/AO)" to "10xlog(OMA/AO)" and "AN is the normal amplitude without ISI, as shown in Figure 87-4." to "OMA is the optical modulation amplitude as defined in 87.8.5."
In Figure 87-4 remove AN and related histograms etc. In 88.8.5.1 change as defined in 52.9.9.2 is less than to "as defined in 87.8.11.2 is less than".

Comment Type: TR
Comment Status: D

With the sinusoidal interference and sinusoidal jitter turned off, greater than two thirds of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the fourth-order Bessel-Thomson filter.

Provide a range rather than a limit for the Bessel-Thomson Filter contribution

Suggested Remedy:
Change to:
"With the sinusoidal interference and sinusoidal jitter turned off, between 0.6 and 0.7 of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the fourth-order Bessel-Thomson filter."

There will be a contribution at the September interim to support this comment

Proposed Response: PROPOSED REJECT.
This text is drawn from clause 52 and includes a range of 0.667 to 1.0 of the VECP. The proposed changes restrict the range and is an unnecessary constraint on test equipment manufacturers.

Comment Type: ER
Comment Status: D

The sinusoidal jitter added should result in at least 0.05 UI peak to peak DCD.
This is the only indication of a minimum DCD requirement in the draft and is not normative anyway. This sentence is redundant and should be removed.

Suggested Remedy:
Remove the sentence.

Proposed Response: PROPOSED ACCEPT IN PRINCIPLE.
Many requirements are contained at only one place in the draft. To be discussed by the Task Force.
All but two 10G Ethernet Bessel-Thomson responses for measurement (even the one in 87.8.9) have a bandwidth / reference frequency fr / 3 dB upper electrical cutoff frequency of 7.5 GHz. 86.8.4.4 has 6.2 GHz for a reason. Here we have 7.73 GHz. Implementers are going to use the same 10G instruments for 40GBASE-LR4 as for 10GBASE-L and 10GEPON, so this difference, between 7.5 and 7.73, is not practical.

Proposed Remedy
Change 7.73 to 7.5.

Elsewhere in 802.3 where a Bessel-Thomson response for measurement (scope or reference receiver) is specified, it isn't called "3 dB upper electrical cutoff frequency" but "bandwidth" or "reference frequency fr" or simply '7.5 GHz Bessel-Thomson'.

Proposed Remedy
Please change "3 dB upper electrical cutoff frequency" to "reference frequency fr", or change "ideal fourth-order Bessel-Thomson response with a 3 dB upper electrical cutoff frequency of * GHz." to "ideal * GHz fourth-order Bessel-Thomson response", or "ideal fourth-order Bessel-Thomson response with a bandwidth of * GHz."

But please don't try to change "response" to "loss!"

Proposed Remedy
Please move L0-L3 before and after optical mux.

Proposed Remedy
Please update figure to show gearbox and CAUI

CAUI is an optional interface and therefore may not be present. The gearbox function is within the PMA function and a possible future 25G electrical interface would not need it.

Proposed Remedy
Please update figure to show gearbox and CAUI

Stress receiver sensitivity has corner frequency of 10 MHz also see comment 224 and 225. D2.1 can limit the receiver to analog type instead of more efficient lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remain even in the case of future generations where ASIC/SerDes operate at 25 G!

Suggested Remedy:
Propose to consider corner frequency of 7 MHz instead of current 10 MHz and change 100 KHz to 70KHz. Higher CRU BW has very little benefit on the VCO noise and power supply noise but significant penalty on the receiver, see ghiasi_02_0909

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
See Response to Comment # 127
Comment Type: TR  Comment Status: D

The CRU BW for the TDP measurement is defined to be 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficient lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remain even in the case of future generations where ASIC/SerDes operate at 25 G!

Suggested Remedy

Propose to consider CRU BW 7 MHz instead of current 10 MHz. Higher CRU BW has very little benefit on the VCO noise and power supply noise but significant penalty on the receiver, see ghiasi_02_0909

Proposed Response  Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.
To be considered by the Task Force whether to change from 10 MHz to 7 MHz.

Either stay with 10 MHz:
In Table 88-13 correct the formula:
change ”2 x 10^5/ f” to ”5 x 10^5/ f”

Or Change to 7 MHz:
In 88.3.2 change ”clock and data recovery units’ high frequency corner bandwidths are 10 MHz” to ”clock and data recovery units’ high frequency corner bandwidths are 7 MHz”
In 88.8.3.3 change ”The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 10 MHz” to ”The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 7 MHz”
In 88.8.8 change ”the clock recovery unit’s high frequency corner bandwidth is 10 MHz.” to ”the clock recovery unit’s high frequency corner bandwidth is 7 MHz.”
In Table 88-13 change 100 kHz to 70 kHz (2 places), change 10 MHz to 7 MHz (2 places), change ”2 x 10^5/ f” to ”3.5 x 10^5/ f”

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Comment Type: E  Comment Status: D

There is a wrap around error in the listing for Clause 52.

Suggested Remedy

fix wrap-around error for Clause 52 entry.

Proposed Response  Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.
Fix ToC formatting as appropriate