# Unconfirmed Minutes - Multiple MCS IEEE 802.3bn EPoC Ad Hoc - 011713

## Attendance

| Attendee | Present |
|---|---|
| Alan Brown – Aurora | x |
| Andrea  Garavaglia – Qualcomm | x |
| Avi Kliger – Broadcom | |
| Bill Powell – ALU | x |
| Charaf Hanna – ST Micro | |
| Christian Pietsch – Qualcomm | x |
| Curtis Knittle – CableLabs | x |
| Dave Urban – Comcast | |
| David Law – HP | |
| Duane Remein – Huawei | x |
| Dylan Ko – Qualcomm | |
| Ed Boyd – Broadcom | x |
| Eugene Dai – Cox | x |
| George Hart – Rogers | |
| Hesham ElBakoury – Huawei | |
| Jim Farmer – Aurora | |
| Joe Solomon – Comcast | |
| Joe Solomon – Comcast | x |
| John Dickinson – Brighthouse | |
| John Ulm – Motorola | x |
| Jorge Salinger – Comcast | x |
| Juan Montojo – Qualcomm | |
| Leo Montreuil – Broadcom | x |
| Lup Ng – Cortina | x |
| Marek Hajduczenia – ZTE | x |
| Mark Laubach – Broadcom | x |
| Matt Schmitt – CableLabs | |
| Michel Allard – Cogeco | x |
| Mike Darling – Shaw | |
| Mike Emmendorfer – Arris | x |
| Nicola Varanese – Qualcomm | x |
| Ony Anglade – Cox | x |
| Patrick Stupar – Qualcomm | |
| Peter Wolff – Titan Photonics | x |
| Raanan Ivry – Wide Pass | x |
| Ramdane Krikeb – Videotron | |
| Saif Rahman – Comcast | x |
| Satish Mudugere – Intel | |
| Steve Shellhammer – Qualcomm | x |

| | |
|---|---|
| Thushara Hewavithana – Intel | |
| Tim Brophy – Cisco | |
| Tom Staniec – Cohere | x |
| Tom Williams –Cablelabs | |
| Venkat Arunarthi – Cortina | |
| Volker Leisse - CEL | |
| Yitshak Ohana - Broadcom | |

## Patents Policy

- Everyone familiar with the policy; no response to call for patents

## Upcoming Meeting

Will have F2F ad hoc meeting on Wednesday, 1/23 at 7:30 AM in Phoenix

Future meetings TBD, based on outcome of the interim meeting

## Any additional comments on the Qualcomm Presentation

Last meeting, Qualcomm presented; any additional comments?

No jitter issue? Jitter concerned with is the MAC layer data passing through

- Where are the reference points for the jitter?
- Basic issue is the shuffling of the packets; have backpressure, then releasing in groups. In that process, packets are held back to be grouped, causing the jitter
    - Jitter accumulated at scheduling?
        - Yes; jitter accumulates depending upon the block size. In some scenarios, have to wait for the shuffling time
    - Phy proposal stated that the penalty was too much and would require a buffer on the other end to remove the jitter; leave the jitter for the upstream. It already has to poll and combine into packets
    - Agree that the jitter problem shouldn't be ignored and pushed into another layer
- Jitter is introduced during step 1 on slide 2
    - Not just control plane, but on data packets going through above
    - It is user/higher layer data
    - Have to consider that the case assumes 4 profiles; there could be different tuning. The packets were group to improve the efficiency of the encoder.
- When the jitter is calculated, and based on 90% FEC, what would the penalty be?
    - 2 cases: with 16k codeword and other with 8k bits
        - 16k penalty: below 3 % if you do nothing at the scheduler (no additional attempt to fill the codeword)
            - If you attempt to fill the codeword, it's below 2%
            - Is the 2% an average, best case, or worst case?
                - In testing over 4 profiles and packets from 64bytes and 1500 bytes, then calculated the average

        - Another analysis shows 8% for the 4 terminations in the block; going to be 4 – 8% for gigabit; gets worse as the size of the channel reduces
            - What is the sorting interval in this case?
            - Used 80 us
        - The Qualcomm proposal is for a 1.5 gigabit BW; the numbers seem to scale the same
- The penalty as you get smaller is pretty severe (30%)
    - For smaller BW, it does ***NOT*** make less sense to use a large number of profiles, but in this case you would reduce the number of profiles you use

Where does channel bonding blend in with this? Packet sorting goes into the MAC.

- Can review this in more detail at the interim
- Sorting will have to take into account channel info as well as profile info
- To maximize efficiency, you have to fill up the codeword, so both must be considered
- Will spend some time in Phoenix discussing this.

Gate frames: Scheduler issues a gateframe based on when it needs to go out. There is a 1 in 4 chance that it will hit the correct profile. What happens when a gateframe for one profile goes to another

- Slide 7 illustrates this
- 2 timelines: top is the MAC control client. Below is the multipoint transmission control entity. This is the one that does the reshuffling.
    - MAC control client wants a report for all CNUs within a polling interval; wants to scan them. This can be accomplished in a 1 ms polling interval
    - Multipoint transmission control reshuffles during this time period (MCS turnaround); smaller than polling interval (100 us)
    - The duration of the MCS turnaround time is the max delay
    - MCS turnaround time is the grouping time; and will delay by most 100 us
    - Based on the number of profiles and the likelihood of gate mismatch, we'd have more delay, wouldn't we
- Consider slide 8
    - Gate to gate interval doesn't change with sorting
    - Report frame increases the loop by 100 us; report limit is 1 ms, and this takes 10% of that limit
        - Therefore, adds to the delay in the loop
    - In this slide, it is represented as "first time delay"; contend that this happens more often? Yes.
        - Gate process receives primitive from MAC control client and uses it to decide the content of the gate and posts to send to the appropriate LLID. MAC control client that generates the messages decides when resources are assigned; while it may not be a one-time delay, but it can be minimized by tuning.

        - There has to be a correlation between the gate and the incoming report. If it's not there, it could be built.
            - To be able to build would be challenging
            - Assume that the primitive could have correlation between gate and profile
    - What about interleaving? Grouping operation comes for free.
        - That's why adding 100 us is painful
        - Assuming that the time from the report coming in and the gate going out is already 0
        - There is processing time at the OLT/CLT where an incoming report will get translated (maybe 20 us); could make this bigger
    - Does distance impact this? What about a node 20 km away?
        - Will have to compensate for round trip time; content of the gate and the time the gate is sent has to take this into account
        - If you add a longer walk time (up to 200 us), and then add this delay (100 us), then you have 300 us for a SG that is 20 km away.
        - Could have a bridge in between, rather than a repeater, but these slides were made agnostically to what is in the middle
        - Should we model this to understand impact on performance?
        - The OLT would know the distance and take this into account for the gate timing
            - This delay is independent of this feature

Do we agree that packet sorting is necessary?

- It's a feature that you could have; without, your FEC will be less efficient
- Based on traffic pattern, could go down to 70% efficiency
- This is not intended to mandate this implementation of the scheduler; you could do it with a single profile. This would always be an option.

Do we agree that 1 ms request time limit in the PHY is impacted by this? Also may be another symbol worth of delay.

- 1 ms only applies if you are trying to get the entire BW of the line to a single ONU
- Can't burst to a single device at line rate
- Limits the amount of data you can get from an ONU, but you aren't trying to get line rate out of a single ONU
- For any period over a ms, the line rate is less than a gigabit
    - No, burst rate is always at line rate. May not have a gig of data to send, but the burst is at line rate.

## MMP Efficiencies

Spreadsheet rolls up the efficiencies; will be shared on the reflector later today

To adjust the codeword, you can adjust the interval and worst case shortened codewords

The different tabs show examples for different parameters.

512 QAM used for LCD, based on analysis from Comcast and performance gains expected from LDPC(?)

We need to decide what all the inputs we want to have represented here; feedback welcome and the tool can be modified to reflect that.

The model reflects today's architecture and traffic patterns; if we move to all digital, then we could get more gain

- The tool should allow this to be modified and modeled

How do you model a single profile?

- Model as the LCD profile A 100%

## Addressing the "Additional Information Needed" to decide on MMCS

Simulation: New model reviewed today could help

Complexity: Impact from HW perspective, based on Huawei analysis, is less than 1%

Usefulness: What else do we need to show usefulness?

## New Straw Poll

Do you think that Multiple Modulation Profiles could be included as an optional feature in the EPoC Standard?

| Attendee | In Favor | Opposed | Undecided | Abstained |
|---|---|---|---|---|
| Alan Brown – Aurora | x | | | |
| Andrea Garavaglia – Qualcomm | x | | | |
| Bill Powell – ALU | x | | | |
| Christian Pietsch – Qualcomm | x | | | |
| Curtis Knittle – CableLabs | | x | | |
| Duane Remein – Huawei | x | | | |
| Ed Boyd – Broadcom | | x | | |
| Eugene Dai – Cox | | x | | |
| Joe Solomon – Comcast | x | | | |
| John Ulm – Motorola | x | | | |
| Jorge Salinger – Comcast | x | | | |
| Leo Montreuil – Broadcom | | x | | |
| Lup Ng - Cortina | | | x | |
| Marek Hajduczenia – ZTE | | x | | |
| Mark Laubach – Broadcom | | | x | |
| Michel Allard – Cogeco | | | | x |
| Mike Emmendorfer – Arris | x | | | |
| Nicola Varanese – Qualcomm | x | | | |
| Ony Anglade – Cox | | | | x |
| Peter Wolff – Titan Photonics | | | | x |
| Raanan Ivry – Wide Pass | x | | | |
| Saif Rahman – Comcast | x | | | |
| Steve Shellhammer – Qualcomm | x | | | |
| Tom Staniec – Cohere | x | | | |
| **Totals** | **14** | **5** | **2** | **3** |

This might be better phrased as whether you think it should be mandatory or if you think it could be made optional.

- Making it optional makes testing and interoperability more challenging

*After the meeting, Tom Staniec contacted Joe Solomon: he intended to vote in favor. The straw poll has been updated to reflect this.*