
802.3bs - 400 Gb/s Task Group Considerations for Test Fixture Specifications

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Purpose

- Considerations for 802.3bs 400 Gb/s test fixture specifications.

Background

- Review - 83E.2 CAUI-4 chip-to-module compliance point definitions
- Review – 802.3bj Clause 92 type 100GBASE-CR4 test fixture specifications.

802.3bm

- 802.3bm - Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables

- Annex 83E (normative) Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83E.2 CAUI-4 chip-to-module compliance point definitions

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 - The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at TP1a. The input of the HCB at TP4a is used to verify the host input compliance.

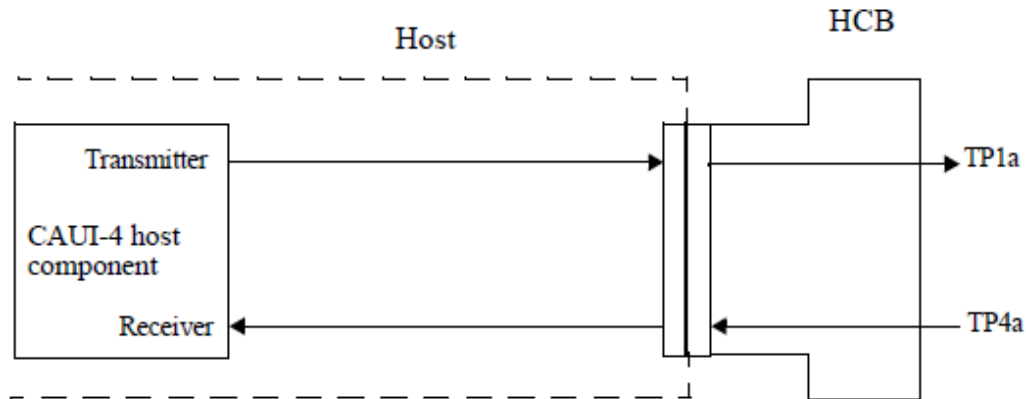


Figure 83E-4—Host CAUI-4 compliance points

83E.2 CAUI-4 chip-to-module compliance point definitions

- 83E.2 CAUI-4 chip-to-module compliance point definitions
 - The output of the Module Compliance Board (MCB) is used to verify the module electrical output signal at TP4. The input of the MCB at TP1 is used to verify the module input compliance.

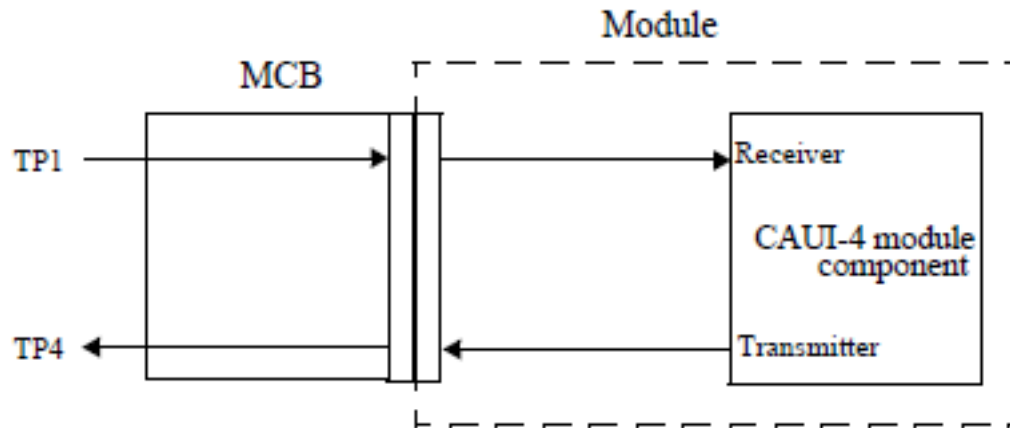


Figure 83E-5—Module CAUI-4 compliance points

83E.4.1 HCB/MCB characteristics

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- The HCB characteristics are described in 92.11.1 where the HCB performs the equivalent function as the TP2 or TP3 test fixture.
- The MCB characteristics are described in 92.11.2 where the MCB performs the equivalent functionality as the cable assembly test fixture.

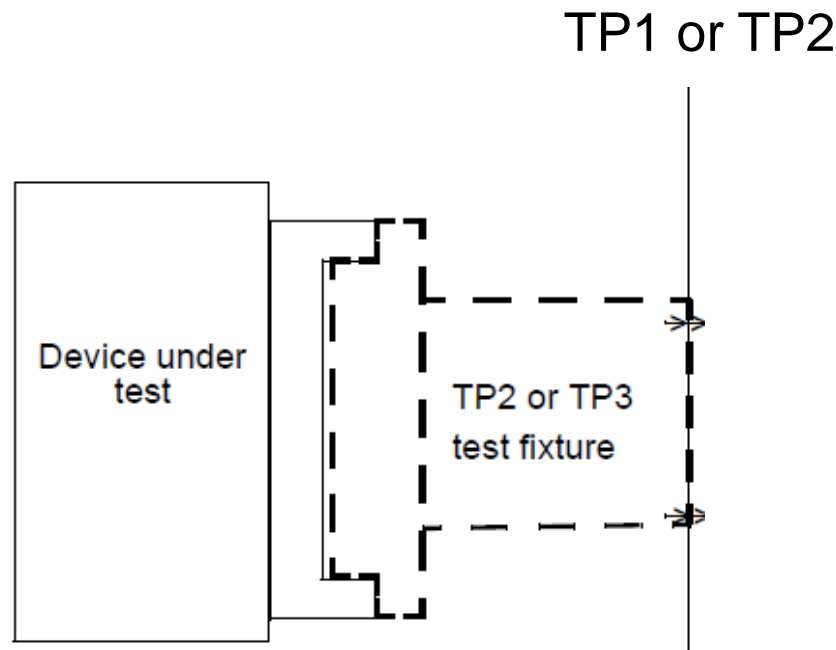
802.3bj Clause 92 Test Fixtures

92.11 Test Fixtures

92.11.1 TP2 or TP3 test fixtures (Host Compliance Boards)

92.11.1.1 Test fixture return loss (Mated)

92.11.1.2 Test fixture insertion loss (PCB reference insertion loss)



802.3bj Clause 92 – Test Fixtures

92.11.2 Cable assembly test fixture (Module Compliance Board)

>>>PCB reference insertion loss

92.11.3 Mated test fixtures

92.11.3.1 Mated test fixtures insertion loss

>>>Figure of merit insertion loss deviation FOMILD

92.11.3.2 Mated test fixtures return loss

92.11.3.3 Mated test fixtures common-mode conversion loss

92.11.3.4 Mated test fixtures common-mode return loss

92.11.3.5 Mated test fixtures common-mode to differential-mode return loss

92.11.3.6 Mated test fixtures integrated crosstalk noise

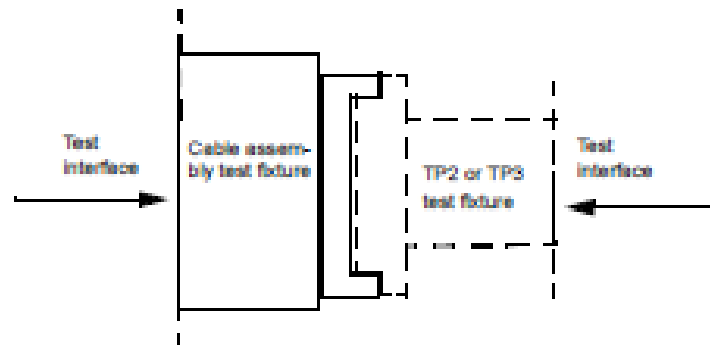


Figure 92-18—Mated test fixtures

IEEE P802.3bs Baseline Summary

Topic Matter	Motion	Reference Presentation
Architecture	Motion #3, Jan 15: Move to adopt slides 4 and 8 from dambrosia_3bs_02b_0115 as baseline architecture.	http://www.ieee802.org/3/bs/public/15_01/dambrosia_3bs_02b_0115.pdf
RS / CDMII	Motion #3, July 14: Move to adopt the baseline for the CDMII logical interface as shown in slide 5 of gustlin_3bs_03_0714.pdf.	http://www.ieee802.org/3/bs/public/14_07/gustlin_3bs_03_0714.pdf
FEC	Motion #3, Mar 15: Move to adopt RS(544,514,10) as the FEC in the 802.3bs 400GbE architecture	
Electrical Interfaces (C2C and C2M)	Motion #4, Sept 14: Move to adopt 16 x 25Gb/s and 8 x 50Gb/s as the basis for the lane rates for any optional C2C and C2M electrical interfaces	
C2C / C2M 25G Electrical	Motion #6, Sept 14: Move to adopt the P802.3bm C2C and C2M specifications with current values (except that the BER requirement is TBD) as a baseline draft for the 16 x 25Gb/s electrical interfaces	
C2C 50G Electrical	Motion #4, Mar 15: Move to adopt li_3bs_01a_0315.pdf as the baseline proposal for CDAUI-8 chip-to-chip electrical I/O interface except for the differential return losses (on slide 11) for the TX and the RX shall be TBD.	http://www.ieee802.org/3/bs/public/15_03/li_3bs_01a_0315.pdf
C2M 50G Electrical	Motion #5, Mar 15: Move to adopt brown_3bs_01a_0315.pdf as the baseline proposal for CDAUI-8 chip-to-module electrical I/O interface.	http://www.ieee802.org/3/bs/public/15_03/brown_3bs_01a_0315.pdf
C2C Informative Channel	Motion #6, Jan 15: Move to adopt the following equation as the informative insertion loss equation for CDAUI-8 chip-to-chip electrical I/O interface $IL \leq \begin{cases} 1.083 + 2.543\sqrt{f} + 0.761f & 0.01 \leq f \\ \leq 28.05\text{GHz} \end{cases} \text{ dB}$	
C2M Informative Channel	Motion #8, Jan 15: Move to adopt the following equation as the informative insertion loss equation for CDAUI-8 chip-to-module electrical I/O interface $IL \leq \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \\ \leq f \leq 28.05\text{GHz} \end{cases} \text{ dB}$	

Source: http://www.ieee802.org/3/bs/baseline_3bs_0315.pdf

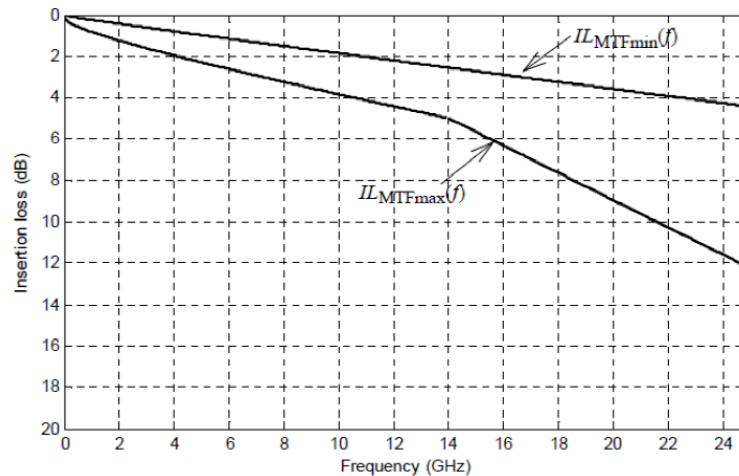
802.3bs C2M Electricals

- C2M 25G Electrical - 16 x 25Gb/s - 802.3bm C2M specifications with current values (except that the BER requirement is TBD) as a baseline draft.

- Includes compliance boards

- C2M 50G Electrical brown_3bs_01a_0315.pdf as the baseline proposal for CDAUI-8 chip-to-module electrical I/O

Compliance Boards



- Same as CR4 (Cl. 92)
 - No new compliance boards required

802.3bs test fixtures/compliance boards

- For 802.3bj, 802.3by and in general, test fixture PCB trace geometries (e.g., trace width, trace length, etc.) key element of achievable signal integrity (e.g., insertion loss, crosstalk, balance, etc.).
- Connector form factors (e.g., QSFP, SFP) constrain test fixture geometries and therefore SI but provide the basis for commonality in test fixture geometry.
- CR4 compliance boards SI related directly to QSFP form factor.

Recommendation

- Baseline to include informative annex detailing mechanical interface(s) that may be used at the compliance points.

