

## New comment (r01-141, not submitted. Clause 145.3.3.3.5 Page 191 line 48)

In the PD state machine in NOPOWER we have the assignment  $pse\_power\_level \leftarrow 8$  that may cause overload condition in the PSE whenever the assigned power is lower than the required power.

The overload condition happens when we force compliant PDs in NOPWER that do remember their assigned class (and their  $pse\_power\_level$ ) data to redefine their  $pse\_power\_level$  in NOPOWER to higher power level in NOPWER when PSE has no knowledge about it.

The assignment  $pse\_power\_level \leftarrow 8$  in NOPOWER looks redundant at least if the PD remembers its  $pse\_power\_level$  when PD input voltage is above  $VReset\_PD\_max$  (2.81V), or  $VReset\_th\_max$  (6.9V) which ensures sufficient voltage to PD to keep its memory.

Asking PD to assign  $pse\_power\_level \leftarrow 8$  in NOPOWER for  $VPD < VOff\_PD\_min$  without specifying that the lowest value for  $VPD < VOff\_PD\_min$  is  $VReset\_th\_max$  is the issue.

Example for the problem:

- PD requested class is 8 and the assigned class is 6.
- When transitioning from NOPWER back to POWERED, the PSE has still available power of 6 (that is why it has assigned class to 6) and now power level is 8.

The  $pse\_power\_level=8$  will cause the  $pse\_assign\_class$  in POWER\_DELAY to be:

$pse\_assign\_class = \min(pse\_power\_level, pd\_req\_class) = \min(8, 8) = 8$ .

This in turn will set  $pd\_max\_power$  in POWERED to be:

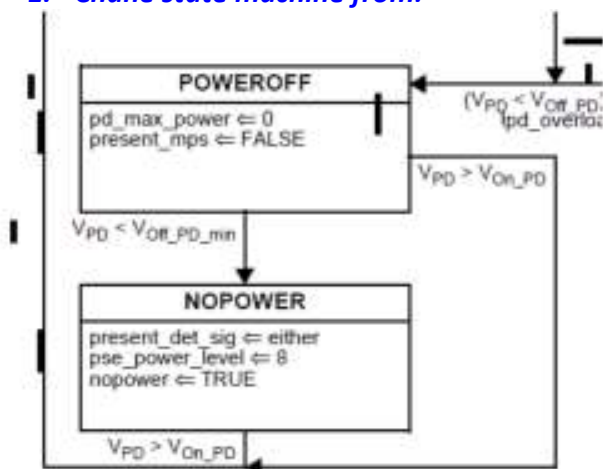
$pd\_max\_power \leftarrow \min(pse\_assigned\_class, pd\_req\_class) = \min(8, 8) = 8$  which is  $> pse\_available\ power = 6 \rightarrow$  PSE OVERLOAD condition.

This comment tries to minimize the exposure of a compliant PD that do remember its  $pse\_power\_level$  to be forced to reassign  $pse\_power\_level$  to 8 which will cause that PD to cause PSE overload which is uncompliant behavior after that PD that didn't go to IDLE was behave in a compliant way.

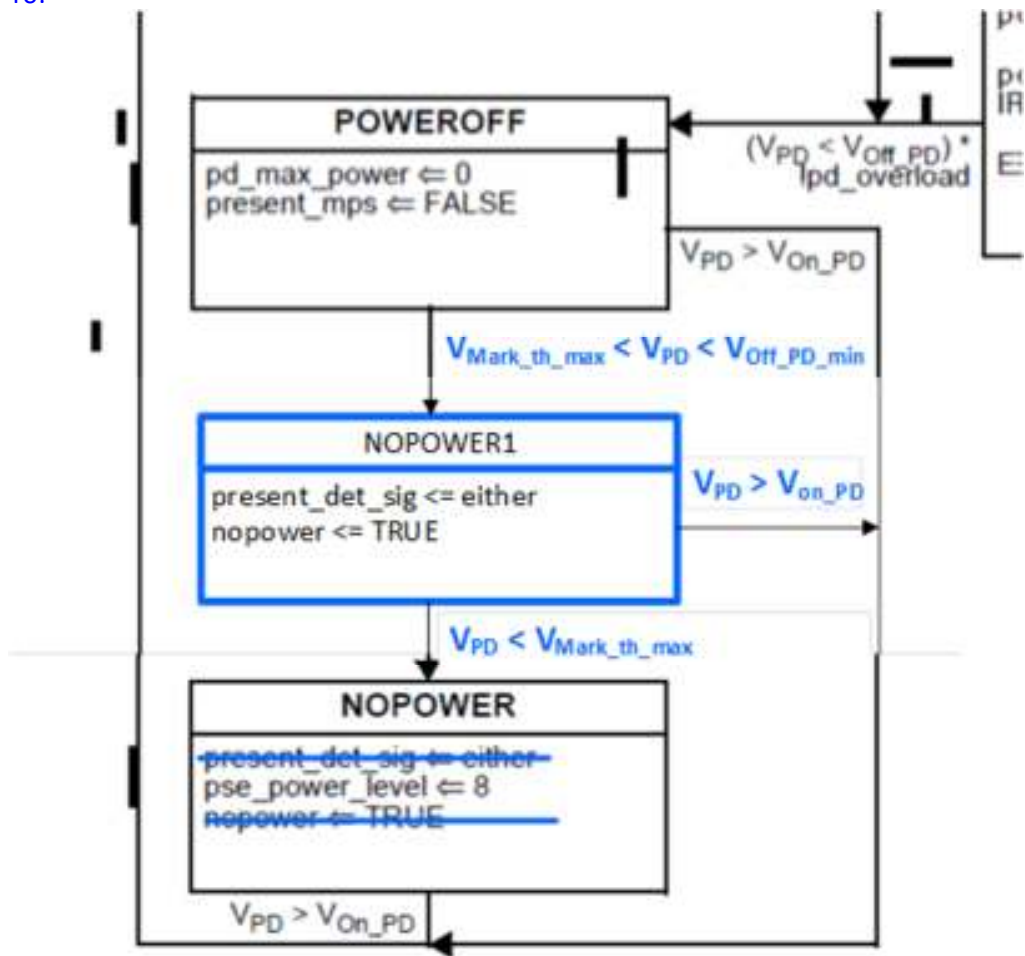
The proposed remedy is based on reducing the input voltage range in which we are forced to assign  $pse\_power\_level$  to 8 from:  $Vpd < VOff\_PD\_min$  to:  $Vmark\_th\_max < Vpd < VOff\_PD\_min$ .

**Proposed Remedy:**

### 1. Chane state machine from:



To:



2. Repeat the proposed changes for dual-signature PD.

*End of Remedy*

