



## PD PI & 57V

Rectifying the infamous “...*PD shall withstand any voltage from 0V to 57V at the PI indefinitely...*” text

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# Problem Statement

From 33.3.1 PD PI: *“The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.”*

- This text is vague, open to misinterpretation
  - The text is wrong because no PD can withstand 57V between pins within a twisted pair
  - We need to clarify this statement for Type 3/Type 4 (if not all) PDs
- ❖ D1.1 Comments 5, 145, & 189 all pertain to this sentence!

# Key Considerations

- Must exclude the application of 57V within a twisted pair for all Types
- Cannot place a new requirement, when compared with the most reasonably loose interpretation of the text, for Type 1/Type 2 PDs
- Requirements must be abundantly clear for Type 3 /Type 4 PDs

# Interpreting Legacy Text in Isolation

What is meant by “...at the PI...”?

- Can 57V be applied across ANY two twisted pairs or only two twisted pairs within the same Mode?
- Can 57V be applied across multiple twisted pairs simultaneously?

# Interpreting Legacy Text in Context

- The term “PI” is used extensively throughout 802.3-2012, yet it is rarely in reference to **all 4** twisted pairs
- Other text provides appears to provide guidance
  - From 33.2.3: “...PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously.”
  - From 33.3.1: “The PD shall be capable of accepting power on either of two sets of PI conductors.”
  - From 33.3.1: “PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard.”

# Reasonable Interpretation of Legacy Text

What is meant by “...at the PI...”?

- Can 57V be applied across ANY two twisted pairs or only two twisted pairs within the same Mode? **57V is only to be applied between two twisted pairs within the same Mode**
- Can 57V be applied across multiple twisted pairs simultaneously? **No, 57V is applied to each Mode individually**

# Suggested Remedy

- Modify the original text:
  - “~~The Type 1 and Type 2 PDs~~ shall withstand any voltage from 0 V to 57 V ~~at the P1~~ on either Mode A or Mode B indefinitely without permanent damage.”
- Consider supplementing with the following text:
  - “**Type 1 and Type 2** PDs **should** withstand any voltage from 0 V to 57 V **on any 2 sets of twisted pairs, in any polarity combination**, indefinitely without permanent damage.
- Add clear requirement for new PDs:
  - **Type 3 and Type 4** PDs **shall** withstand any voltage from 0 V to 57 V **on any 2 sets of twisted pairs, in any polarity combination**, indefinitely without permanent damage.”