



# Connection Check & Detection Sequencing & Timing

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# Background

- Many implementation details of Connection Check (CC) have been left to the reader
- Provides implementation flexibility – a noble goal
- However, flexibility burdens the standard in other ways (e.g. state diagram), and potentially leads to poor implementations
- Goals:
  - Provide rationale behind comments 176 & 178
  - Generate discussion within the Task Force on how best to balance flexibility and complexity, building up to new baseline text and state diagram for September

# CC & Detection Sequencing

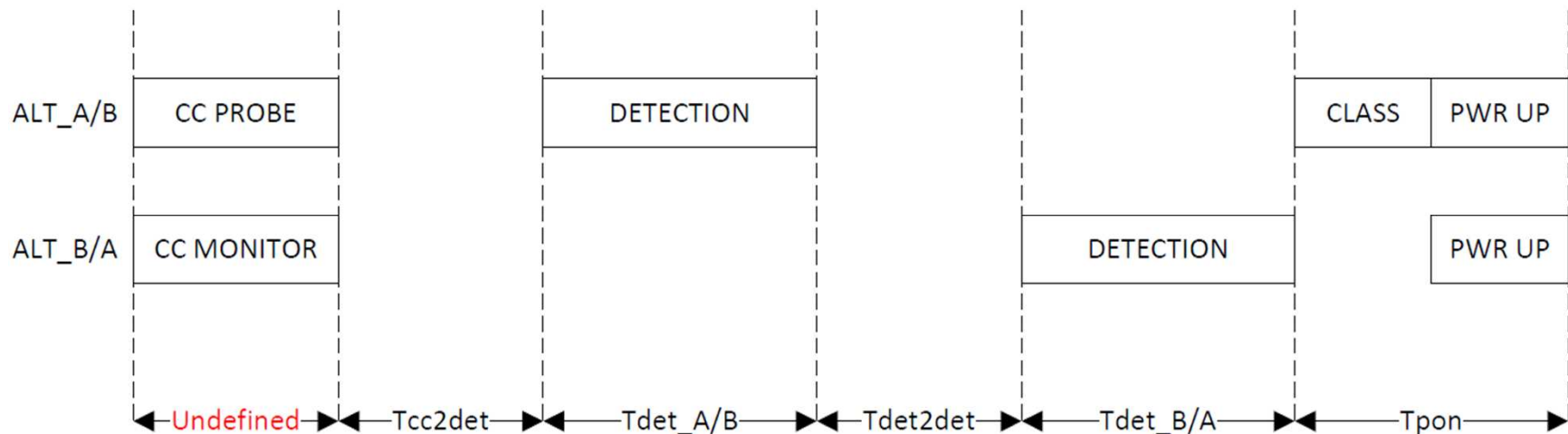
- Currently, there are **4** permitted sequences for CC and detection
  - 1) CC → detection
  - 2) Detection ALT\_A/B → CC → detection ALT\_B/A
  - 3) Detection → CC
  - 4) Simultaneous\*

\*Not covered since timing is straightforward – CC fits within Tdet, with or without parallel detection

# Sequence 1:

CC → Detection

## CC → DET (SS PD, D1.1)



- Duration of CC has not been specified, and it seemingly need not be
- However, a cable-plug mid-CC could possibly fool some implementations...

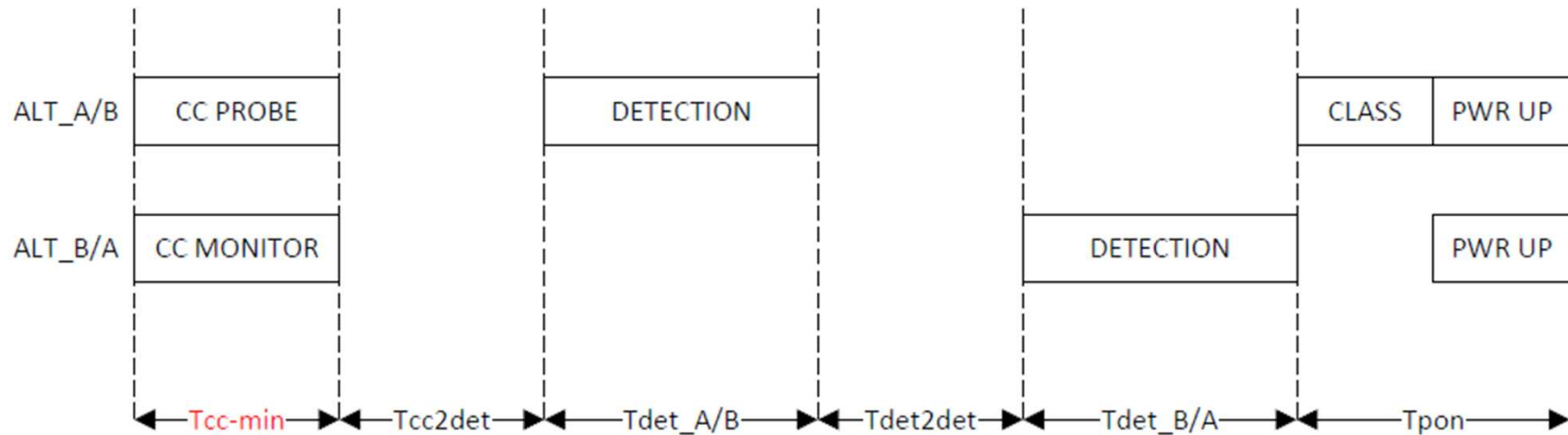
# Theoretical Mid-CC Cable-plug Example

- In reality, the RJ45 pins will mate at different times
- Investigation of the upper bound of the delta underway, but on the order of milliseconds seems reasonable
- One implementation-specific, problematic sequence:
  - 1) ALT\_A connects
  - 2) CC probes ALT\_A
  - 3) CC determines ALT\_A is not open circuit
  - 4) CC probes ALT\_B
  - 5) CC sees that probing ALT\_B has no bearing on ALT\_A
  - 6) PSE transitions to Detection as ALT\_B connects
  - 7) Detection returns “valid\_AB”
  - 8) PSE wrongly concludes DS (2 pairsets can meet Tpon independently)

# Mid-CC Cable-plug Prevention

- May be a rare occurrence, but the intermittence makes it challenging to troubleshoot and may be perceived as an interop issue
- So, some options for prevention:
  - 1) Require a detection prior to CC (i.e. outlaw this seq.)
  - 2) Define CC mechanism to the extent that any implementation will not be susceptible to a cable-plug
  - 3) Specify a minimum CC timing parameter (Tcc-min) – with informative text or annex explaining its existence – that exceeds the worst-case cable-plug mating delta

## CC → DET (SS PD, Option 3)



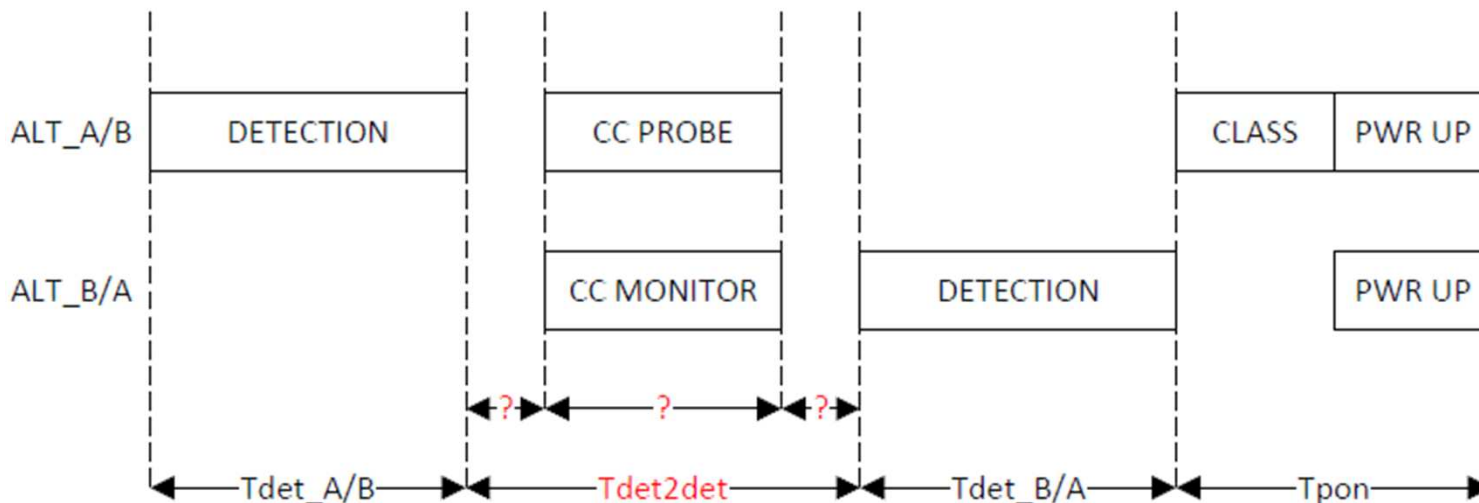
- Assuming Tcc-min can be specified with confidence, this sequence remains viable and most of the implementation details are left to the reader



# Sequence 2:

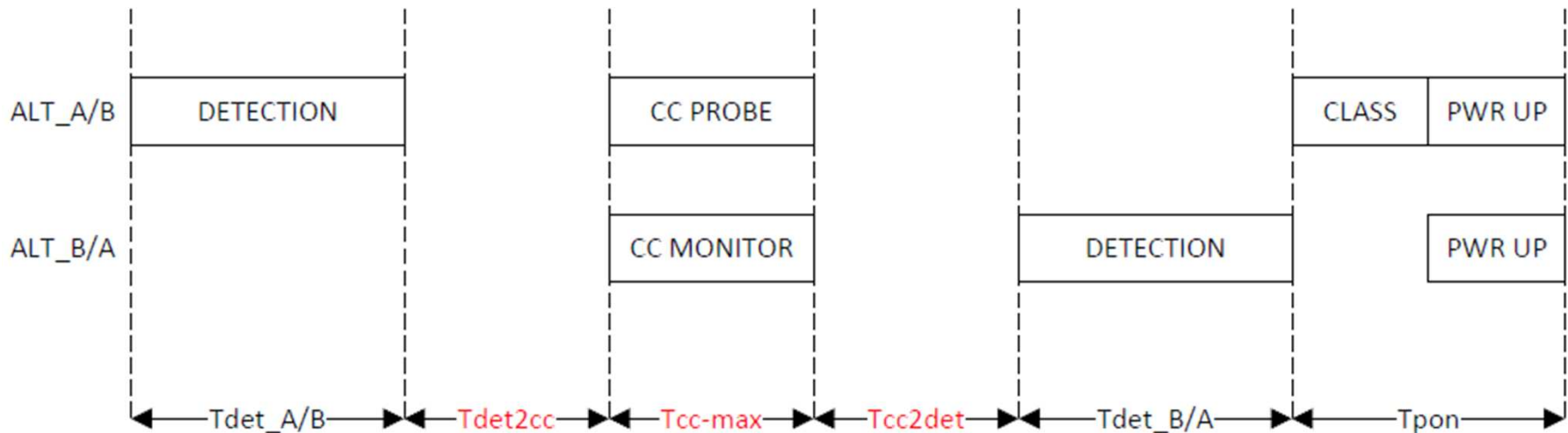
Detection ALT\_A/B → CC → Detection ALT\_B/A

## DET → CC → DET (SS PD)



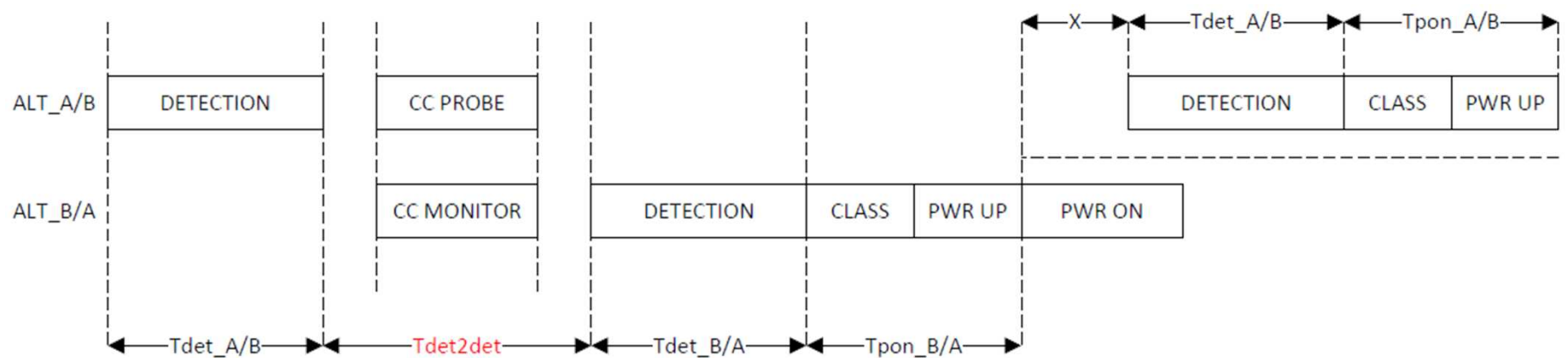
- CC timing for this sequence is more stringent than for Sequence 1, but this sequence is inherently impervious to cable-plug
- At the expense of further complexity, other timing parameters can be defined to potentially make this sequence more attractive

## DET → CC → DET (SS PD, Relaxed Timing)



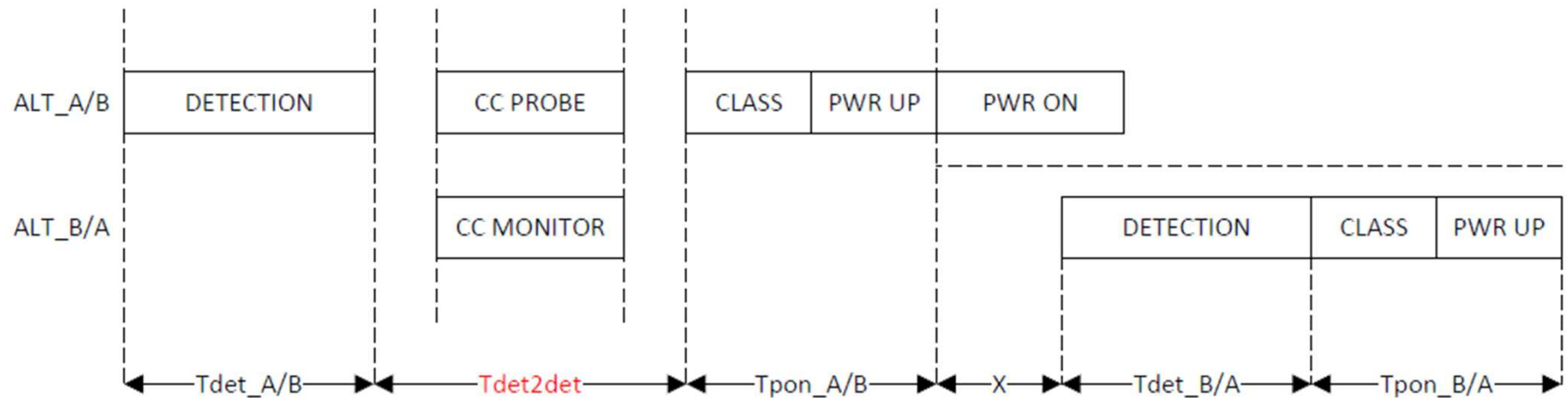
- Tcc2det exists, and Tcc-min (not necessarily applicable) can be paired with a max value, Tcc-max = 400ms
- Tdet2cc = Tcc2det = 400ms
- Safely transition to Class and Power Up with increased timing budget, but worth the added complexity?

## DET → CC → DET (DS PD, Ex. 1)



- D1.1 states that Tdet2det “Applies only when connected to a single-signature PD.”
- For this sequence to support DS, Tdet2det must be applicable

## DET → CC → DET (DS PD, Ex. 2)

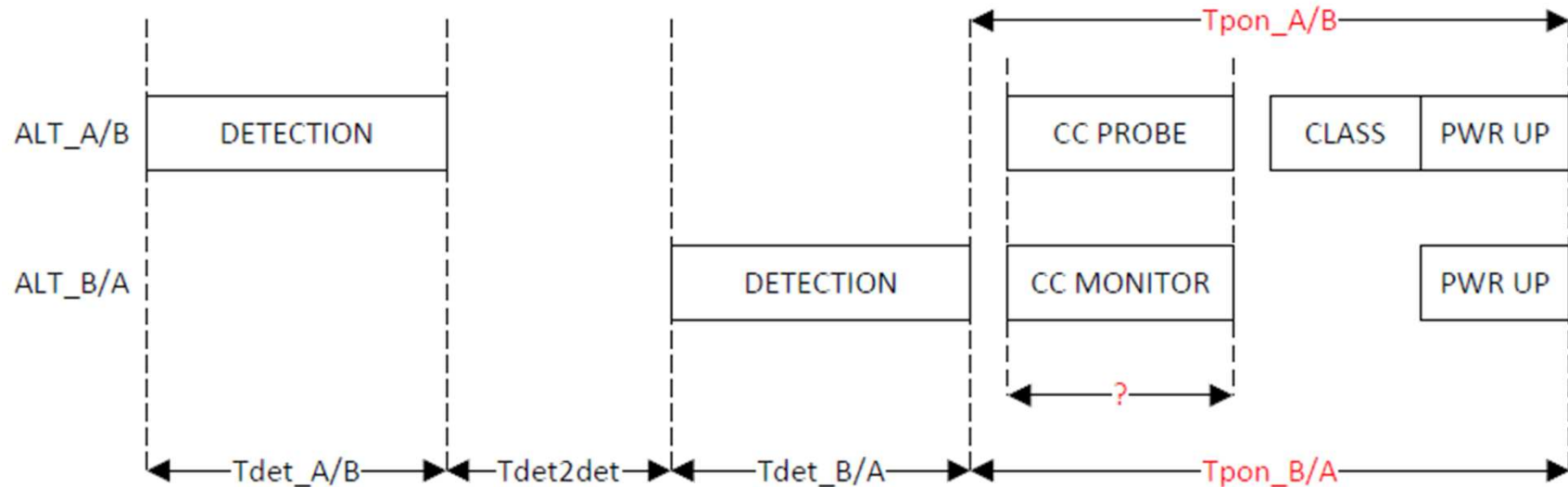


- $T_{det2det}$  is the right value, but it looks wrong in name
- Do we modify the definition of  $T_{det2det}$  or add a new parameter ( $T_{cc2cls}$ ?) to legitimize this sequence?

# Sequence 3:

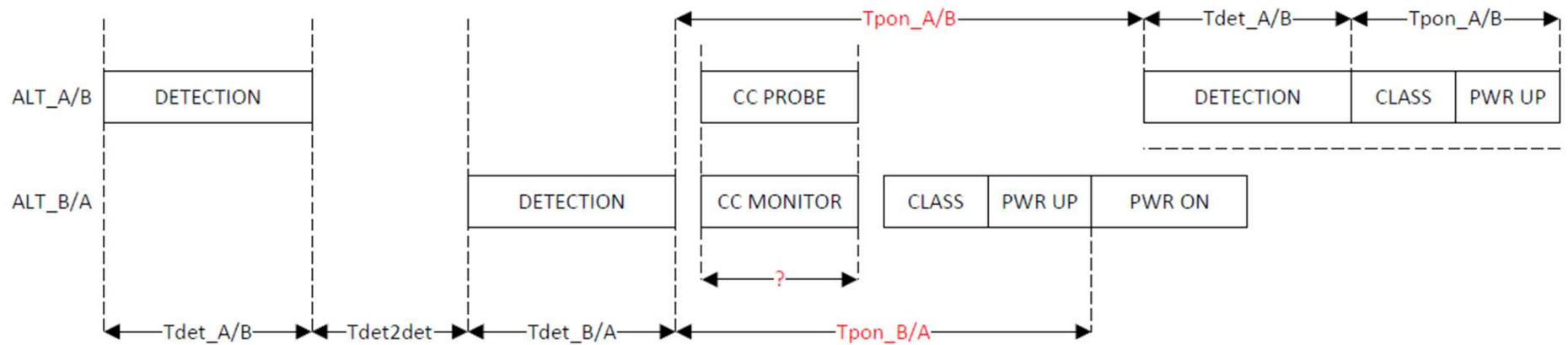
Detection → CC

## DET → CC (SS PD)



- Tightest timing because CC must be wedged into  $T_{pon}$  per D1.1
- Assuming timing can be met, this sequence appears feasible for SS

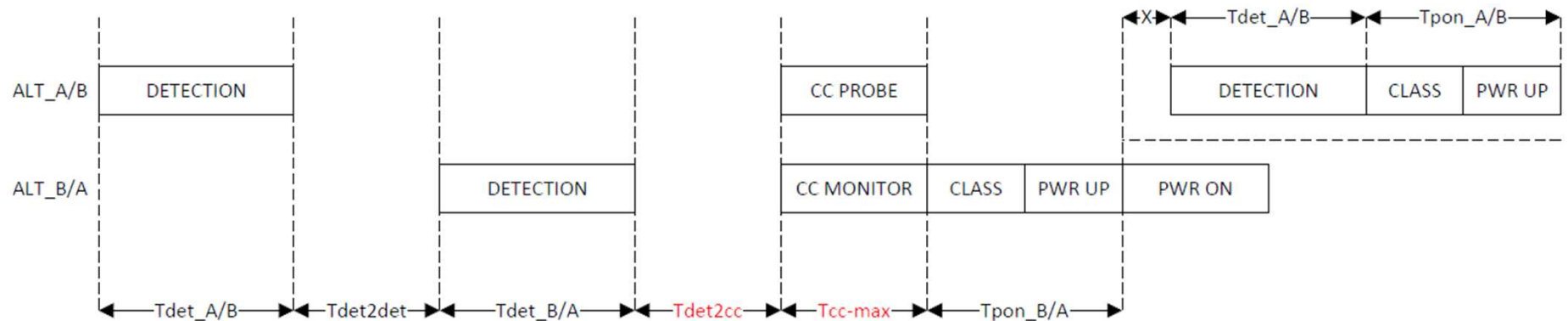
## DET → CC (Type 1/Type 2 DS PD)



- Potential Problem: Tpon must be started on both pairsets before DS identified
  - CC, Class, Power Up, and margin to Power On must fall within Tpon
  - Tpon bridges to a re-Detection instead of Power On for 1 pairset



# DET → CC (Type 1/Type 2 DS PD w/ Fix?)



- $T_{cc\_min}$  (not necessarily applicable) can be paired with a max value,  $T_{cc\_max} = 400ms$
- $T_{det2cc} = T_{cc2det} = 400ms$
- Safely transition to Class and Power Up with increased timing budget and no unnatural  $T_{pon}$  bridge to re-Detection, but worth the added complexity?

# D1.1 Comments

## CC & State Diagram

# Comment #176

CI 33	SC 33.2.4.3	P 34	L 29	# 176
Walker, Dylan		Cisco		

*Comment Type*    **TR**    *Comment Status*    **X**

To allow for PSEs that perform connection check before, during, between, or after detection, a new constant is needed to define the disparate pathways these PSEs take through the state diagram and their associated timing requirements.

## *Suggested Remedy*

Add constant "PSE\_CC\_DET\_SEQ" as follows:

### **PSE\_CC\_DET\_SEQ**

A constant indicating the sequence in which the PSE performs connection check and detection.

- Values:
- 1: Connection check and detection performed simultaneously
  - 2: Connection check performed prior to detection
  - 3: Connection check performed between detections
  - 4: Connection check performed after detection

# Comment #178

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CI 33	SC 33.2.5.0a	P 53	L 34	# 178
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Walker, Dylan

Cisco

*Comment Type*    **TR**    *Comment Status*    **X**

In Table 33-3a, under Additional Information for Item 2, it's stated that "Applies only when connected to a single-signature PD."

This may not be true if we allow connection check to occur between the 2 detections and don't want to create new timing parameters.

*SuggestedRemedy*

Presentation forthcoming to cover this and other aspects of connection check.

# References

# References

- [http://www.ieee802.org/3/bt/public/jun15/abramson\\_01bt\\_0615.pdf](http://www.ieee802.org/3/bt/public/jun15/abramson_01bt_0615.pdf)
- [http://www.ieee802.org/3/bt/public/sep14/dwelley\\_01\\_0914.pdf](http://www.ieee802.org/3/bt/public/sep14/dwelley_01_0914.pdf)