

MPS Unbalance v140

Lennart Yseboodt, Dave van Goor, Matthias Wendt

Philips Research

March 5, 2015

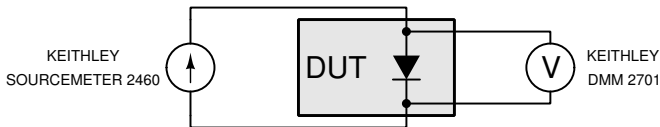
Overview

- ▶ Explore effect of diode forward voltage unbalance at low currents
- ▶ Temperature effect on diodes
- ▶ End to end MPS current unbalance
- ▶ Consequences for MPS design
- ▶ Proposal for MPS requirements

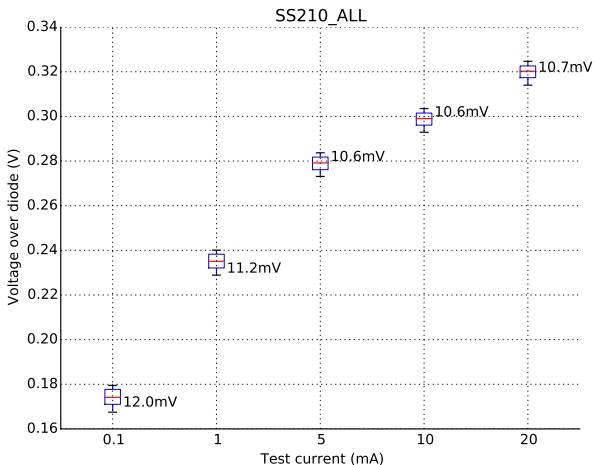
Measurement method

This presentation will explore measured difference in diode voltage over a number of different diodes at low current.

- ▶ Test currents: 100 μ A, 1 mA, 5 mA, 10 mA, 20 mA
- ▶ Diodes: MBRM1H100, MBRM2H100, MBRS2H100, MBRS1100, MBRS1100T, MURS110, MURS210, NTSS2100ET1, NTSS2100T1, SS210, VSSA210E361T
- ▶ DUT at stable room temperature
- ▶ Total 720 measured diodes

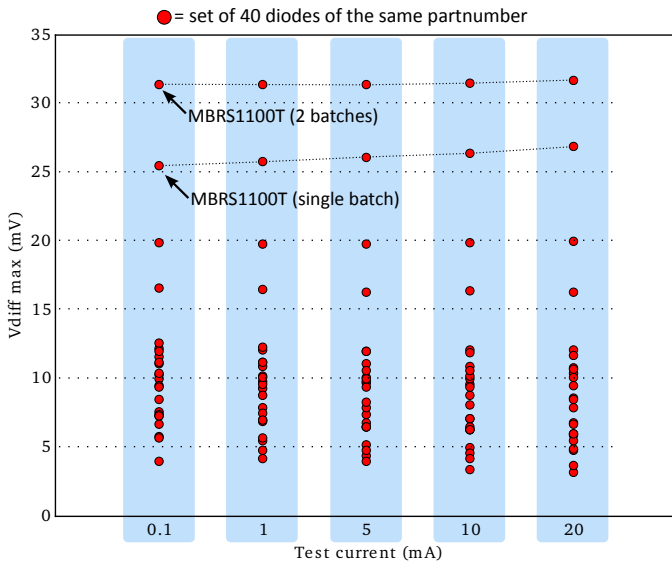


Example results



V_{diff} = highest measured V_D - lowest measured V_D at test current.

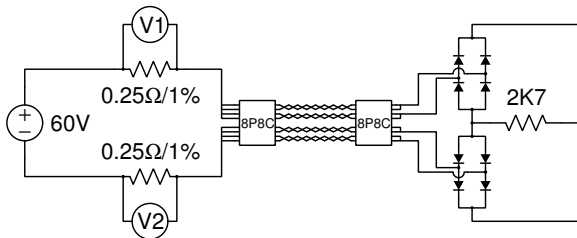
Vdiff overview



Conclusion Vdiff measurement

- ▶ Results match with [darshan_02_0115.pdf](#)
- ▶ In the current range 100 μ A to 20 mA the diode voltage difference remains constant, but absolute diode voltage goes up with current
- ▶ Of all measured diodes, the maximum sample to sample difference (for the same partnumber) is 32 mV
- ▶ Comparing a batch of diodes, purchased from 1 reel, to a combination of two batches (different time, different reel) increases the maximum diode voltage different by 6 mV
- ▶ Silicon or Schottky diodes exhibit the same amount of maximum voltage difference
- ▶ ... however, this is all measured at a stable constant temperature.

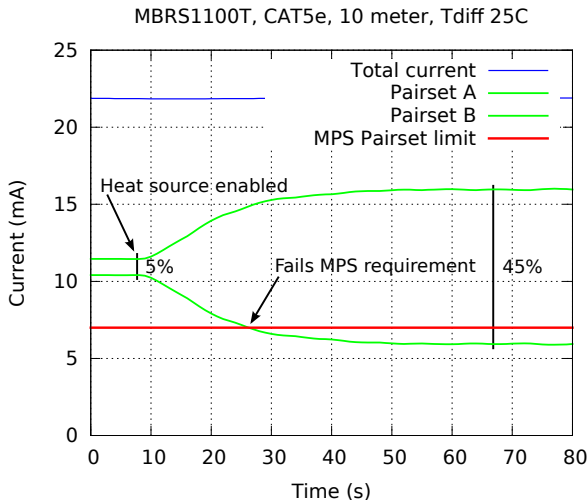
End to end MPS unbalance



- ▶ Measured pair-set current over 0.25 Ω precision resistor (resistors matched better than 1%).
- ▶ Tested with various cable lengths (1 m, 10 m)
- ▶ Diode: MBR51100T & SS210
- ▶ Test to fail: introduce temperature difference → can we fail MPS ?

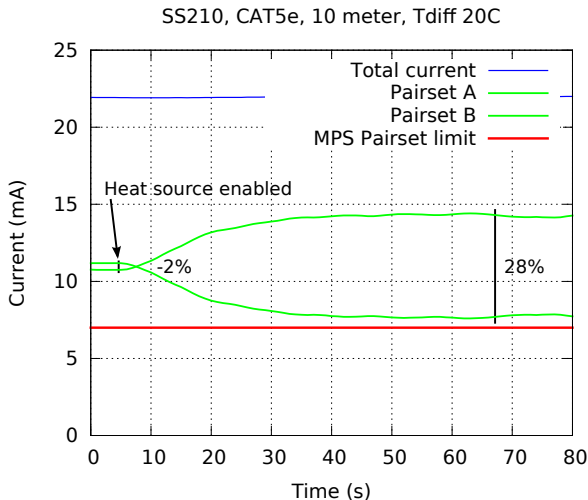
Measurement results 1

- ▶ I_{Port} : 22 mA
- ▶ 10 meter CAT5e
- ▶ Diode: MBRS1100T
- ▶ $V_{\text{diff(max)}}$: 34 mV
- ▶ Applied 25 °C difference between diode bridges (43 °C / 68 °C)
- ▶ Current unbalance 5% → 45%



Measurement results 2

- ▶ I_{Port} : 22 mA
- ▶ 10 meter CAT5e
- ▶ Diode: SS210
- ▶ $V_{diff(max)}$: 10 mV
- ▶ Applied 20 °C difference between diode bridges (40 °C / 60 °C)
- ▶ Current unbalance -2% → 28%



Conclusion system measurements

System end to end low current unbalance measurements show:

- ▶ Initial (room-temperature) low current unbalance looks good
- ▶ Temperature difference between diodes creates large unbalance
- ▶ Temperature effect is potentially far greater than intrinsic V_{diff} .
Temperature coefficient $-2.0 \text{ mV}/^{\circ}\text{C}$
- ▶ Maximum V_{diff} is not a typically specified parameter in datasheets
- ▶ Other effects, like aging, are hard to predict

PDs will need a carefully designed input stage to control unbalance if a low power mode is needed. Use of diode rectifiers is probably not recommended if the PD must ensure a per pairset MPS.

MPS proposal

$I_{\text{Hold 2P}}$	Current the PSE must see on powered pairset(s) to consider MPS OK.
$I_{\text{Hold 4P}}$	Total current the PSE must see on both pairsets to consider MPS OK.
MPS both	PSE requires MPS to be met on both pairsets.
Sum/Max	Allowed MPS methods: sum-pairset and max-pairset
$I_{\text{Port_MPS}/2P}$	Minimum current the PD must guarantee per powered pairset
$I_{\text{Port_MPS}}$	Minimum total current the PD must guarantee
Timing	PSE or PD should follow the 'old' or 'new' timing

PSE	PD	PSE Requirements				PD Requirements		
		$I_{\text{Hold 2P}}$	$I_{\text{Hold 4P}}$	Timing	Sum/Max	$I_{\text{Port_MPS}/2P}$	$I_{\text{Port_MPS}}$	Timing
Type 1,2	Type 1,2	5-10 mA	-	Old	-	-	10 mA	Old
	Type 3,4 Class ≤ 4	5-10 mA	-	Old	-	-	10 mA	Old
	Type 3,4 Class ≥ 5	5-10 mA	-	Old	-	-	10 mA	Old
	Type 3,4 2-channel	5-10 mA	-	Old	-	-	10 mA	Old
Type 3,4	Type 1,2	-	5-10 mA	New	Yes	-	10 mA	Old
	Type 3,4 Class ≤ 4	-	5-10 mA	New	Yes	-	10 mA	New
	Type 3,4 Class ≥ 5	2-7 mA	-	New	Yes	7 mA	-	New
	Type 3,4 2-channel	2-7 mA	-	New	No	7 mA	-	New

Type 3/4 PSE MPS Rules

▶ PD Type 1, 2, 3[\leq Class 4]

- ▶ I_{Hold} = 5-10 mA, total current (no balance requirement)
- ▶ Support new MPS timings (6 ms / 354 ms)
- ▶ MPS methods: per-pairset, sum-pairset, max-pairset

▶ PD Type 3[\geq Class 5], Type 4

- ▶ I_{Hold} = 2-7 mA per pairset
- ▶ Support new MPS timings (6 ms / 354 ms)
- ▶ MPS methods: per-pairset, sum-pairset, max-pairset

▶ PD Dual channel

- ▶ I_{Hold} = 2-7 mA per pairset
- ▶ Support new MPS timings (6 ms / 354 ms)
- ▶ MPS methods: per-pairset, ~~sum-pairset, max-pairset~~

Type 3/4 PD MPS Rules

- ▶ **PSE Type 1, 2**

- ▶ $I_{\text{Port_MPS}} = 10 \text{ mA}$, total current (no balance requirement)
- ▶ Legacy timing: 75 ms / 250 ms

- ▶ **PSE Type 3[\leq Class 4]**

- ▶ $I_{\text{Port_MPS}} = 10 \text{ mA}$, total current (no balance requirement)
- ▶ New timing: 7 ms / 318 ms

- ▶ **PSE Type 3[\geq Class 5], Type 4**

- ▶ $I_{\text{Port_MPS}} = 7 \text{ mA}$, per pairset
- ▶ New timing: 7 ms / 318 ms

Balanced flexibility

The MPS rules in the previous slide are a balance between PSE and PD flexibility and allow a further reduction in standby power.

- ▶ Legacy Type 1/2 PDs cannot have any requirement imposed for unbalance at MPS currents.
- ▶ Since a PSE cannot distinguish the Type of a PD in classes 0-4, we can apply the legacy MPS rules (amplitude & balance) also to Type 3 PDs of class 0-4, without causing (extra) complications for the PSE.
- ▶ Type 3/4 single channel PDs in Class 5 or higher must present I_{Port_MPS} on both pair-sets.
- ▶ Type 3/4 PSEs may also look at the sum of currents or the highest current of both pairsets to consider MPS satisfied.
- ▶ Dual channel PDs must present I_{Port_MPS} on both pairsets

Conclusion

- ▶ Measurements of 720 diodes, 11 types, reveal $V_{diff(max)} < 35 \text{ mV}$
- ▶ Parallel diodes cannot be expected to have reliable current sharing behaviour at MPS level currents
- ▶ PDs should be able to implement diode rectifiers and support low standby
- ▶ This MPS proposal offers balanced design flexibility for PSE and PD
- ▶ Diode bridges are possible for Class 4 and below
- ▶ PDs without low power modes are not impacted by this unbalance issue

Propose for .bt group to adopt MPS rules in this presentation.



Diode equation

$$I = I_s \left(e^{\frac{qV}{nkT}} - 1 \right)$$

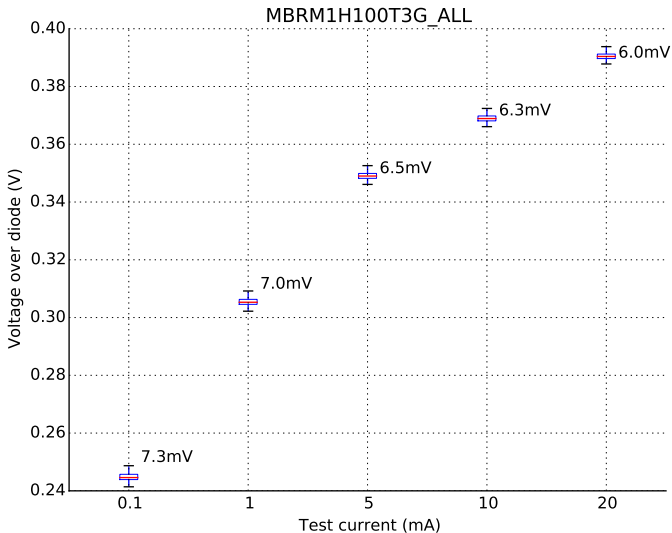
$$I_s = qA \frac{D n_i^2}{L N_D} = qA \frac{D}{L N_D} B T^3 \exp \left(-\frac{E_{G0}}{kT} \right)$$

Silicon diode voltage shifts by about $-2.5 \text{ mV}/^\circ\text{C}$

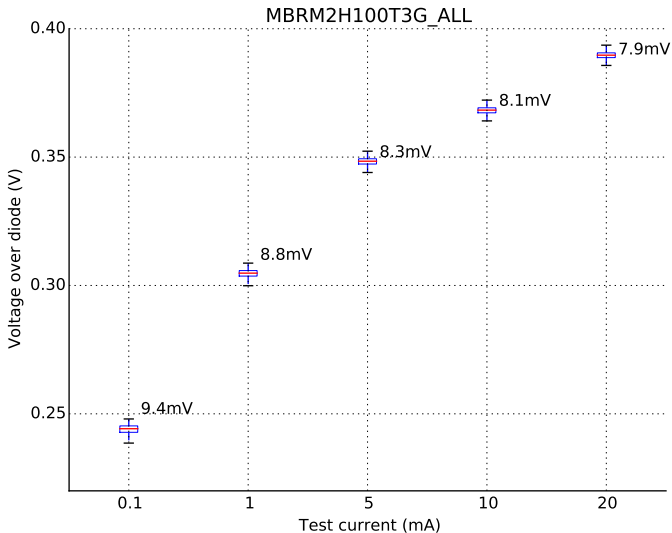
Schottky diode voltage shifts by about $-2.0 \text{ mV}/^\circ\text{C}$

Reference: <http://www.pveducation.org/pvcdrom/solar-cell-operation/effect-of-temperature>

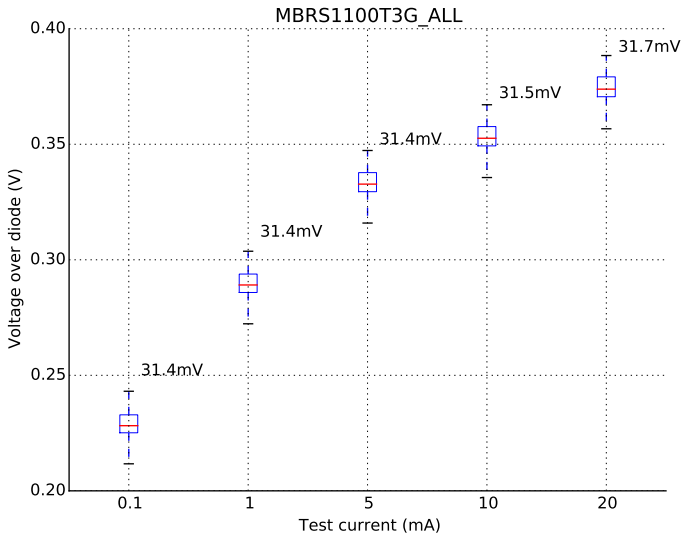
Diode measurement results: MBRM1H100T3GALL



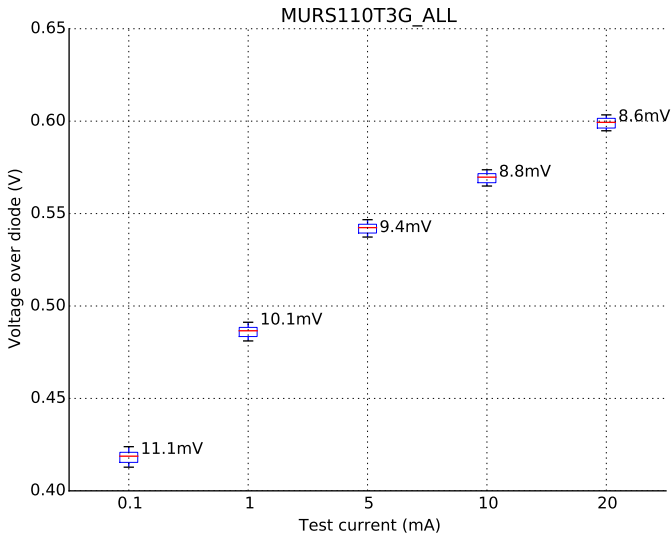
Diode measurement results: MBRM2H100T3GALL



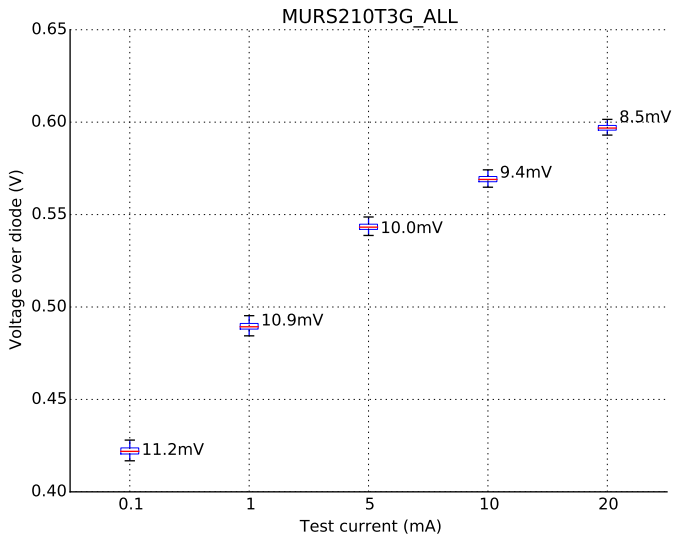
Diode measurement results: MBR1100T3GALL



Diode measurement results: MURS110T3GALL



Diode measurement results: MURS210T3GALL



Diode measurement results: SS210ALL

