FEC Proposal for NGEPON – update (rev 1a)

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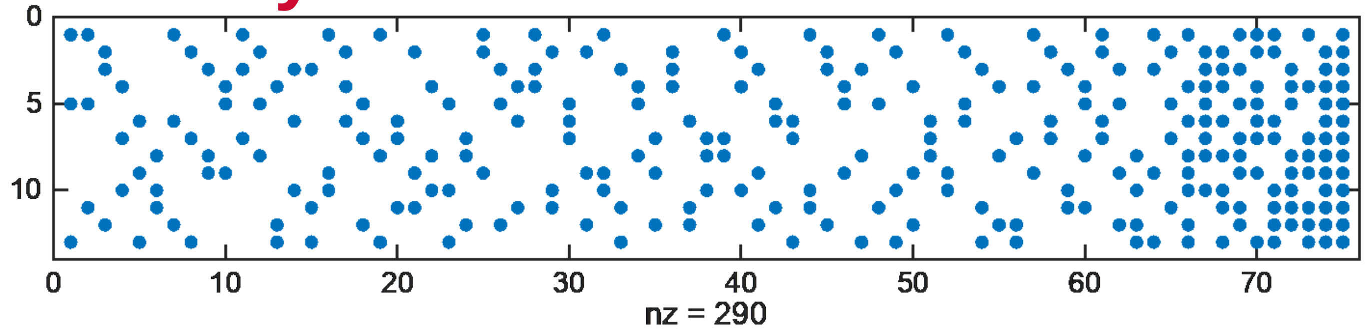
Introduction

- An LDPC(18493,15677) [11x74x256] 0.848 rate FEC code, code matrix, and interleaver was proposed at the May 2017 meeting
  - laubach_3ca_1_0517 with update laubach_3ca_4_0517
- This presentation introduces an updated “New” LDPC(18493,15677) [13x75x256] 0.848
  - Increased use of parity word puncturing for improved correction performance
    - Motivation from jinyinrong_3ca_2b_0717
  - Error floor below BER $1x10^{-12}$ (meets TF Objective)
  - Iterations capped at 15
- Author’s LDPC proposal is updated
  - Recommend code matrix and puncturing from this presentation
- AWGN and Gilbert burst error models are studied
  - Pre-coding and Gilbert burst study is still in progress as of 10/27/17.
- Impact of Omega256 structured and random interleaving is reviewed.

Proposed New Parity Check Matrix



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-1 -1 21 -1 -1 -1 174 -1 -1 -1 -1 -1 153 -1 -1 -1 -1 93 -1 -1 -1 -1 -1 239 -1 172 -1 -1 -1 -1 185 -1 -1 -1 183 -1 4 -1 -1 -1 117 -1 -1 -1 65 -1 -1 -1 -1 137 -1 -1 -1 -1 97 234 -1 -1 -1 -1 -1 98 0 -1 -1 185 -1 -1 8 -1 13 19 156 232 50
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Puncturing:

- 512 bits punctured
- Location from right side of the H matrix (two circulants with weight 12 and 13)

Parity Word Shortening:

- 195 bits shortened
- Location from the left side of the H matrix (the circulant with weight 3)

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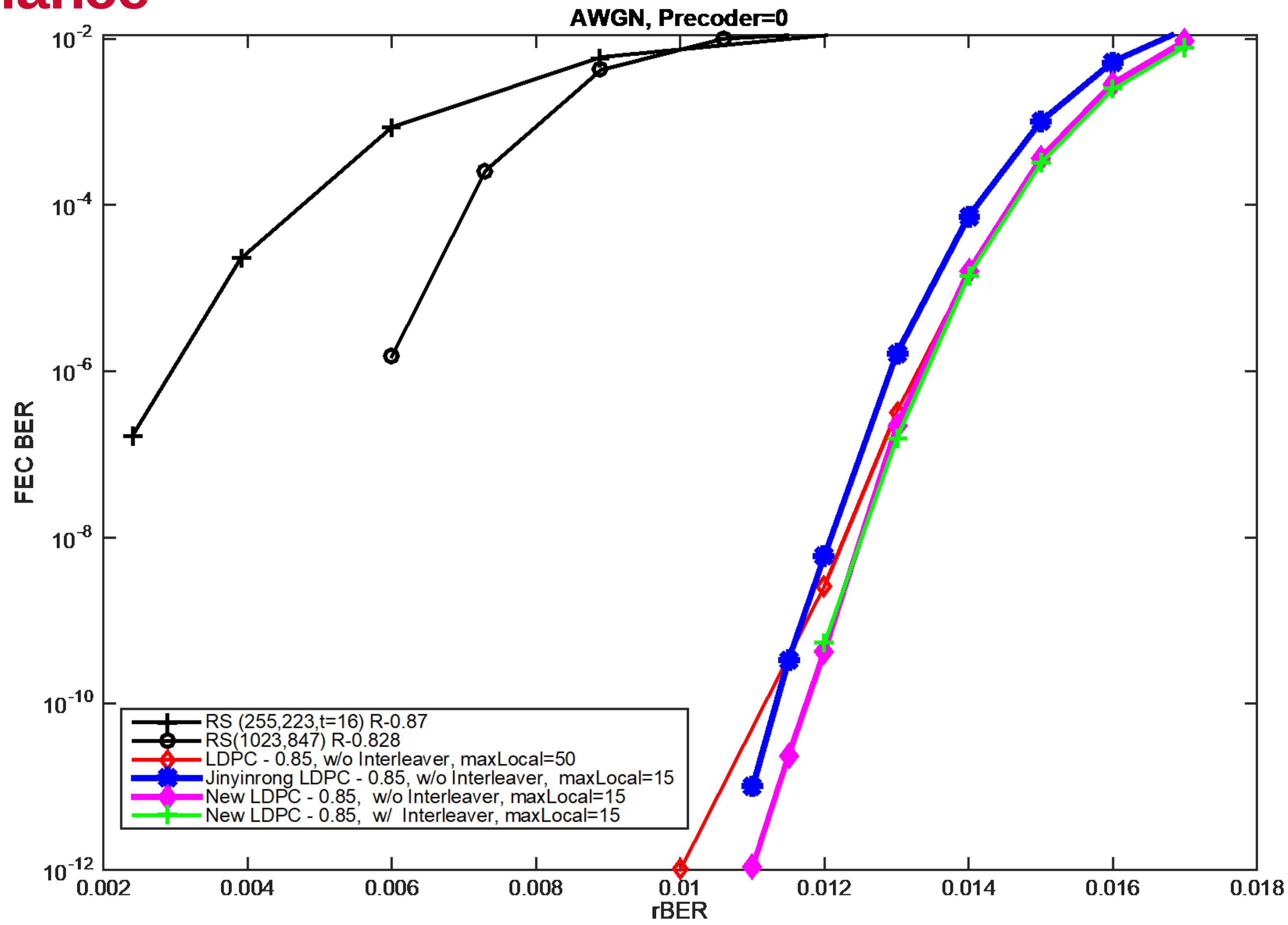
Use shortening to support handling of different burst lengths

- Upstream, set to zero for the bits corresponding to shortened locations during encoding. Encode normally for the full length of the code. Shortened bits are not transmitted.
- Downstream, set to maximum LLR at decoder input for shortening locations. Decode normally for the full length of the code.
- Decoding complexity/latency stays the same
- Shortening doesn’t degrade error floor performance. If the shortening locations are carefully chosen, shortening will improve error floor performance

AWGN Performance

Note: interleaver provides no additional performance gain for AWGN only model as expected.



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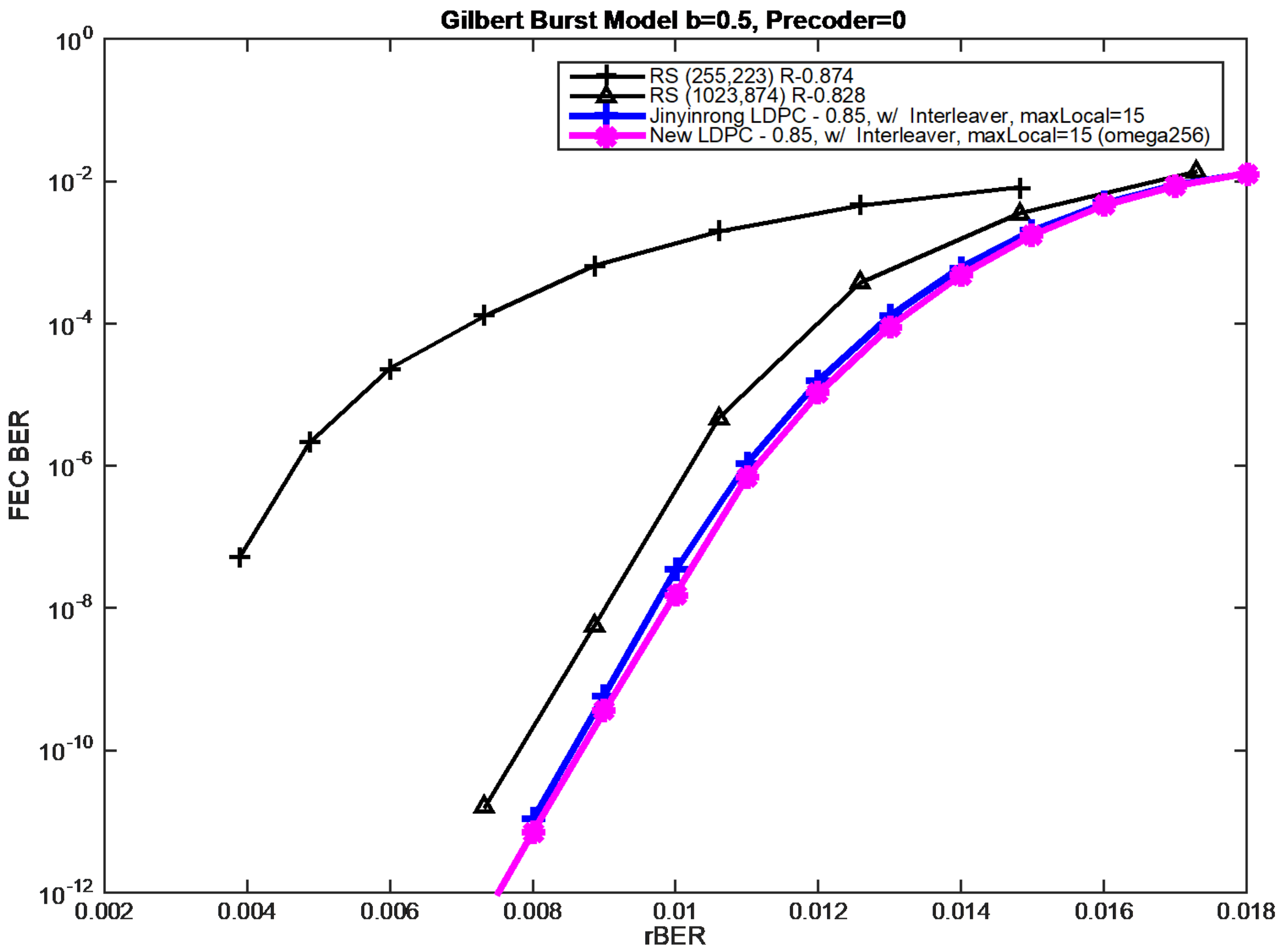
Gilbert burst error performance

Note 1: with “hardware friendly” local Omega256 interleaver presented in laubach_3ca_1_0517.

Note 2: original Omega256 interleaver was optimized for use with precoding. No precoding is used in this presentations studies.



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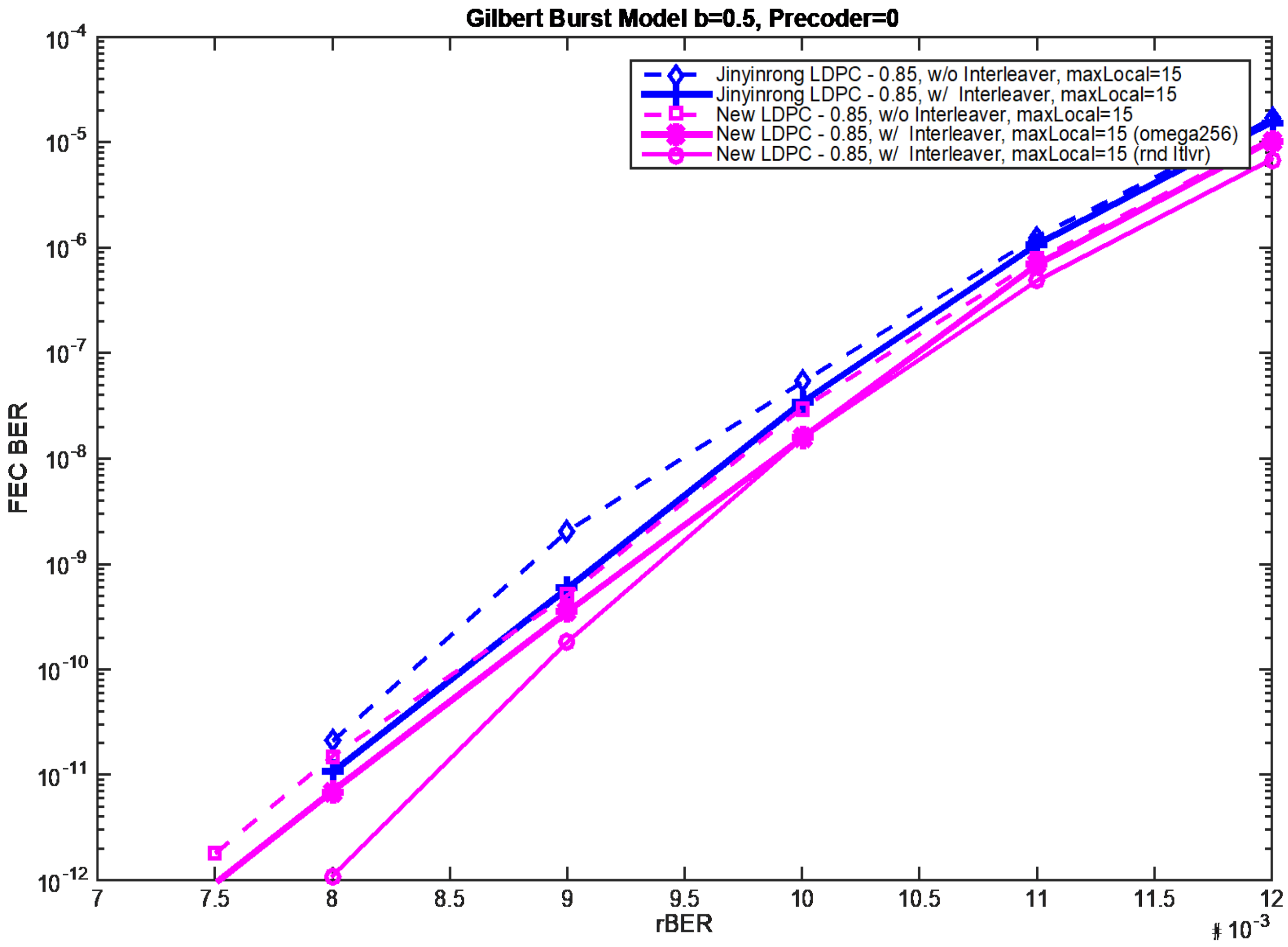
Gilbert burst error performance “zoom in”

Comparison with & without interleaver.

“Omega256” is a local interleaver sized for spanning a single circulant of 256 bits.

“Random” intereaver spans the entire codeword.

Observation: random interleaver provides better performance but at increased complexity.



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FEC Code Gains, sizes, and latencies

	Length	Rate	Non-Zero Blocks	NECG [1] (dB) (optical gain)		M Gates Encoder + Decoder (approximately)	Latency [3] (μsec) (includes single buffer)	Reference
				AWGN	Gilbert Burst [2]			
LDPC	(18493,15677) [11x74x256] [7]	0.848	382	2.46 (1.7-2.2)	1.85 (1.3-1.8)	1.65 to 1.8	E 2.77 + D 2.95 = 5.72 [4]	laubach_3ca_1_0517
	(18493,15677) [13x75x256]		290	2.6 (1.8-2.3)	1.76[5] (1.2-1.6) 1.87[6] (1.2-1.7)			This presentation.
	(18493,15677) [13x76x256] [8]		296	2.56 (1.8-2.3)	1.75 (1.2-1.8)	3.4	-na-	jinyinrong_3ca_2b_0717
RS	(1023, 847)	0.828	-na-	1.34 (0.94-1.2)	1.35 (0.95-1.2)	1.06	E+D: 0.77	

[1] Electrical gain over RS(255,223) of 7.1 dB. Optical gain is 0.7 to 0.9 * NECG

[2] Gilbert Burst (with interleaver, no precoding)

[3] Capped at 15 iterations

[4] Implementation dependent: LDPC encoding and decoding latency can be reduced with more parallel operations, with the cost of additional area; e.g. encoder could be reduced from 2.0 to 0.94 by adding more complex multipliers. In decoder latency could be reduced by lowering the iteration cap, however this needs further study.

[5] Hardware friendly interleaver

[6] Full random interleaver

[7] [11x74ex256] code gain first presented is based on 50 max iteration

[8] From our own simulation Jinyinrong code gain is 2.56 dB on AWGN and 1.75 dB on Gilbert with max 15 local, hardware friendly interleaver

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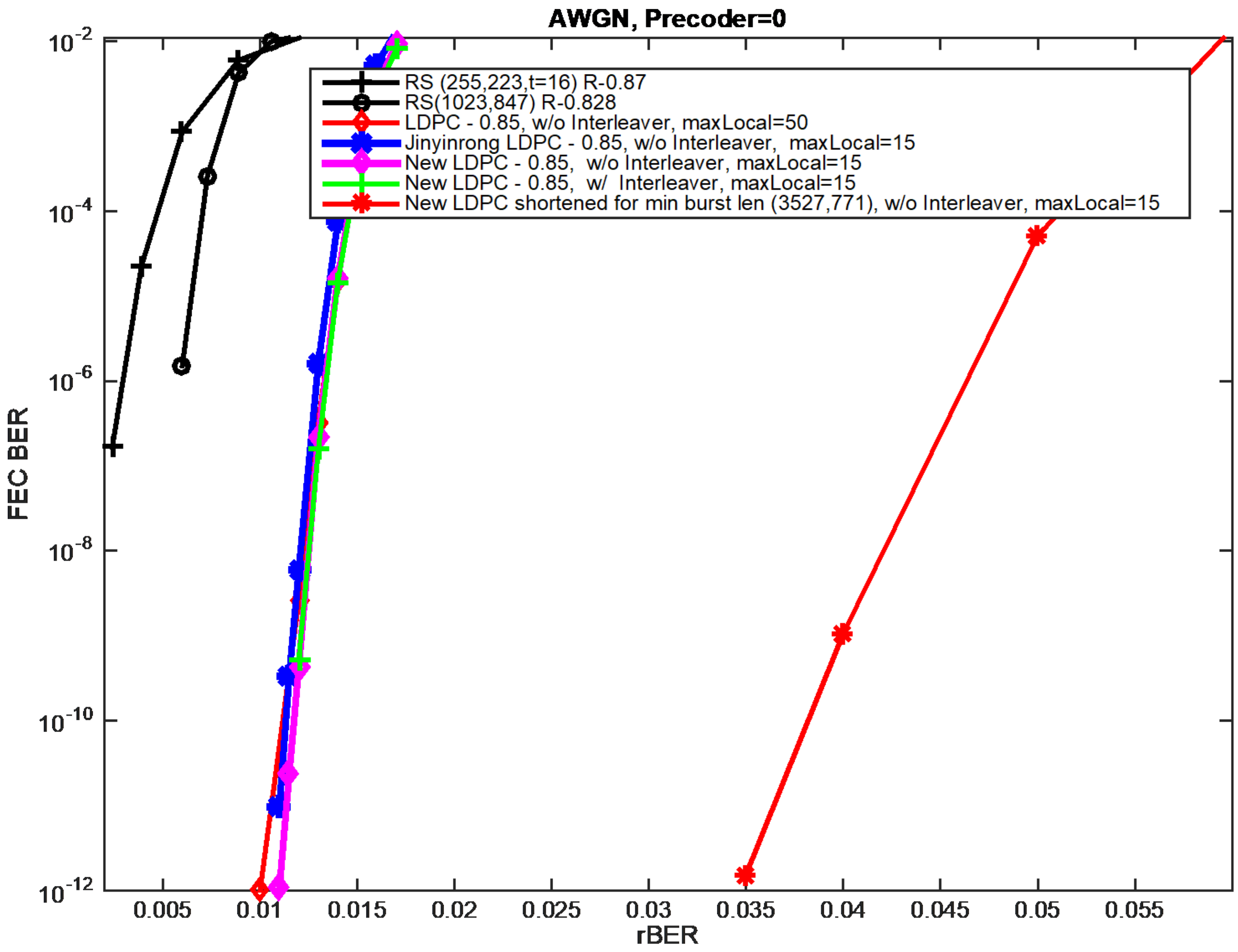
On Shortening methodology

New Slide

- Please refer to Glen Kramer's analysis presented in laubach_3ca_1_0317
- Conclusion
  - Only one code word size needed for upstream
  - Shorten information word only, parity word stays the same size
- For this graph, minimum information word size is:
  - 64 byte Ethernet frame + 8 byte EH in 3 * 257 bits = 771 bits (investigating line coding that has already be standardized in 25Gb/s Ethernet as a starting point)
- Observation
  - Gain increases
  - No error floor



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On processing latency

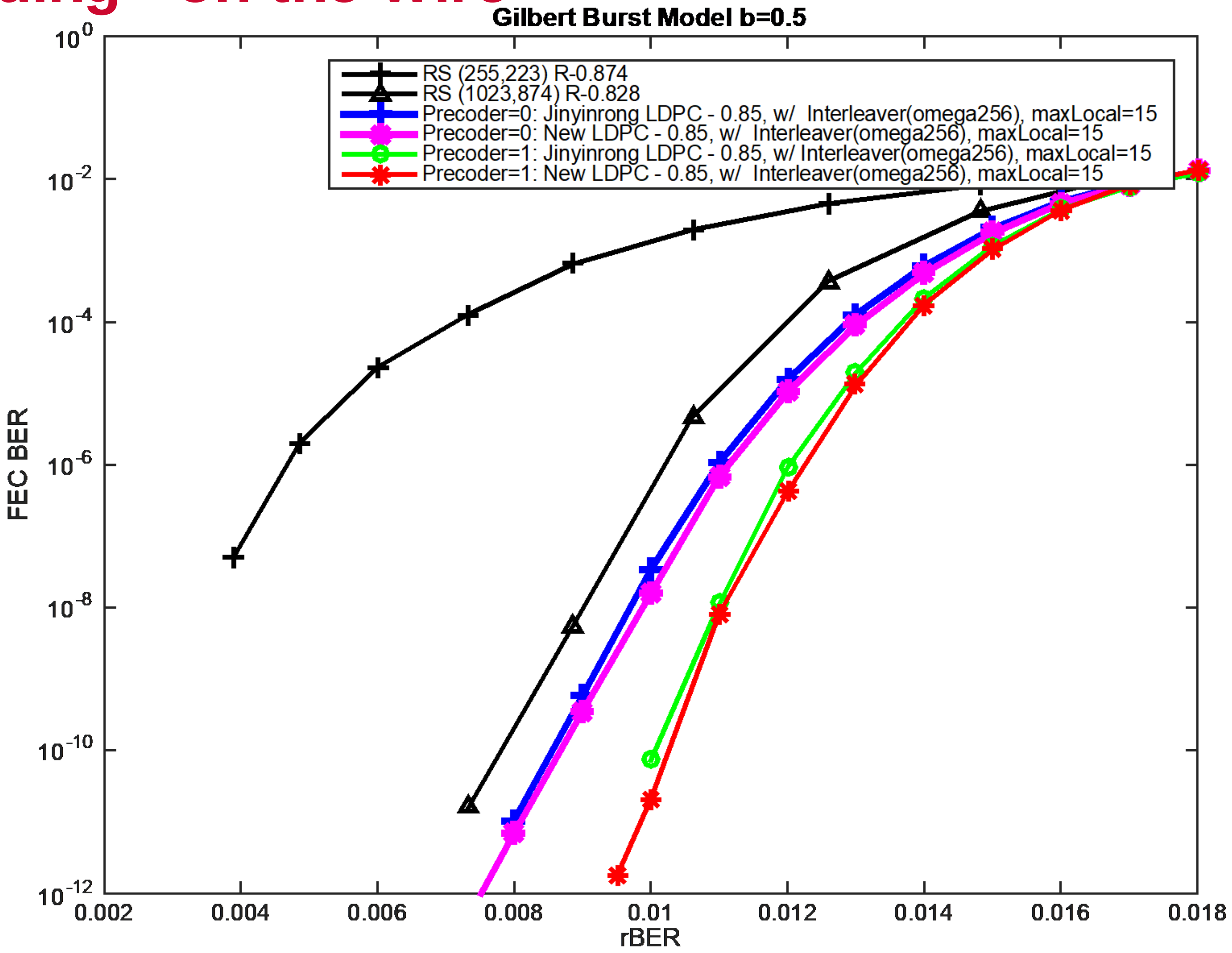
New Slide

- Several good awareness raising presentations on eCPRI and 3GPP
  - Lowest one-way latency comes from eCPRI at 100 µsec (3GPP 250 µsec)
- Was hoping to see proposals on one-way latency budgets for P802.3ca
  - Like optical power budget, need to understand what latency gets allocated between the test points for the measurement, separate for downstream and upstream e.g.:
    - Propagation delay (what is our maximum support distance?)
    - OLT processing (includes FEC)
    - ONU processing (includes FEC and any upstream scheduling latency considerations)
- Until then a total one-way FEC latency contribution < 10% (10 µsec) seems reasonable

New Slide

Impact of using pre-coding "on the wire"

- We had a request to look at performance for Gilbert burst + precoding



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Summary

- Updated “New” LDPC(18493,15677) [13x75x256] 0.848 rate, using puncturing and min-sum decoding sufficiently provides a NECG that meets error performance using 10^{-2} raw input, with an error floor below the Task Force BER objective of 1×10^{-12}.
  - The authors continue to recommend selection of LDPC as the FEC method for P802.3ca
  - Recommend code matrix and puncturing from this presentation
- Original Omega256 interleaving technique provides small gain with Gilbert burst error model for both the Jinyinrong and “New” LDPC codes studied.
  - Was optimized for a noise environment that included pre-coding in original studies
  - Other local interleaver optimizations for AWGN only and Gilbert burst only noise models may or may not provide advance beyond random interleaver.

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Thank you

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