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FEC Selection for 25G/50G/100G EPON

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Current FEC Code Proposals

A number of LDPC and RS FEC codes have been proposed and analyzed the past several meetings

Comparison of recent FEC proposals

FEC code	OH (%)	FEC Gain (dBe) @ BERout = 1e-12	BERin for BERout = 1e-12	Optical Gain Δrel to RS(255,223)		Length (bits/ usec)	Burst errors capable (bits)	Huawei		Broadcom		Nokia	
								Complexity (rel. to RS(255,223)	Latency (us)	Complexity (rel. to RS(255,223)	Latency (us)	Complexity (rel. to RS(255,223)	Latency (us)
RS(255,223) [10G EPON, XGS-PON]	12.5	7.1	1.1e-3	0		2040/ 0.08	121	1	1.2	1	?	1	0.3
RS(1023,847)	17	8.5	4.2e-3	1-1.3	1.3* 1.4#	10230 /0.40	871	7	4.5	6.9	1.1M	E+D: 0.77	Note 1	Note 1
RS(2047,1739)	15	8.5	4.1e-3	1-1.3	1.8*	22517 /0.90	1684	15	7.6	-	3.3M	E+D: 1.54	Note 1	Note 1
LDPC(16000,13184) [Huawei]	18	?	1.0e-2	1.7-2.2		16000 /0.64	208	~30	6		-	-	-	-
LDPC(18493,15677) [Broadcom]	15		1e-2	2.5* 1.8#	2.5* 1.9#	18493 /0.74	?	-	-	7.7	E: <0.3M D: 1.5M	E: 2.77 D: 2.92	64	14
LDPC(19200,16000) [Broadcom]	17	9.6	1e-2	2.8*/2.1#		19200 /0.77	?	-	-	9.1		?	-	-
LDPC(32768,16000) [Huawei]	16.7	?	1e-2	1.7-2.2		32768 /1.31	335	~33	10	-	-	-	-	-

zhao_3ca_1_0517 — laubach_3ca_4_0517 — laubach_3ca_1a_0917 — Nokia FPGA estimates

- Optical FEC gain, latency, complexity, and burst error capability are all important

Note 1 - estimation in progress
* - AWGN noise model
\# - Gilbert Elliot noise model

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From [1]

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Comparison of Proposed RS and LDPC Codes

Performance

- Proposed LDPC codes have a higher theoretical optical gain when compared with RS codes of similar code lengths (~0.5-1 dBo), [1]

Issues

- Need to operate in a high input-BER region (4E-3 to 1E-2) to achieve this extra gain
- Upstream burst mode performance in this BER region is largely unknown or shows error propagation issues [2] and degraded performance from theoretical
- LDPC codeword length can be shortened for smaller upstream bursts, but this limits the use of an interleaver, and has a significant impact on the code rate for short codes [3], or producing error floors if puncturing [4]
  (e.g., for a 100-byte payload, the code length is 3618, i.e., a rate of 0.22)
- Other similar P2MP standards (EPoC, DOCSIS 3.1) handled shortened US bursts with three different LDPC codes of different length and rate (added complexity)
- Complexity and encoding/decoding latency for LDPC is higher than for RS codes of similar length

Upstream Risks

- LDPC codes bring a lot of risks for speculative performance
- LDPC may not perform as well as RS codes for high input-BER & short US burst lengths

Shortening calculations

FEC block code sizes proposed:

- LDPC - 16,000 to 32,768 bits
- RS - 10,230 bits (RS(1023,847)) to 22,517 bits (RS(2047,1739))

Calculation of code rates with shortening
(fixed the input BER and set the output BER to 1E-12)

- **RS(255,223)** - Max input BER-1.05E-3, shortened both information & parity symbols keeping input & output BER constant; Lowest info length 64 bytes, Code rate = 0.744

- Similarly, but now with higher input BER
  - **RS(1023, 847)** - p_BER_in = 4.22E-3, R_min = 0.575, R_max = 0.829
  - **RS(2047,1739)** - p_BER_in = 4.08E-3, R_min = 0.569, R_max = 0.850
  - **LDPC(18493,15677)** - p_BER_in = 1E-2, R_min = 0.1538

Observations

To minimize risks, perhaps RS codes are the best choice for upstream burst mode operation, whereas an LDPC code for downstream continuous mode might give better performance

Past Working Assumptions

- It is desirable to use the same FEC for DS and US (BCM request for ASIC testing/verification purposes)

Proposals

Proposal. Use an LDPC code in the downstream and an RS code in the upstream

This could be the optimal solution, where

- The performance gain for full-length LDPC codes are exploited for the continuous-mode downstream
- The reconfigurability and burst error capabilities of RS codes are exploited for the burst-mode upstream.

Alternative proposal. Use a RS code for both upstream and downstream.

This proposal

- Satisfies the request to use the same FEC codes in both directions for ASIC testing and verification purposes
- Provides extra robustness against burst errors

References

[1] B. Powell et al., Latency and Complexity for Various 25/50/100G FEC Code Proposals, powell_3ca_2a_0917, Charlotte, NC, Sep. 2017

[2] D. van Veen, et. al., CDR Locking and Error distribution at High BER for 25 Gb/s, houtsma_3ca_2_1117, Orlando, FL, Nov. 2017

[3] M. Laubach et al., FEC Proposal for NGEPON - update, laubach_3ca_1_1117, Orlando, FL, Nov. 2017

[4] R. Bonk et al., LDPC Code Length Reduction, bonk_3ca_1_1117, Orlando, FL, Nov. 2017


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Backup

Shorter US bursts

- We will be transmitting some number of whole FEC codewords in an US burst
- Summary of LDPC Puncturing Analysis ([Bonk]) and Code Shortening ([Laubach]) analyses
  - Nokia - Puncturing - Cannot puncture LDPC codes to less than ~80% w/o error floors; possible need for a family of LDPC codes for a range of lengths (and possibly input BER)
  - BCM - Has shown shortening but at greatly reduced code rates (0.848 nom. Down to ~0.21)
  - Poor efficiency for smaller US bursts using LDPC codes
- RS codes capable of handling burst errors, adjusting to a given input BER, and to handle shortened codes

  For an RS(N,K) code with m-bit symbols, capable of correcting T = N-K symbols, it is easy to use this one .
- Maybe this is an argument for different FECs for DS & US
- Alternative - Use RS-1K/2K for both US and DS if testability (and lower latency & complexity) still important

Comparison of recent FEC proposals (powell_3ca_1a_0917)

FEC code	OH (%)	FEC Gain (dBe) @ BERout = 1e-12	BERin for BERout = 1e-12	Optical Gain Δ rel to RS(255,223)	Length (bits/ usec)	Burst errors capable (bits)	Huawei		Broadcom		Nokia	
							Complexity (rel. to RS(255,223)	Latency (us)	Complexity (rel. to RS(255,223)	Latency (us)	Complexity (rel. to RS(255,223)	Latency (us)
RS(255,223) [10G EPON, XGS-PON)	12.5	7.1	1.1e-3	0	2040/ 0.08	121	1	1.2	1	?	1	0.3
RS(1023,847)	17	8.5	4.2e-3	1-1.3	10230 /0.40	871	7	4.5	6.9	1.1M	E+D: 0.77	Note 1	Note 1
RS(2047,1739)	15	8.5	4.1e-3	1-1.3	22517 /0.90	1684	15	7.6	-	3.3M	E+D: 1.54	Note 1	Note 1
LDPC(16000,13184) [Huawei]	18	?	1.0e-2	1.7-2.2	16000 /0.64	208	~30	6		-	-	-	-
LDPC(18493,15677) [Broadcom]	15		1e-2	2.5* 1.8#	18493 /0.74	?	-	-	7.7	E: <0.3M D: 1.5M	E: 2.77 D: 2.92	64	14
LDPC(19200,16000) [Broadcom]	17	9.6	1e-2	2.8*/2.1#	19200 /0.77	?	-	-	9.1		?	-	-
LDPC(32768,16000) [Huawei]	16.7	?	1e-2	1.7-2.2	32768 /1.31	335	~33	10	-		-	-	-

1.3* 1.4#

1.8*

2.5* 1.9#

zhao_3ca_1_0517

laubach_3ca_4_0517

laubach_3ca_1a_0917

Nokia FPGA estimates

- Optical FEC gain, latency, complexity, and burst error capability are all important

Note 1 - estimation in progress
* - AWGN noise model
\# - Gilbert Elliot noise model

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Comparison of enhanced FEC candidate codes

FEC code	Length(bit)	Code rate	BER_in@ BER_out= 1.0e-12	Optical coding gain relative to RS(255,223) (dBo) (*a)	Burst Error Correction Capability(bit) (*b)	Relative Complexity (*c)	Estimated Decoding Latency (us)
RS(255,223)	2040	0.87	1.1e-3	0	121	1	1.2us
RS(1023,847)[1]	10230	0.83	4.2e-3	0.9~1.2	871	7	4.5us
RS(2047,1739)[1]	22517	0.85	4.5e-3	1~1.3	1684	15	7.6us
Bolded 3DBCH[2]	16K or 37K	0.83 or 0.85	1.0e-2	1.7~2.2	?	?	?
LDPC(16000,13184)	16000	0.82	1.0e-2	1.7~2.2	208	~30	6us
LDPC(32768,27648)	32768	0.84	1.0e-2	1.7~2.2	335	~33	10us

(*a) Assume APD receiver with 1 dBe=(0.7~0.9)dBo
(*b) Assume RS decoder for 25Gbps is 100K gates
(*c) The burst error correction capability for RS codes is calculated by (t-1)*m+1, referring to [3]

FEC Codes Studied

From laubach_3ca_1_0517.pdf page 14. Added Normalized Die Size column.

	Length	Rate	Parity	User	Encoded	NECG[1] (dB)		Normalized Die Size [2]	Notes
						AWGN	Gilbert Burst		
Folded BCH	2kB	0.83	3272	16576	19848	2.25	1.48	n/a	bits
	4kB	0.83	6064	30784	36848	2.6	1.78	n/a	bits
LDPC	2kB	0.848	2816	15677	18493	2.46	1.8	7.7	bits (18493,15677)
	2kB	0.833	3200	16000	19200	2.82	2.12	9.1	bits (19200,16000)
RS	(255,223)	0.8745	256	1784	2040	0	0	1	S=8, T=16 (10G-EPON)
	(1023,847)	0.828	1760	8470	10230	1.34	1.35	6.9	S=10, T=88

[1] Electrical gain over RS(255,223)

[2] Relative to RS(255,223) size

Comparison of suitable codes proposed thus far
Using ideal AWGN-model (only random errors)

*) Assuming APD-based receiver with 1 dBe = (0.7-0.9) dBo

FEC code	OH (%)	FEC Gain (dBe) @BERout =1e-12	BERin for BERout =1e-12	Optical gain delta relative to RS(255,223) (dBo)*	Length (bits)	Burst errors Capable (bits)	Power consumption	Complexity	Latency
RS(255,223)	12.5	7.1	1.1e-3	0	2040	121	low	low	low
RS(1023,847)	17.2	8.5	4.2e-3	1-1.3	10230	871	med	low	low
RS(2047,1739)	*15*	*8.5*	*4.1e-3*	*1-1.3*	*22517*	*1684*	*med/high*	*med*	*med*
BCH(4095,3501)	14.5	8.5	4e-3	1-1.25	4095	49	med	low	low
LDPC(16000,13952)	13	8.9	5.8e-3	1.25-1.6	16000	?	high	high	high
LDPC(19200,16000)	17	9.6	1e-2	1.75-2.25	19200	?	high	high	high
Folded product BCH	17	9.7	1.1e-2	1.8-2.35	16384	?	?(<LDPC)	?	?

We have to be careful when comparing FEC gain relative to RS(255, 223) for alternative codes that have shorter burst error capabilities.
Coding gain improvement might turn out smaller than expected!

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FEC decoding latency & implementation complexity

						Zhao - Huawei		Laubach - BCM		Nokia (FPGA est.)	
FEC code	**Length(bit)**	**Code rate**	**BER_in@ BER_out= 1.0e-12**	**Optical coding gain relative to RS(255,223) (dBo) (*a)**	**Burst Error Correction Capability(bit) (*b)**	**Relative Complexity (*c)**	**Estimated Decoding Latency (us)**	**Relative Complexity**	**Estimated Decoding Latency (us)**	**Relative Complexity**	**Estimated Decoding Latency (us)**
RS(255,223)	2040	0.87	1.1e-3	0	121	1	1.2us	1	Note 1	1	0.3
RS(1023,847)[1]	10230	0.83	4.2e-3	0.9~1.2	871	7	4.5us	6.9	Note 1	Note 2	Note 2
RS(2047,1739)[1]	22517	0.85	4.5e-3	1~1.3	1684	15	7.6us			Note 2	Note 2
Bolded 3DBCH[2]	16K or 37K	0.83 or 0.85	1.0e-2	1.7~2.2	?	?	?	-	-	-	-
LDPC(16000,13184)	16000	0.82	1.0e-2	1.7~2.2	208	~30	6us	7.7 LDPC(18493,15677)	5.5[4]	64 LDPC(18493,15677)	14
LDPC(32768,27648)	32768	0.84	1.0e-2	1.7~2.2	335	~33	10us	9.1 LDPC(19200,16000)		-	-

(*a) Assume APD receiver with 1 dBe=(0.7~0.9)dBo
(*b) Assume RS decoder for 25Gbps is 100K gates
(*c) The burst error correction capability for RS codes is calculated by (t-1)*m+1, referring to [3]

(from zhao_3ca_1_0517.pdf)

(laubach_3ca_4_0517.pdf)

(# - 15 decode iterations)

Note 1 (BCM) - Looking for contrib. ref. w/BCM latency #'s
Note 2 (Nokia) - Will fill in as many values as available - KALEB - Action item for you :-)

Note 3 - Aug. 7 email from Kaleb - "In simulation the decoder latency is ~170 clocks. The data path is 32bit, so a 255 RS code is 64 clocks" => 0.08 usec?. KALEB - Is this correct?

Note 4 (BCM) - Recalling that BCM decoding latency for LDPC(18493,15677) is ~5.5 usec; looking for contrib. ref.

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FEC concerns

- To minimize risks, perhaps R-S is the best choice for upstream burst mode operation
- LDPC for downstream continuous mode might give better performance
- Past working assumptions have been:
  - It is desirable to use the same FEC for DS & US (ASIC/FPGA testing purposes)
- To achieve the improved optical gains with LDPC FECs, operation in the 1E-3 to 1E-2 input BER range is required
- Questions were raised about burst mode CDR performance in this high-BER region
- Questions were also raised about the increased latency of LDPC codes over that of RS-1K/2K codes

Add Latency references?
- powell_1_0917
- wei_1_1117
- dai_2_1117

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Discussion - 2

- Alternative - Use RS-1K/2K for both US and DS if testability (and lower latency & complexity) still important
  - CDR issues
  - Bursty error multiplication
  - Penalty of ~0.4 dBo seen in burst mode in this region over theoretical continuous mode operation (potential FEC gain of 1.64 dBo reduced to 1.24 dBo
- Concerns about smaller US burst sizes needed than current RS-1K/2K & LDPC FEC codewords
- Summarize Puncturing (Nokia) and Shortening (BCM) analyses here
  - Nokia - Puncturing - Can't puncture LDPC codes to less than ~80% w/o error floors
  - BCM - Has shown shortening but at greatly reduced code rates (0.848 nom. Down to ~0.21)
  - Poor efficiency for smaller us bursts using LDPC codes
- RS codes well behaved for shortening (and with significantly higher code rates
  - May need some of Adriaan's equations/arguments here…
- xx
  - yy
- xx