

A blurred photograph of a crowd of people walking across a street at a crosswalk. The people are in motion, creating a sense of a busy urban environment. The crosswalk is marked with white stripes on a dark asphalt surface.

802.3cb Test Points Proposal

Supporters

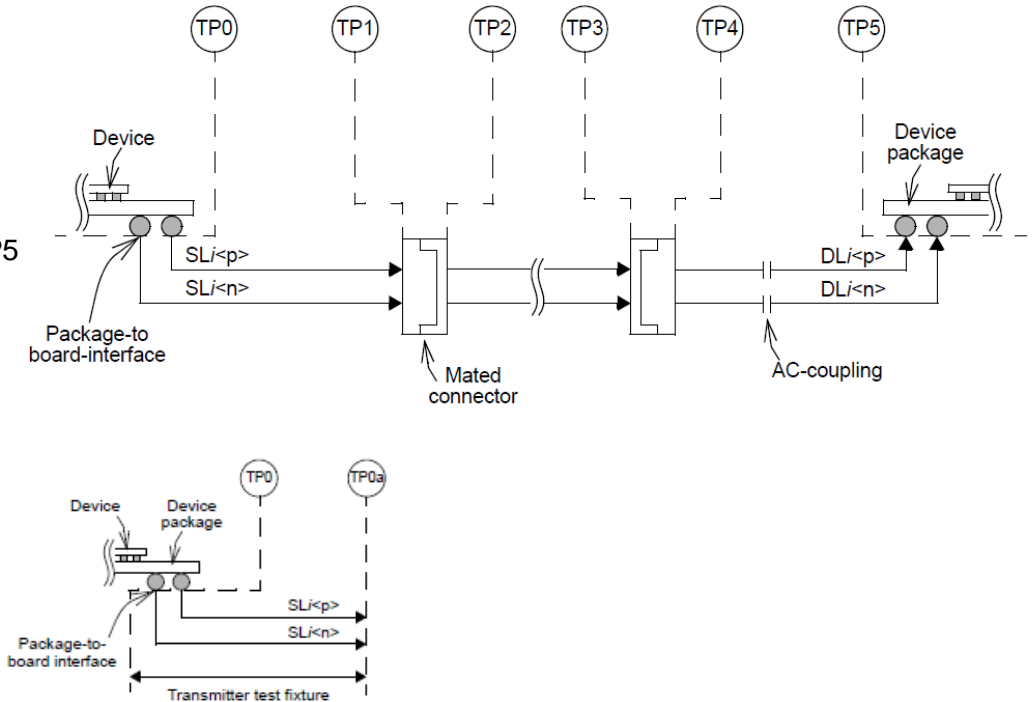
- Rich Mellitz, Intel
- William Lo, Marvell
- Peter Wu, Marvell
- Thomas Skaar, Seagate
- Dan Smith, Seagate

Introduction

- **The goal is to adopt a baseline for test point definition**
 - These will be used as a baseline reference to build upon. The loss budgets and tests associated with each test point will be based on these test points.
- **There are two different models shown in the presentation that use 802.3bj as a starting point**
 - A backplane reference model that is a generic model that could be a closed and/or proprietary system in which the only loss budget is ball-to-ball
 - A storage reference model that is more focused and allows for insertion loss budgeting of the HDD since it's an external interface
 - The ball-to-ball budgets are equivalent between the two models

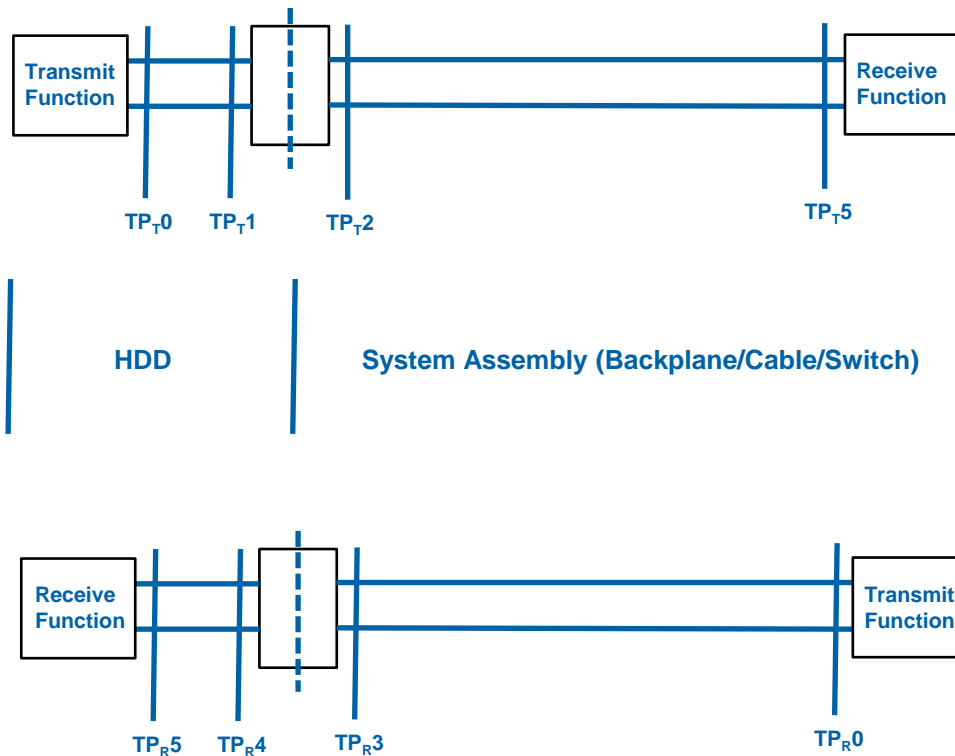
Chip Spec

- Channel is measured from TP0 to TP5
 - Package ball to package ball
- Device Tx is measured at TP0a
 - TP0 is not observable in an implemented system
- Device Rx is measured at TP5a
 - TP5 is not observable in an implemented system
- Receiver Interference Tolerance Test is calibrated at TP5



Storage Device Spec

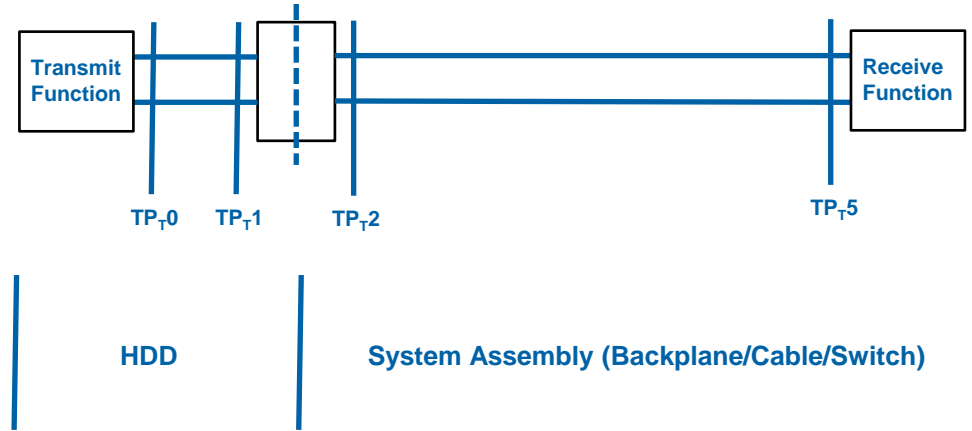
- For the storage application, it's important to budget the drive loss since it's an external component.
- The rest of the "box" is vender specific and can be any combination of cable and backplane
- This implies a Storage Reference Model with an asymmetric loss budget
 - Informative insertion loss would be the same as in the backplane reference model
- For storage device (HDD)
 - Tx is measured at TP_T2, after the mated connector
 - Receiver Interference Tolerance Test is calibrated at TP_T4
- For host chip
 - Use pin to pin spec for compliance
 - Tx is measured at TP₀a
 - Receiver Interference Tolerance Test is calibrated at TP₅



Storage Device Spec Cont'd

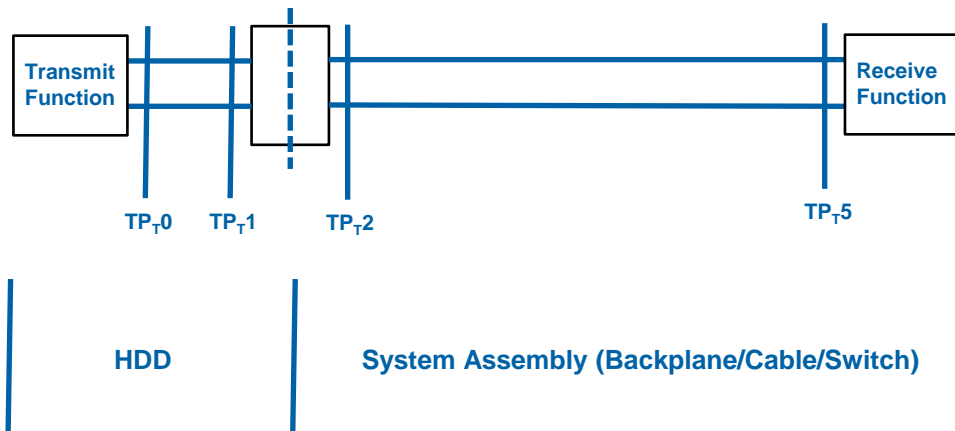
▪ Channel

- Informative storage device loss from TP_{T0} to TP_{T1} and TP_{R4} to TP_{R5}
- Informative system loss from TP_{T1} to TP_{T5} and TP_{R0} to TP_{R4}
- Channel is measured from TP_{T1} to TP_{T5} and TP_{R0} to TP_{R4}
- Channel loss is extrapolated from TP_{T1} to TP_{T0} and from TP_{R4} to TP_{R5} using COM



Storage Device Test Point Definitions

- TP_{T0} to TP_{T5} and TP_{R0} to TP_{R5}
 - The channel including all insertion loss between package balls
 - This includes the HDD and system loss
 - This loss would be equivalent to the chip spec loss
- TP_{T1} to TP_{T5} and TP_{R0} to TP_{R4}
 - Measurement of storage system is done between these points.
- TP_{T0} to TP_{T1} and TP_{R4} to TP_{R5}
 - Recommended maximum insertion loss of the storage device PCB traces
- TP_{T2}
 - Storage device transmitter compliance point
 - TP0a is not applicable to a storage device
 - TP_{T2} is observable in an implemented storage device
- TP_{R3}
 - Storage device receiver compliance point
 - TP5a is not applicable to a storage device
 - TP_{R3} is observable in an implemented storage device



Storage Device Test Point Definitions Cont'd

- TP_{R4}
 - Receiver Interference Tolerance Test calibration point
 - The storage device must be compliant with the delivered signal at TP_{R4}
- TP_{R1} to TP_{T2} and TP_{R3} to TP_{R4}
 - Recommended mated connector pair fixture loss

