

IEEE802.3ca Tx and Rx Spec Proposal

Richard Mellitz, Intel

IEEE 802.3 Interim, Atlanta GA, January 2015

Tx Spec Host

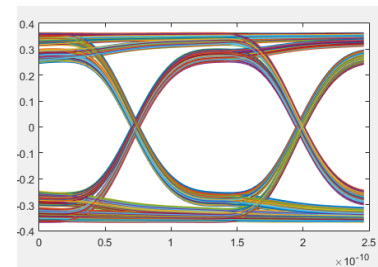
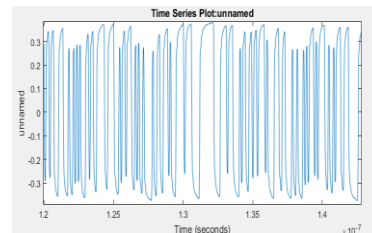
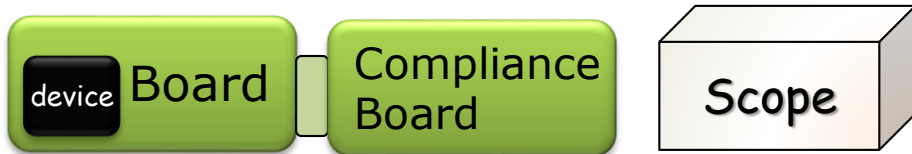
- Transmitted signal to noise distortion ratio (SNDR) and waveform parameters are from a fitted pulse from derived from a PRBS9 test pattern
- Jitter is determined from PRBS9 pattern

Table 92-6—Transmitter characteristics at TP2 summary

| Parameter | Subclause reference | Value | Units |
|--|---------------------|--------------|-------|
| Differential peak-to-peak output voltage (max.) with Tx disabled | 92.8.3.1 | | mV |
| DC common-mode voltage (max.) | 92.8.3.1 | | V |
| AC common-mode output voltage, v_{cmi} (max., RMS) | 92.8.3.1 | | mV |
| Differential peak-to-peak voltage, v_{dt} (max.) | 92.8.3.1 | | mV |
| Differential output return loss (min.) | 92.8.3.2 | | dB |
| Common-mode to differential mode output return loss (min.) | 92.8.3.3 | | dB |
| Common-mode to common-mode output return loss (min.) | 92.8.3.4 | | dB |
| Transmitter steady-state voltage, v_f (min.) | 92.8.3.5.2 | | V |
| Transmitter steady-state voltage, v_f (max.) | 92.8.3.5.3 | | |
| Linear fit pulse peak (min.) | 92.8.3.5.2 | $\times v_f$ | V |
| Transmitted waveform | | | |
| abs coefficient step size (min.) | 92.8.3.5.4 | | |
| abs coefficient step size (max.) | 92.8.3.5.4 | | |
| minimum precursor full-scale ratio | 92.8.3.5.5 | | |
| minimum post cursor full-scale ratio | 92.8.3.5.5 | | |
| Signal-to-noise-and-distortion ratio (min.) | 92.8.3.7 | | dB |
| Output jitter (max.) | | | UI |
| Even-odd jitter, peak-to-peak | 92.8.3.8.1 | | |
| Effective bounded uncorrelated jitter, peak-to-peak | 92.8.3.8.2 | | |
| Effective total uncorrelated jitter, peak-to-peak | 92.8.3.8.3 | | |
| Signaling rate, per lane | 92.8.3.9 | | GBd |
| Unit interval nominal | 92.8.3.9 | | ps |

Transmitter Waveform

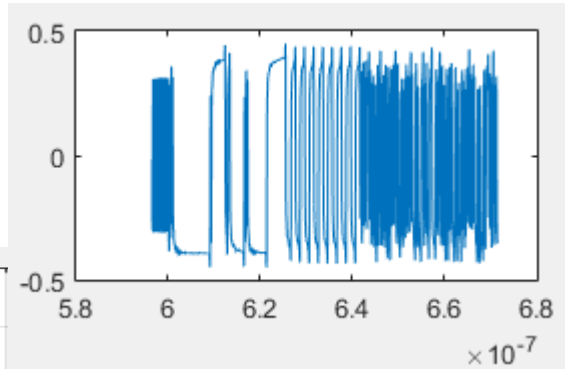
Questions often asked



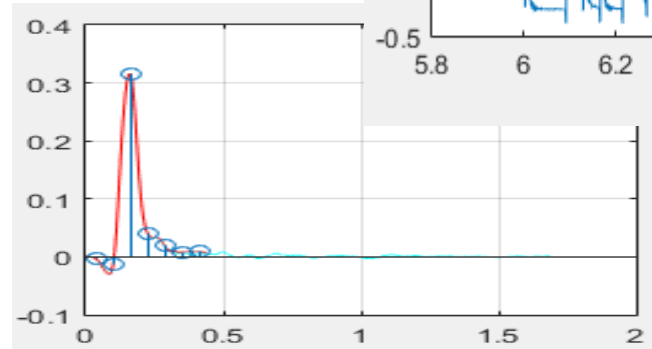
- What does the eye diagram or waveform mean to
 - The board
 - The device
- How much of the board ISI is compensated in the Device
- What is the affect of non linear devices
- How much noise is introduced outside of the lane under test?
- Its hard to tell

Common language

- Pulse response
 - AKA single bit response (SBR)
- Intuitive perspective
- Can we take a measurement something like this



- And get this?
 - Ref Circa 2010 in IEEE specifications



Baseline Understanding of Superposition: Start with the Response to Single Bit

- A measured response may be generated for and arbitrary bit pattern
 - Using a shifted version of that pulse
 - And adjusting for whether the bit corresponding to the shift is a zero or 1
- Its just superposition

Spread Sheet Example: Superposition Review

(M = 1 sample per UI)

| Single bit response samples | | | | | | | | |
|-----------------------------|------|------|-------|-------|-------|-------|------|--|
| 1 | 2 | 3 | 5 | 6 | 7 | 8 | 9 | |
| 0 | -0.1 | 0.75 | -0.05 | -0.1 | | | | |
| | 0 | -0.1 | 0.75 | -0.05 | -0.1 | | | |
| | | 0 | -0.1 | 0.75 | -0.05 | -0.1 | | |
| | | | 0 | -0.1 | 0.75 | -0.05 | -0.1 | |

$$P = \begin{bmatrix} 0 & p_1 & p_2 & p_3 & p_4 & p_5 & 0 & 0 & 0 \\ 0 & 0 & p_1 & p_2 & p_3 & p_4 & p_5 & 0 & 0 \\ 0 & 0 & 0 & p_1 & p_2 & p_3 & p_4 & p_5 & 0 \\ 0 & 0 & 0 & 0 & p_1 & p_2 & p_3 & p_4 & p_5 \end{bmatrix}$$



| Bit stream |
|------------|
| 1 |
| -1 |
| 1 |
| 1 |

X

x1
x2
x3
x4



| Interim bit response samples | | | | | | | | |
|------------------------------|------|------|-------|------|-------|-------|------|--|
| 1 | 2 | 3 | 5 | 6 | 7 | 8 | 9 | |
| 0 | -0.1 | 0.75 | -0.05 | -0.1 | 0 | 0 | 0 | |
| 0 | 0 | 0.1 | -0.75 | 0.05 | 0.1 | 0 | 0 | |
| 0 | 0 | 0 | -0.1 | 0.75 | -0.05 | -0.1 | 0 | |
| 0 | 0 | 0 | 0 | -0.1 | 0.75 | -0.05 | -0.1 | |

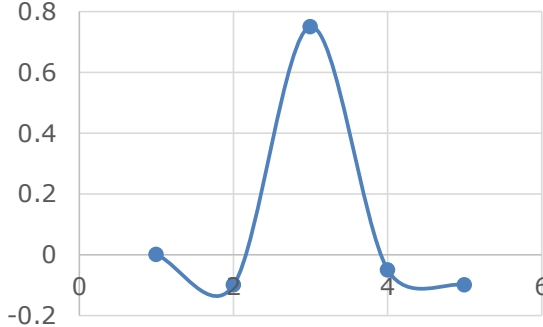
| | | | | | | | | |
|---|------|------|------|-----|-----|-------|------|--|
| 0 | -0.1 | 0.85 | -0.9 | 0.6 | 0.8 | -0.15 | -0.1 | |
|---|------|------|------|-----|-----|-------|------|--|

$$y = [P^T * X]^T$$

$$[0, p_1*x_1, p_1*x_2 + p_2*x_1, p_1*x_3 + p_2*x_2 + p_3*x_1, p_1*x_4 + p_2*x_3 + p_3*x_2 + p_4*x_1, p_2*x_4 + p_3*x_3 + p_4*x_2 + p_5*x_1, p_3*x_4 + p_4*x_3 + p_5*x_2, p_4*x_4 + p_5*x_3, p_5*x_4]$$

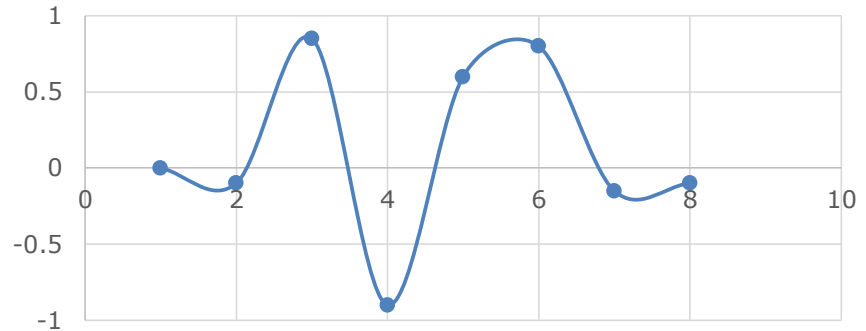
Single Bit Response

[0, p1, p2, p3, p4, p5, 0, 0, 0]



'p' is pulse response
'x' are the bits
'y' is the measured response

Bit stream response



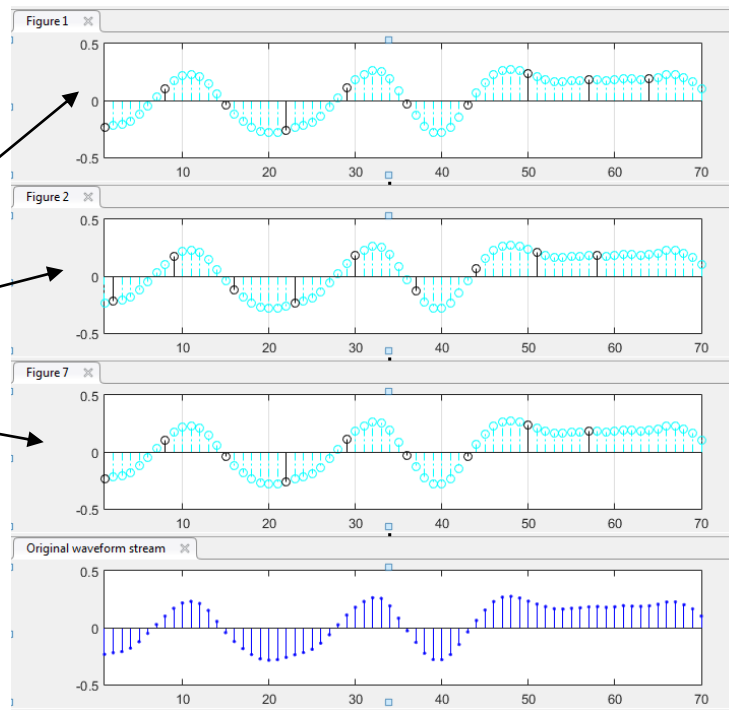
M samples per UI

- Perform for each sample $y = [P^T X]^T$
- That suggest we can have M equations for linear fitting
- y is what we measure.
 - It has M samples per UI
 - Y is the collection of y 's for each sample
- We can solve for P
 - $P = YX^T(XX^T)^{-1}$
 - The first row of P is single bit response

Clause 85 example: Create matrix Y for each sample

Eq. 85-4

$$Y = \begin{bmatrix} y(1) & y(M+1) & \dots & y(M(N-1)+1) \\ y(2) & y(M+2) & \dots & y(M(N-1)+2) \\ \dots & \dots & \dots & \dots \\ y(M) & y(2M) & \dots & y(MN) \end{bmatrix}$$

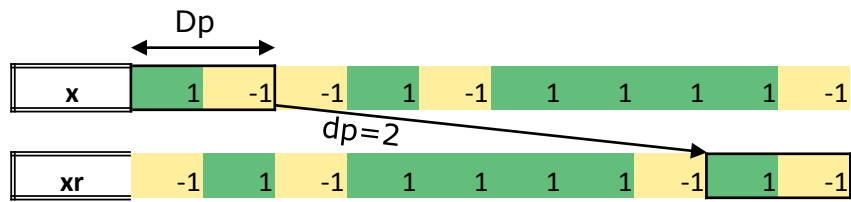


One for each sample
in the UI

Clause 85 example: for bit vector, x for Dp=2 and Np=5

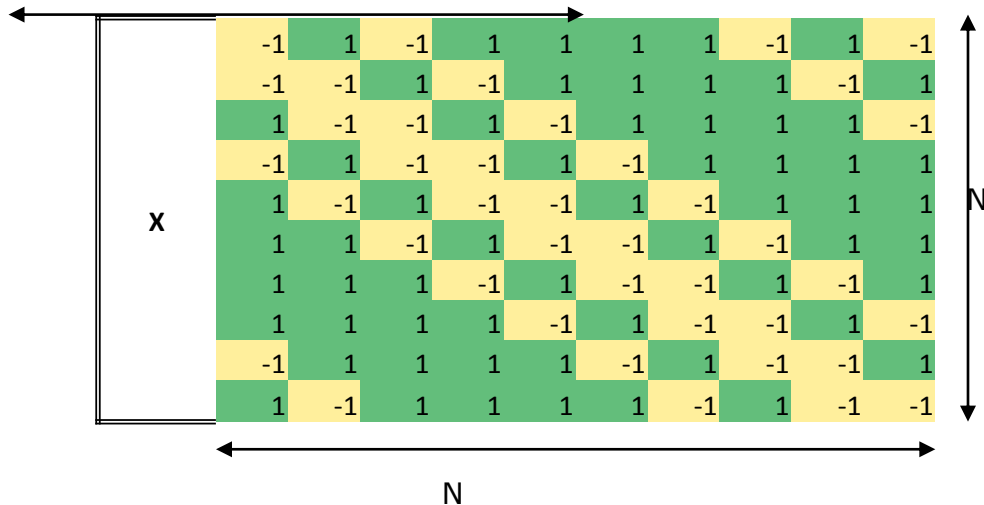
Eq 85-5: Shifted bits bit d_p

$$x_r = [x(D_p + 1) \ x(D_p + 2) \dots \ x(N) \ x(1) \ \dots \ x(N - D_p)]$$

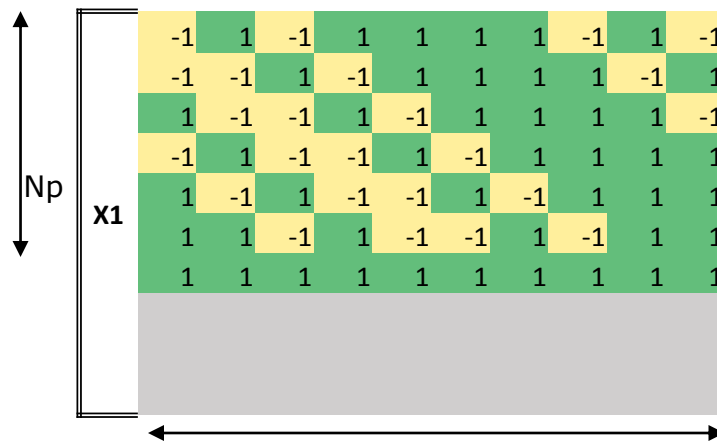
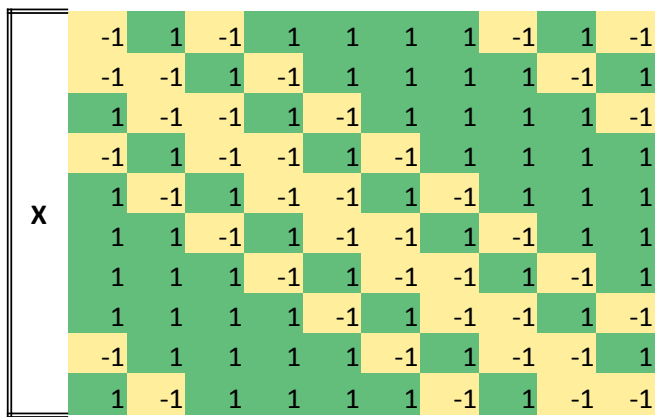


Eq 85-6: Matrix of circular shifted bits

$$X = \begin{bmatrix} x_r(1) & x_r(2) & \dots & x_r(N) \\ x_r(N) & x_r(1) & \dots & x_r(N-1) \\ \dots & \dots & \dots & \dots \\ x_r(2) & x_r(3) & \dots & x_r(1) \end{bmatrix}$$

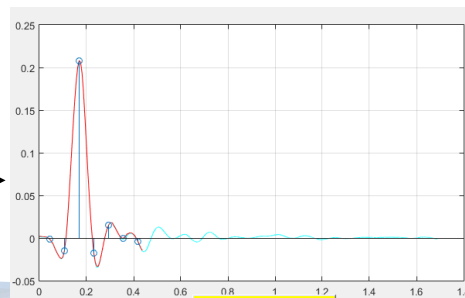


For IEEE802.3ca Recommendation: Dp=2, Np=40, fit is Np+Dp+1 bits

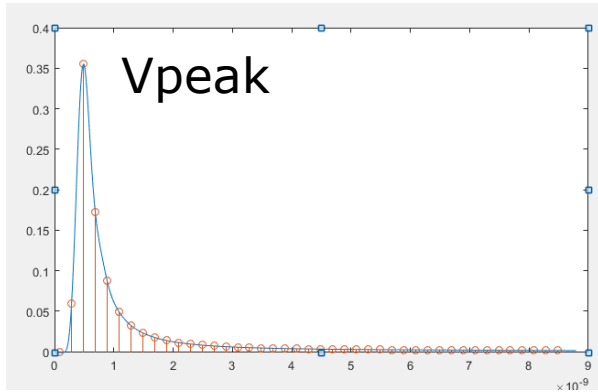


$$P = YX_1^T(X_1X_1^T)^{-1}$$

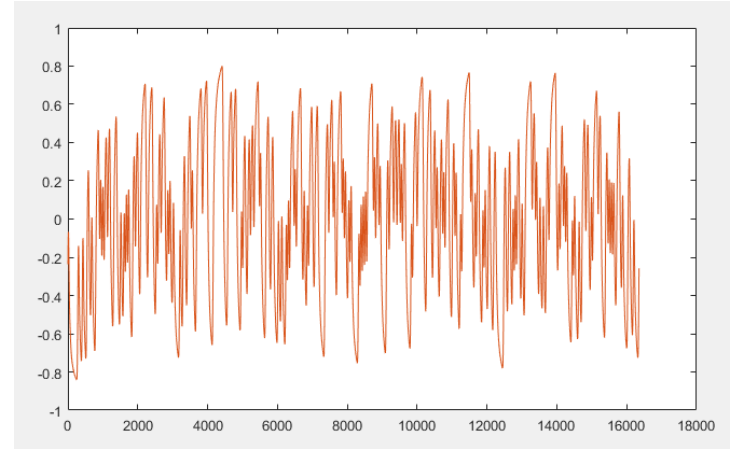
First Column of P



Reconstructed waveform out of fit pulse and data bits



$$\otimes X_1 =$$

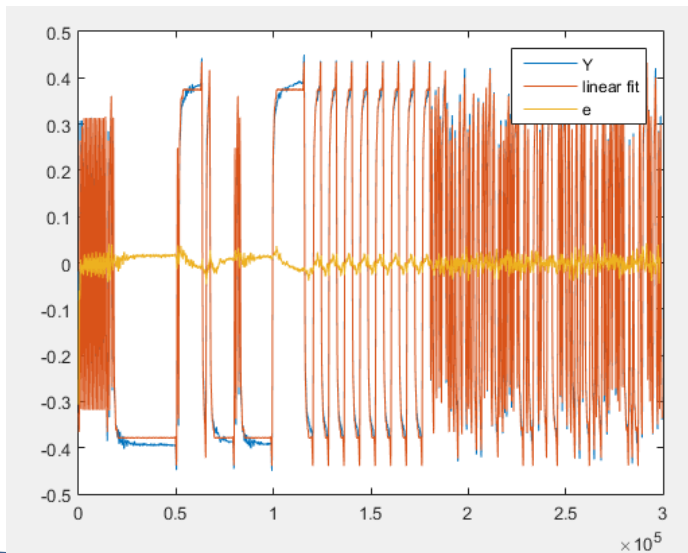


Errors per sample point outside the receiver's DFE reach

Eq 85-8: Errors are the Matrix of column E

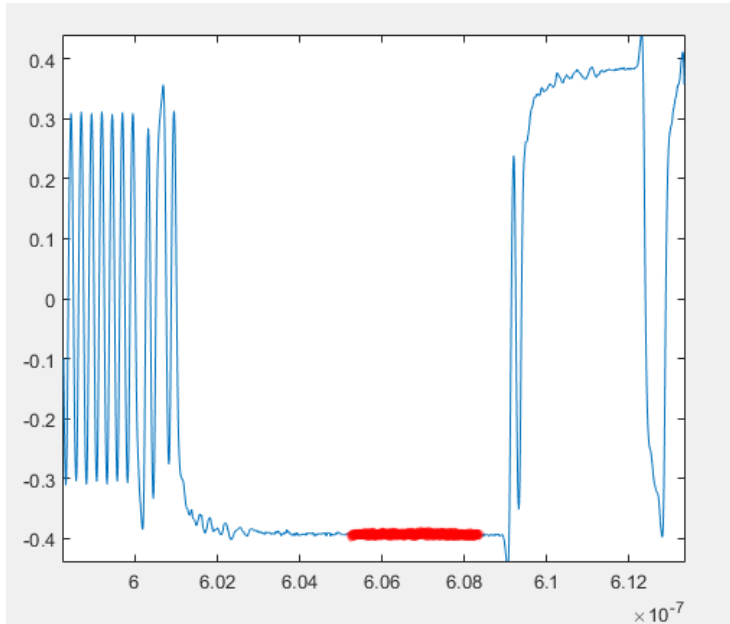
The error waveform, $e(k)$, is then read column-wise from the elements of E as shown in Equation (85-8).

$$E = PX_1 - Y = \begin{bmatrix} e(1) & e(M+1) & \dots & e(M(N-1)+1) \\ e(2) & e(M+2) & \dots & e(M(N-1)+2) \\ \dots & \dots & \dots & \dots \\ e(M) & e(2M) & \dots & e(MN) \end{bmatrix} \quad (85-8)$$



- May be use to justify just how many taps of DFE are required.
- The rms of "E" is basically noise that receiver will see,
 - Lets call that σ_e
- It is in relation to the peak of the pulse
- So the SNR might be $20 \cdot \log_{10}(V_{\text{peak}} / \sigma_e)$
- But there is more noise to consider

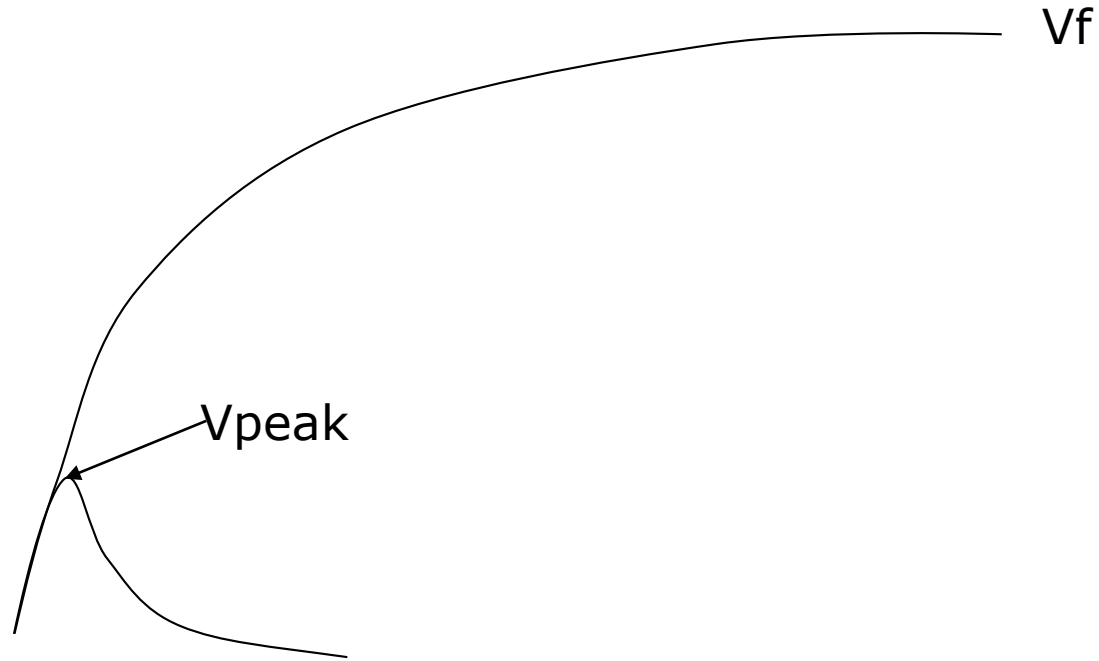
Other noise



- Now the measure waveform not averaged but pattern triggered so we look a that same run of zeroes or ones in the data pattern
- The rms of this noise is introduced outside the lane
 - Lets call this σ_n
 - We RSS σ_n 's from the run of ones and the run of zeroes to and aggregate σ_n
- Combing the two rms values results in a Signal to noise and distortion ratio of SNDR

- $$\text{SNDR} = \frac{V_{peak}}{\sqrt{\sigma_n^2 + \sigma_e^2}}$$

Spec Vf and Vpeak/Vf (it is related to loss)

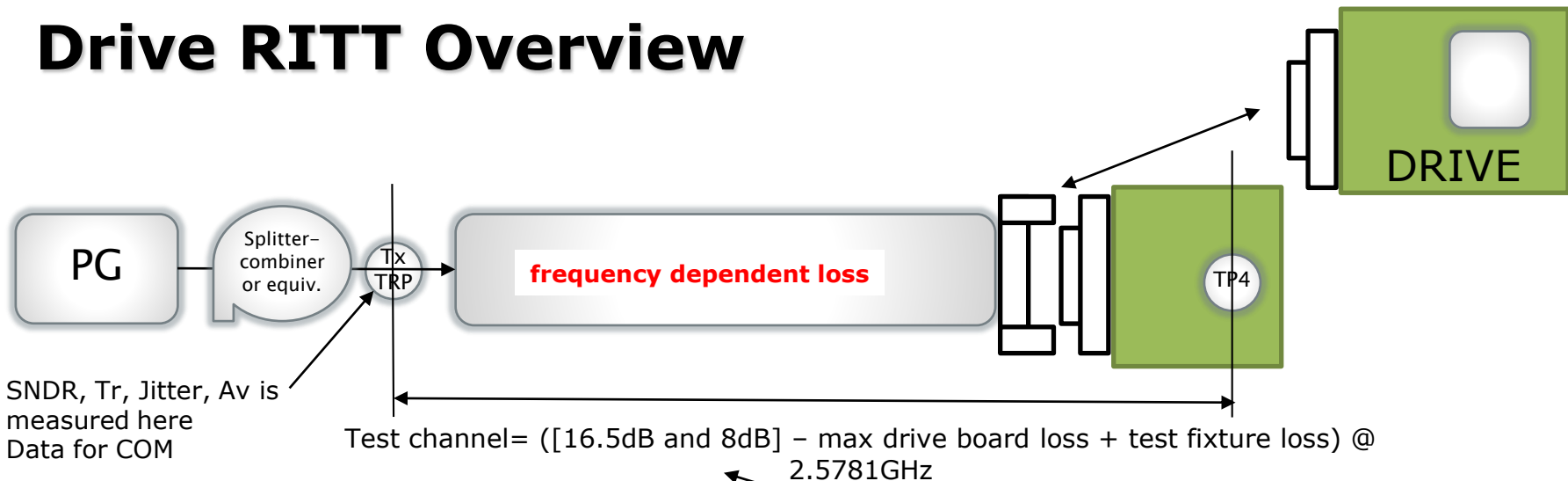


Extracting FFE Tap Coefficients if required

- 2 measurement waveforms required
 - Without equalization
 - With equalization
- Extracted to fitted pulse responses IEEE802.3 Clause 92.8.3.5.1
 - Without equalization, R
 - With equalization, P
- $P = R * C$
 - Where C is the tap coefficient vector
- $C = (R^T * R)^{-1} * R^T * P$ for each sample
- The values of C are used where the error P-R(for each sample) is minimum.

Receiver tests

Drive RITT Overview



- Measure s-parameter for Test Channel
- Set PG Tr, Av, and Jitter
- Measure PG SNDR and use in COM
- COM Tx Parameters are for reference chip spec
- Add board loss parameter in COM equivalent to max drive board loss - test fixture loss
- Determine what value of SNDR (SNR_TX) makes COM fail
- Sent noise to in to produce SNDR at TxTRP indicated by SNR_TX in last step.
- Determine DER using a test reference pattern
- Jitter tolerance use same setup except no noise is added and COM is not used.

Host RITT has its own table of losses

CHIP TO CHIP specs

- Borrow from IEEE802.3bj CL 93
- TX (Remove adaptive TX eq)
- RX
- Channel
 - Adopt reference package and ref equalizer developed in future adhoc work.