50GBASE-FR and 100GBASE-DR, ER and MPI (Comment 138, 139) (200GBASE-DR4 and 400GBASE-DR4)

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Summary

- Extinction ratio specifications for 400GBASE-DR4 (P802.3bs cl.124), 100GBASE-DR (P802.3cd cl.140), 200GBASE-DR4 (P802.3bs cl.121) and 50GBASE-FR currently preclude directly modulated lasers.
- MPI modeling shows that the ER spec for 50GBASE-FR and 100GBASE-DR could be reduced to 3.5 dB with an almost negligible increase in MPI penalty.

MPI calculations using *king_02a_0116_smf*

MPI link model: 400GBASE-DR4 (P802.3bs cl.124)

- MDI reflection is -26 dB (Tx and Rx); min 5 dB ER in draft 3.0
- 3 dB IL lumped just before last reflection
- 4 connections with reflectance -45 dB, plus 4 connections with reflectance -55 dB

MPI link model: 100GBASE-DR (P802.3cd cl.140)

- MDI reflection is -26 dB (Tx and Rx), min 5 dB ER in draft 1.2
- 3 dB IL lumped just before last reflection
- 4 connections with reflectance -45 dB, plus 4 connections with reflectance -55 dB

MPI link model: 200GBASE-DR4 (P802.3bs cl.121)

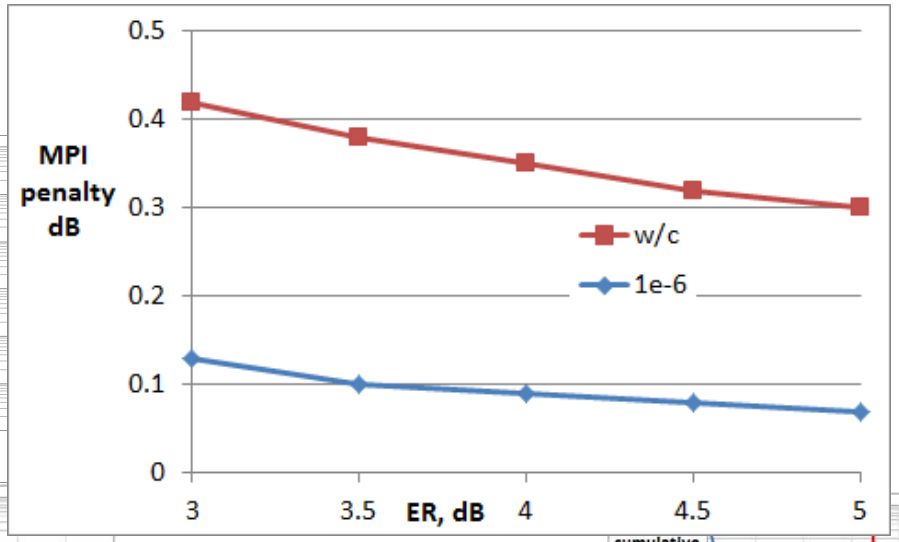
- MDI reflection is -26 dB (Tx and Rx); min 4.5 dB ER in draft 3.0
- 3 dB IL lumped just before last reflection
- 4 connections with reflectance -45 dB, plus 4 connections with reflectance -55 dB

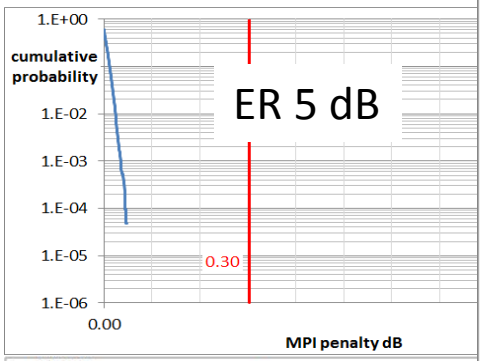
MPI link model: 50GBASE-FR (P802.3cd cl.139)

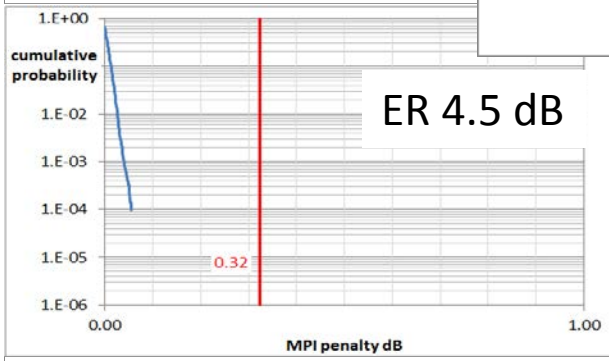
- MDI reflection is -26 dB (Tx and Rx); min 4.5 dB ER in draft
- 4 dB IL lumped just before last reflection
- 4 connections with reflectance -35 dB, plus 4 connections with reflectance -55 dB

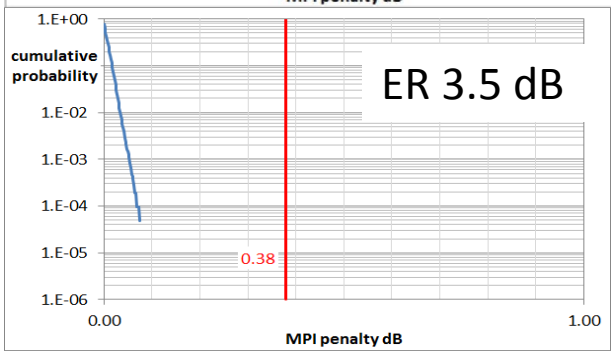
http://www.ieee802.org/3/bs/public/adhoc/smf/16_01_07/king_02a_0116_smf.7z

MPI penalty vs ER (3 dB IL, 4x45 dB RL)

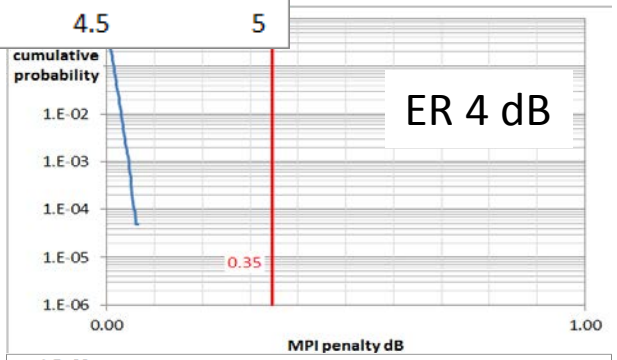


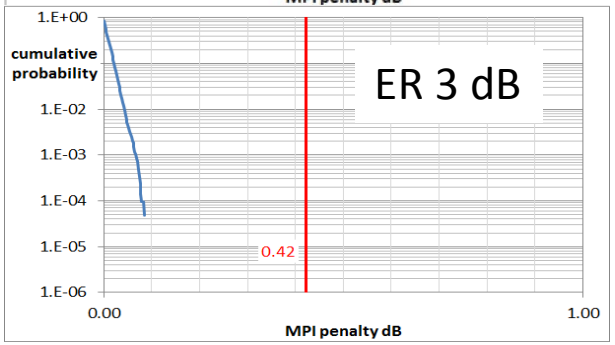




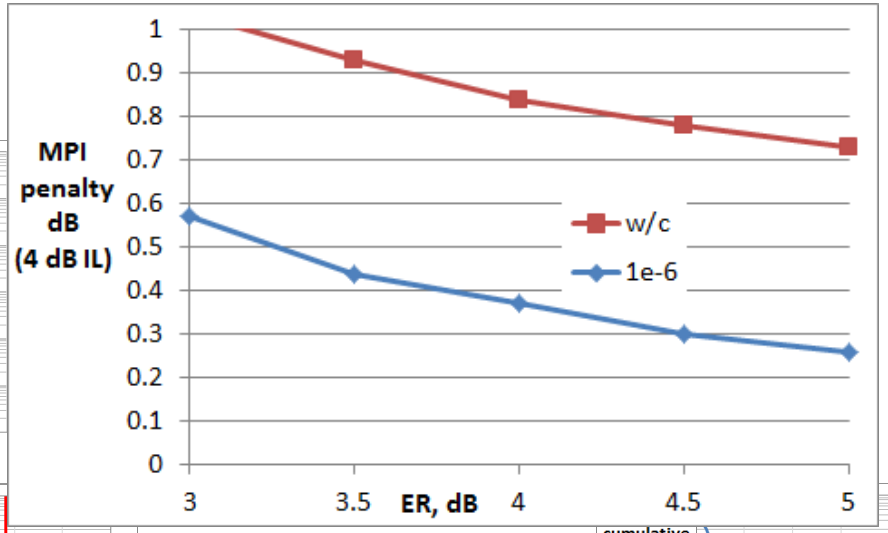


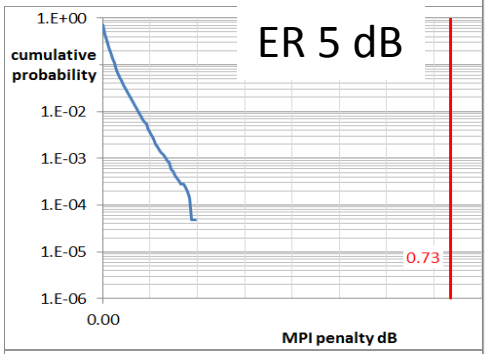
MPI penalty increase is 0.03 dB for ER = 3.5 dB (from ER = 5 dB)

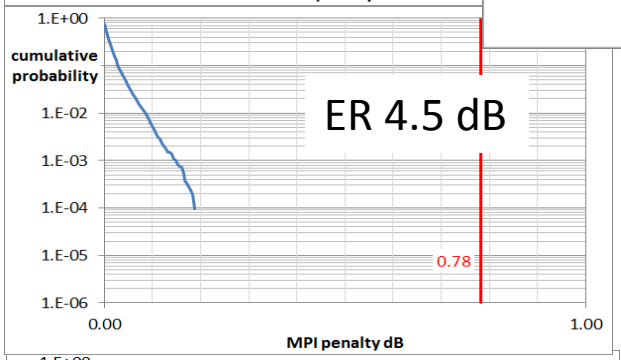


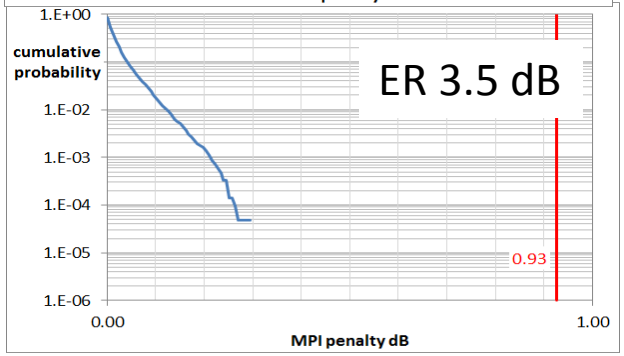


MPI penalty vs ER (4 dB IL, 4x35 dB RL)

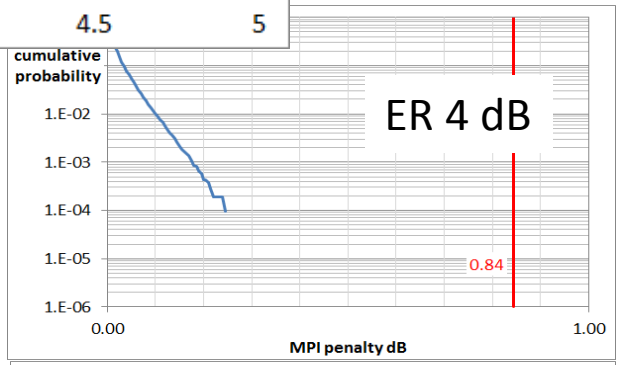


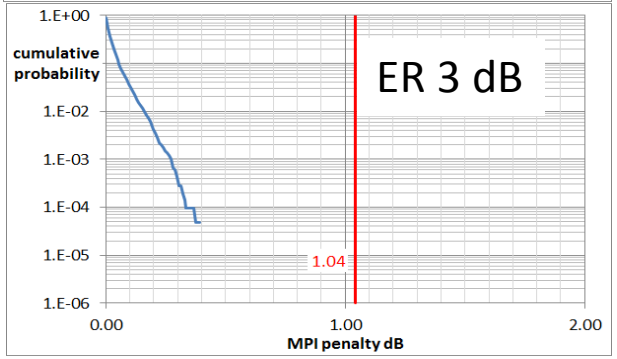






MPI penalty increase is 0.12 dB for ER = 3.5 dB (from ER = 4.5 dB)





Notes and proposals

- Directly modulated lasers (DMLs) are viable technology for the single lane 50Gb/s PAM4 transmitter, and offer a potentially lower cost/power implementation.
- For 50GBASE-FR, decrease the ER spec to 3.5 dB, to enable DML technology for single lane implementations.
  - The increase in MPI penalty for reducing ER from 4.5 dB to 3.5 dB is 0.12dB
- DML technology is likely to be viable for 100Gb/s PAM4 transmitters within a few years, within the life of the 100GBASE-DR standard.
- For 100GBASE-DR, decrease the ER spec to 3.5 dB, to enable future DML technology for single lane implementations.
  - The increase in MPI penalty for reducing ER from 4.5 dB to 3.5 dB is 0.03 dB

Comments against 802.3cd D1.2

- In section 139.6.1, Table 136-6 reduce minimum ER to 3.5 dB
- In section 140.6.1, Table 140-6 reduce minimum ER to 3.5 dB

- No changes to the 'Average launch power, max' or 'Average received power, max' specs

Back up

Connector RL tables for *DR PMDs

Table 121–15—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance
1	–37 dB
2	–42 dB
4	–45 dB
6	–47 dB
8	–48 dB
10	–49 dB

Table 124–13—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance
1	–37 dB
2	–42 dB
4	–45 dB
6	–47 dB
8	–48 dB
10	–49 dB

Table 140–13—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance
	100GBASE-DR
1	–37 dB
2	–42 dB
4	–45 dB
6	–47 dB
8	–48 dB
10	–49 dB

Table 139–14—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance	
	50GBASE-FR	50GBASE-LR
1	–25 dB	–22 dB
2	–31 dB	–29 dB
4	–35 dB	–33 dB
6	–38 dB	–35 dB
8	–39 dB	–37 dB
10	–40 dB	–38 dB