The bridge to possible

Pin Optimized PHY Interface

Call For Interest Consensus Building

Jason Potterf
Affiliated with Cisco
November 12, 2024

Supporters and Contributors

- Tim Baggett – Microchip Technology
- TJ Houck – Marvell
- Chad Jones – Cisco
- Peter Jones – Cisco
- Ragnar Jonsson – Marvell
- Jon Lewis – Dell Technologies
- Brett McClellan – Marvell
- Brian Murray – Analog Devices
- Alireza Razavi – Marvell
- Mehmet Tazebay – Broadcom
- Max Turner – Ethernovia
- Bob Voss – Panduit
- Peter Wu – Marvell
- George Zimmerman – CME Consulting / ADI, APL Group, Cisco, Marvell, OnSemi, Sony, SenTekse

CFI Announcement

This is a call for interest to initiate a Study Group to develop a PAR and CSD for an Ethernet Media Independent Interface (MII) optimized for an exposed interconnect, e.g., chip-to-chip. The growing body of IEEE 802.3 Copper PHY standards that operate at lower speeds has intensified the demand for a modern, optimized MII. Application of PHYs such as 10BASE-T1L, 10BASE-T1S, proposed 100BASE-T1L, proposed 10BASE-T1M, and potentially future PHYs would see benefit in both single and multi-port implementations. Such an effort may afford reduced pin count and implementation complexity while enabling data for multiple ports on a single interface and support for features such as PHY-Level Collision Avoidance (PLCA). Most importantly, it could provide a modern alternative interface for PHYs that would otherwise use various industry specifications not currently in IEEE Std 802.3.

CFI Consensus Building Agenda

- Brief History of Ethernet MII Solutions
- Motivating Factors in 802.3da and 802.3dg that Require a new MII
- Market Considerations
- Possible Path Forward
- Discussion and Straw Polls

Brief History of Ethernet MII Solutions

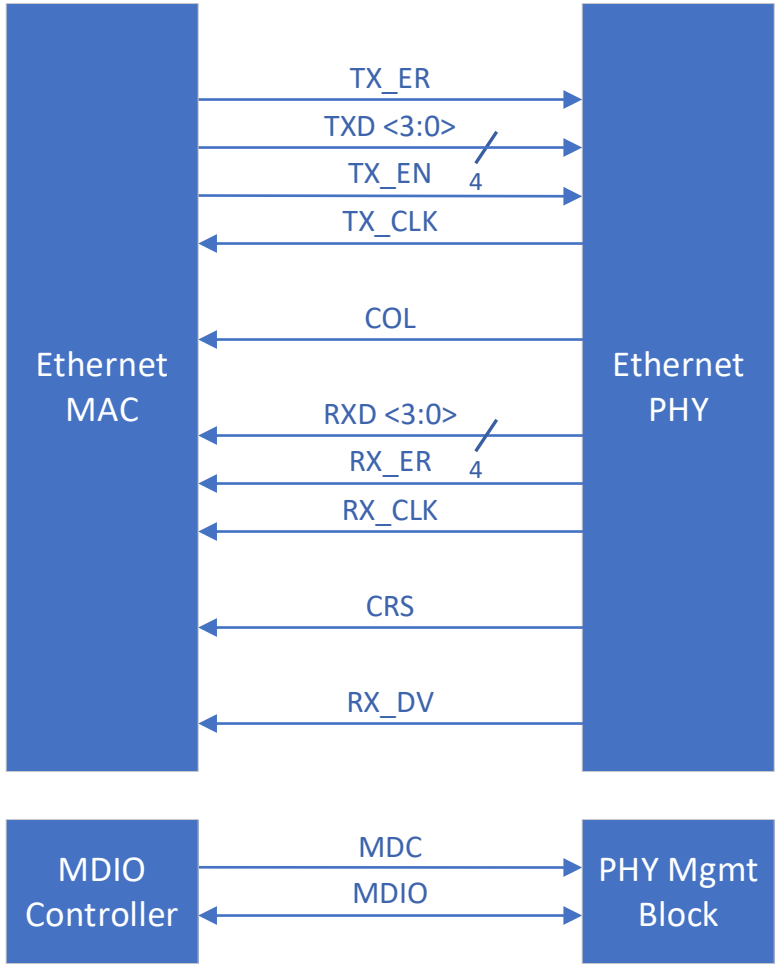
IEEE 802.3 Copper PHYs

- 802.3 is still developing new copper PHY standards
- In the past decade, half of the copper PHY projects have focused on rates **below** 1 Gbit
- 802.3 has not defined a new MII for these low-speed PHYs since 1995
- Multiple industry specs have attempted to fill some gaps, but significant deficiencies remain

Project	802.3 Clause(s)	PHY	Line Speed
802.3i-1990	14	10BASE-T	10 Mbit
802.3az-2010	14	10BASE-Te	10 Mbit
802.3u-1995	21,24,25	100BASE-T (TX)	100 Mbit
802.3ab-1999	40	1000BASE-T	1 Gbit
802.3an-2006	55	10GBASE-T	10 Gbit
802.3bp-2016	97	1000BASE-T1	1 Gbit
802.3bq-2016	113	25GBASE-T	25 Gbit
	113	40GBASE-T	40 Gbit
802.3bw-2015	96	100BASE-T1	100 Mbit
802.3bz-2016	126	2.5GBASE-T	2.5 Gbit
	126	5GBASE-T	5 Gbit
802.3cg-2019	146	10BASE-T1L	10 Mbit
	147	10BASE-T1S	10 Mbit
802.3ch-2020	149	2.5GBASE-T1	2.5 Gbit
	149	5GBASE-T1	5 Gbit
	149	10GBASE-T1	10 Gbit
802.3da-20xx	168	10BASE-T1M	10 Mbit
802.3dg-20xx	xx	100BASE-T1L	100 Mbit
802.3dm-20xx	xx	TBD	Asymmetric

IEEE 802.3
Clause 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

MII Score Card	
Max Data Rate	100 Mbit/s
Signal Count	16 Data + 2 Mgmt
Bus Max Clock Rate	25 MHz
Clock Scheme	PHY Synchronous
Command Space	4-bit
Commands Assigned	Tx - 4/16, Rx - 5/16
PLCA Support	Yes, Beacon and Commit



MII Commands

- Cause Transmission or Indicate Reception of something other than valid data bytes on the wire
- Uses TX_EN / TX_ER / RX_En / RX_ER to create address space
- Currently Defined in 802.3 Clause 22
  - Assert LPI
  - PLCA Beacon Request / Indication
  - PLCA Commit Request / Indication
  - False Carrier Indication

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	0100 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

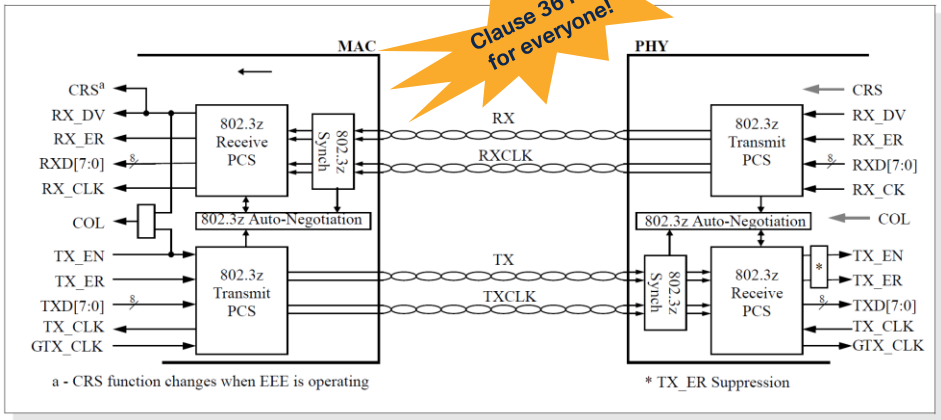
Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON indication
0	1	0011	PLCA COMMIT indication
0	1	0100 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

Cisco Specification
Serial-GMII (aka SGMII)

MII Score Card	
Max Data Rate	1000 Mbit/s
Signal Count	4/port + 2 Mgmt
SerDes Max Rate	1.25 Gbps
Clock Scheme	SerDes or Source Sync
Command Space	Large – Ordered Sets
Commands Assigned	8 Non-Idle Sets Defined
PLCA Support	No

System Diagrams (SGMII Spec)



PCS Scheme (Clause 36)

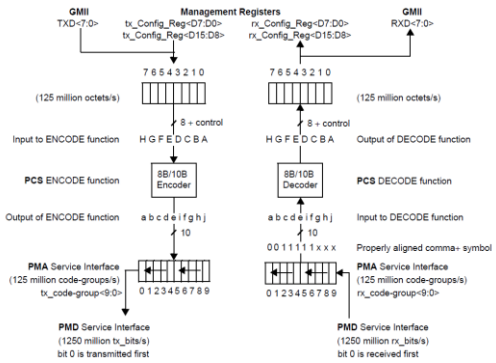


Figure 36–3—PCS reference diagram

Commands (Clause 36)

Table 36–3—Defined ordered sets

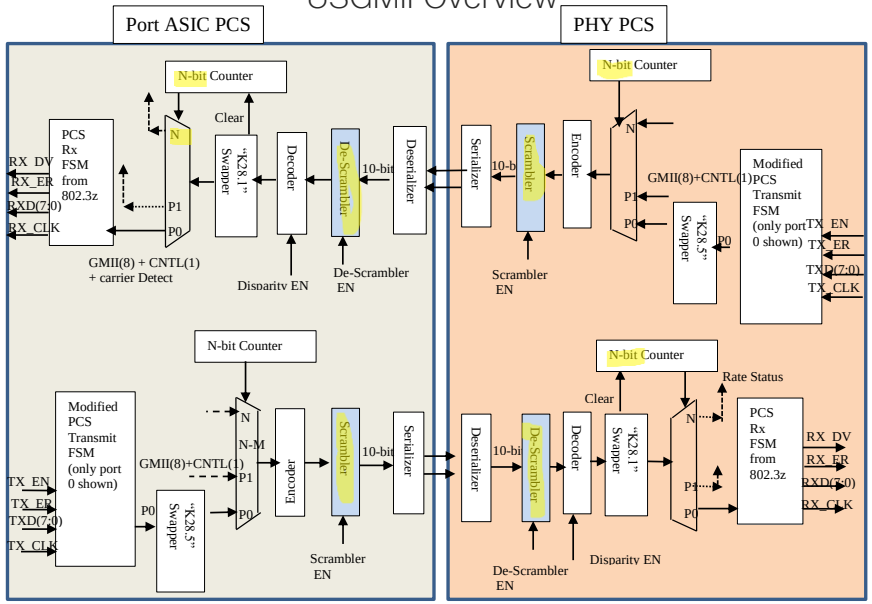
Code	Ordered Set	Number of Code-Groups	Encoding
/C/	**Configuration**		Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg[a]
/C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg[a]
/I/	**IDLE**		Correcting /I1/, Preserving /I2/
/I1/	IDLE 1	2	/K28.5/D5.6/
/I2/	IDLE 2	2	/K28.5/D16.2/
	Encapsulation		
/R/	Carrier_Extend	1	/K23.7/
/S/	Start_of_Packet	1	/K27.7/
/T/	End_of_Packet	1	/K29.7/
/V/	Error_Propagation	1	/K30.7/
/LI/	**LPI**		Correcting /LI1/, Preserving /LI2/
/LI1/	LPI 1	2	/K28.5/D6.5/
/LI2/	LPI 2	2	/K28.5/D26.4/

[a]Two data code-groups representing the Config_Reg value.

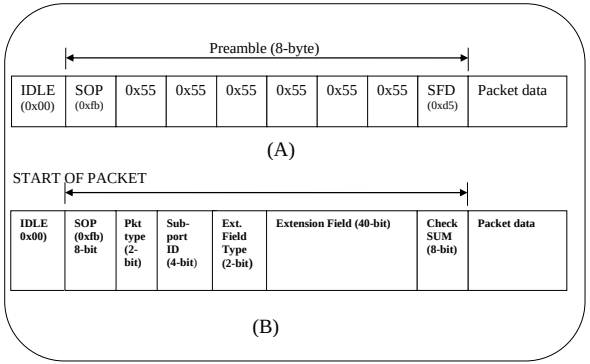
Cisco Specification
Universal Serial GMII (aka USGMII)

MII Score Card	
Max Data Rate	1000 Mbit/s, with 8, 4, and 1 Port Modes
Signal Count	4/Octal PHY + 2 Mgmt
SerDes Max Rate	10.0, 5.0, 1.25 Gbps
Clock Scheme	SerDes
Command Space	Large – Ordered Sets Packet Control Header
Commands Assigned	K28.1 Reserved 8 Non-Idle Sets Defined PCH Packet Types
PLCA Support	No

USGMII Overview



Packet Control Header



PCH Packet Types

00: Ethernet Packet with PCH
01: Ethernet packet, without PCH (packet information)
10: Idle Packet – Contains status data for a port – no packet data
11: Preemption Frame, aka Interspersing Express Traffic (IET) frame

In-Band PTP Timestamps via Extension Field

MII Evolution Summary

IEEE and Common Industry MII Specifications

	Max Data Rate	Signal Count	Bus Max Rate	Clock Scheme	Command Space	Commands Assigned	PLCA
MII	100 Mbit/s	16 Data + 2 Mgmt	25 MHz	PHY Synchronous	4-bit	Tx - 4/16, Rx – 5/16	Yes
RMII *	100 Mbit/s	7 Data + 1 Clk + 2 Mgmt	50 MHz	System Synchronous	2-bit	Tx - 2/4, Rx – 2/4 (Note 1)	No
GMII	1,000 Mbit/s	25 Data + 2 Mgmt	125 MHz	Source Synchronous	8-bit	Tx - 4/256, Rx – 5/256	No
RGMII *	1,000 Mbit/s	12 Data + 2 Mgmt	125 MHz	Source Synchronous DDR	8-bit	Tx - 2/256, Rx – 4/256	No
SMII *	100 Mbit/s	2/port + 2-5/PHY + 2 Mgmt	125 MHz	System or PHY Synchronous	8-bit bitfield	Tx - 5/8, Rx – 7/8 bits	No
SGMII *	1,000 Mbit/s	4/port + 2 Mgmt	1.25 Gbps	SerDes or Source Sync	K-Code Ordered Sets	8 Non-Idle Sets Defined	No
QSGMII *	1,000 Mbit/s (4 Ports)	4/Quad Phy + 2 Mgmt	5.0 Gbps	SerDes	K-Code Ordered Sets	K28.1 Reserved 8 Non-Idle Sets Defined	No
USGMII *	1,000 Mbit/s (8, 4, and 1 Port Modes)	4/Octal PHY + 2 Mgmt	10.0, 5.0, 1.25 Gbps	SerDes	K-Code Ordered Sets Packet Control Header	K28.1 Reserved 8 Non-Idle Sets Defined PCH Packet Types	No
XGMII	10,000 Mbit/s	72 Data + 2 Clk + 2 Mgmt	156.25 Mhz	Source Synchronous DDR	8-bit Bus Command Sequence Ordered Sets	Tx - 8/256, Rx - 8/256 Seq Ord Sets - 4/256	No
XAUI	10,000 Mbit/s	16 Data + 2 Mgmt	3.125 Gbps	SerDes	K-Code Ordered Sets Sequence Ordered Sets	Tx - 8/256, Rx - 8/256 Seq Ord Sets - 4/256	No
USXGMII *	10,000 Mbit/s (8, 4, 2, and 1 Port Modes)	4/Octal PHY + 2 Mgmt	20.625 Gbps	SerDes	K-Code Ordered Sets Packet Control Header	Seq Ord Sets - 4/256 PCH Packet Types	No

* Industry specification created outside of IEEE

See https://www.ieee802.org/3/dg/public/May_2022/potterf_3dg_01_012524.pdf for a detailed review of past industry-specified MIIs

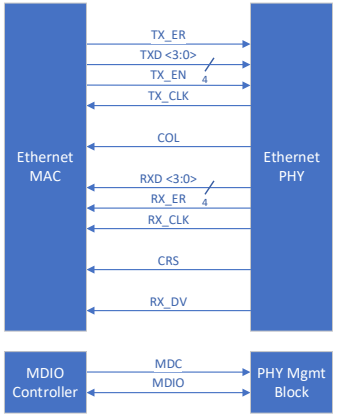
Motivating factors in 802.3da and 802.3dg that prompt considering a new IEEE PHY Interface specification

Common Factors

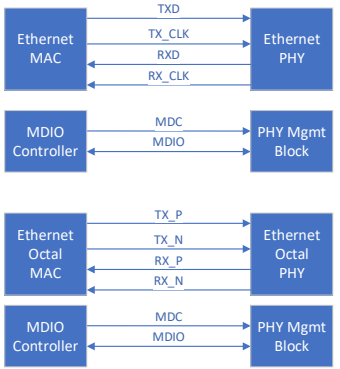
- Pin Count Reduction
  - Industry MII specifications have one common thread – *fewer pins*
  - Current SPE solutions (SPI, 3-Pin) address the MAC interface or PHY PMD and thus do not solve the challenges in front of our current SPE projects
  - Pin count reduction is also beneficial to already defined PHY standards such as 10BASE-T1L, 10BASE-T1S, 10BASE-T, and 100BASE-TX PHYs

New PHY Interface Pin Count Reduction Goals

IEEE 802.3 MII Current Solution

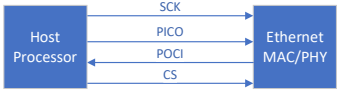


Possible IEEE Outcome

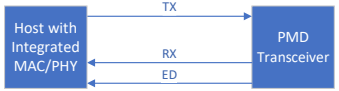


Current SPE Ecosystem Industry Specifications

Open Alliance
10BASE-T1x
MAC-PHY Serial Interface



Open Alliance
10BASE-T1S
PMD Transceiver Interface



IEEE 802.3dg & 802.3da Motivating Factors

802.3dg 100 Mbps Long-Reach Single Pair Ethernet Benefits

- 802.3dg should provide a *modern* single-port solution for 100 Mbps data rates
  - SPI solution for 10 Mbps no longer works at 100 Mbps
  - Three-Pin PMD interface also is problematic at 100 Mbps
- Switch implementations desperately need a simpler multi-port solution
  - Existing multi-port MII solutions require a 10 Gbps SerDes which is overly complex

802.3da 10 Mbps Single Pair Multidrop Segments Enhancement Benefits

- PLCA over MII presents implementation challenges
- Multi-port MII solutions requiring a 10 Gbps SerDes are even less appropriate for 10 Mbps PHY implementations

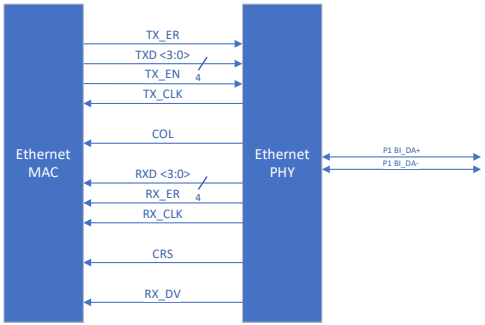
Future Projects

- Existing IEEE and industry specified MII solutions are adequate for 1 Gbit/s and faster
  - Widely implemented
  - Minimal benefit to optimizing for this use case
- Asymmetric PHY projects could benefit from a reduced pin count solution with adaptive rates

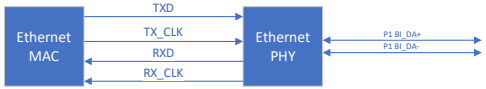
Market Considerations

Enable efficient, adoptable SPE implementations

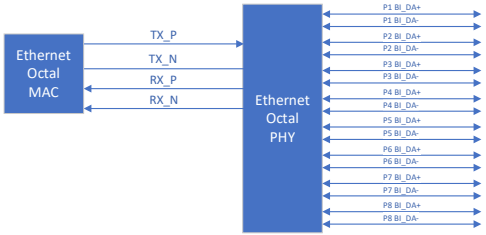
IEEE 802.3 MII
MII:MDI Ratio = 8:1



Potential Single-Port MII
MII:MDI Ratio = 2:1



Potential Multi-Port MII
MII:MDI Ratio = 1:4



A reduced pin count chip-to-chip interface provides more value per IC package pin than an MII-based solution, reducing implementation complexity and encouraging adoption

Market for 10/100 PHYs Could Benefit

- Small processors frequently do not embed PHYs but instead provide a chip-to-chip MII interface
- There is still a large market for single-port 10/100 PHYs that is underserved by existing industry specifications
  - IEEE MII – Too pin-intensive
  - RMII – Half the pins, but still but room for improvement
  - SPI Connected MAC/PHY – Performance suffers in many applications
- Small devices multiplex pins, so choosing to adopt Ethernet instead of legacy serial buses carries a significant opportunity cost

Single-Pair Ethernet Adoption Accelerator

- PHY interconnect complexity for switches is hindering adoption
- Available MII interfaces prevent efficient implementation of 802.3cg 10-BASET1S and 10-BASET1L switches
- Octal PHY Implementation Options for 80 Mbit/s total bandwidth
  - MII – 16 pins / port x 8 ports + 2 Mgmt = *130 Pins*
  - RMII – 8 pins / port x 8 ports + 2 Mgmt = *66 Pins*
  - SGMII – 32 pins + 2 Mgmt = 34 pins and *eight 1 Gbps SerDes*!
  - USGMII – 4 pins + 2 Mgmt = 6 pins, but requires a *10 Gbps SerDes*!

Possible Path Forward

Path Forward – Identified Goals

Goals to Achieve

- Reduce pin count
- Reduce interface speed
- Enable both single and multi-port PHYs
- Provide support for SPE-specific features such as PLCA

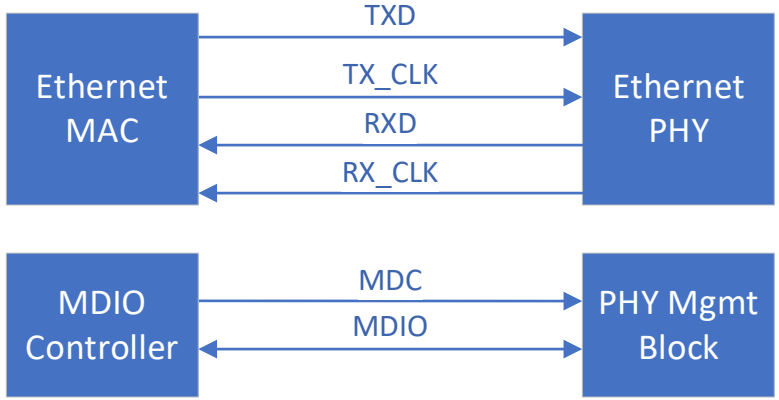
Outcomes to Avoid

- Avoid requiring a SerDes for single-port MIIs
- Avoid complex interfaces and excessive feature sets
- Avoid precluding features required by one SPE PHY to support or expedite another

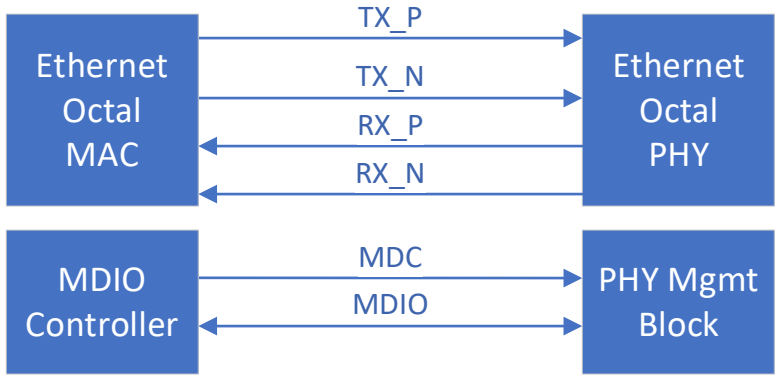
Proposal
SPE-SMII and SPE-MP-SMII

MII Score Card	
Max Data Rate	100 Mbit/s, with 8 and 1 Port Modes
Signal Count	4 per PHY + 2 Mgmt
Clock Scheme	SP –125 MHz Source Sync Clock MP – 1.0 Gbps SerDes
Command Space	K-Code Ordered Sets
Features	PTP Timestamping Preemption EEE PLCA

Single-Port Configuration



Multi-Port Configuration



Issues for Study Group to Consider

Scope Issue 1 – PLCA RS

- In theory, the Reconciliation Sublayer (RS) controls the PHY's PLCA-related actions from the host side of the MII
- In practice, backwards compatibility with non-PLCA MCUs in the market has driven PLCA into the PHY
- Standardized registers to manage PLCA-aware PHYs could be of value as part of the 802.3 standard

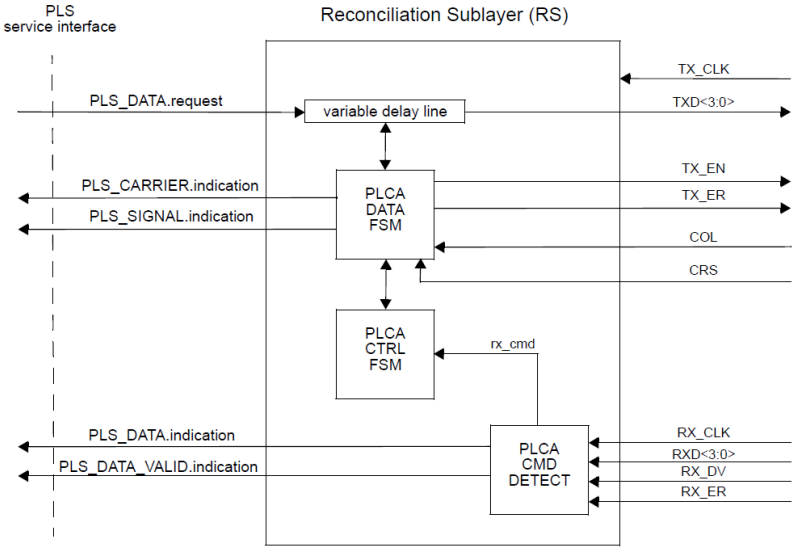
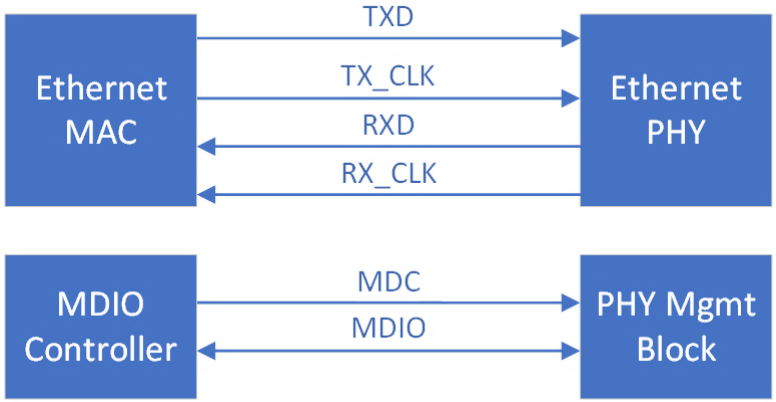


Figure 148–2—PLCA functions within the Reconciliation Sublayer (RS)

Scope Issue 2 – Single Port Interfaces

- Single Port Reduced Pin Interface
  - Complements Open Alliance Specs
    - SPI MAC/PHY Serial Interface
    - Three-Pin PMD Interface
  - More useful in 802.3dg than 802.3da due to ease of integration of a 10BASE-T1S PHY in an MCU with external PMD
  - Could be useful for 4-pair 10/100 PHYs as well

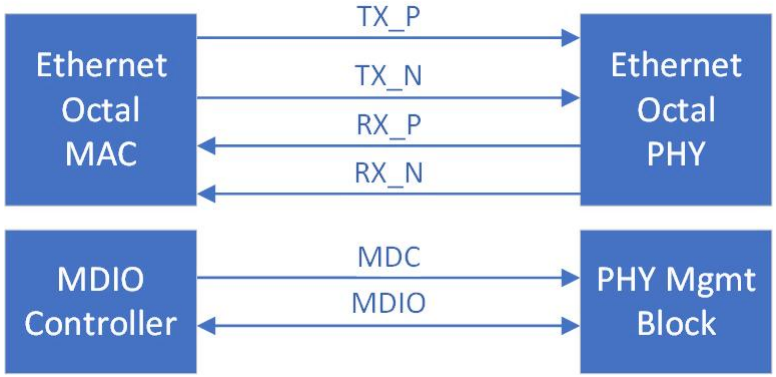
Single-Port Configuration



Scope Issue 3 – Multi-Port Interfaces

- Features to Consider
  - Slow SerDes / No SerDes
  - Variable Port Mux Ratio
    - 1-8 Ports / Interface
  - Embedded MDIO
  - Ordered Sets for Control
    - PLCA, LPI, Faults, Collisions, etc.
  - PTP Timestamping
  - Preemption
  - Collision Tracing

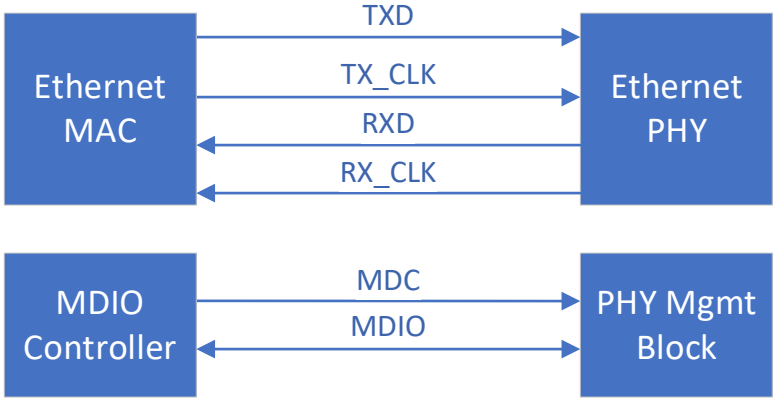
Multi-Port Configuration



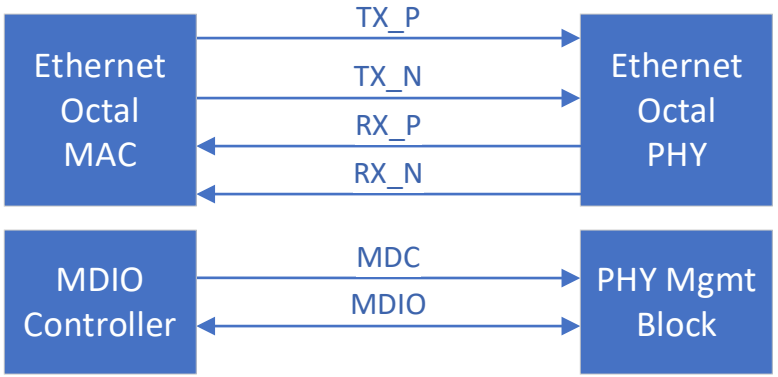
Scope Issue 4 – One Solution or Two

- Should we have a single logical solution that scales from single to multi-port?
- Should we allow multiple electrical interfaces to enable hardware optimization?
- See following slides for an example of a single logical solution…

Single-Port Configuration



Multi-Port Configuration



Discussion and Straw Polls

Proposed
Pin Optimized PHY Interface
Study Group Motion

Move that the IEEE 802.3 Working Group request the formation of a Study Group to develop a Project Authorization Request (PAR) and Criteria for Standards Development (CSD) responses for an Ethernet Media Independent Interface (MII) optimized for an exposed interconnect.

Straw Poll Question # 1

Should a study group be formed to develop a PAR, CSD responses, and objectives for “Pin Optimized PHY Interface”?

- ❑Yes
- ❑No
- ❑Abstain

Straw Poll Question # 2

Would you participate in the "Pin Optimized PHY Interface" Study Group in IEEE 802.3?

- ❑ Yes
- ❑ No
- ❑ Abstain

Straw Poll Question # 3

Do you believe your affiliation would support your participation in the "Pin Optimized PHY Interface" Study Group in IEEE 802.3?

- ❑Yes
- ❑No
- ❑Abstain

Supporting Material

Previous MII Straw Poll Results

Feature Requirement Straw Poll Results Summary

Features	Mandatory	Optional	Omit	Abstain
Control Bandwidth Reservation	15	2	3	13
Embedded MDIO	16	5	3	10
PTP Timestamping	14	9	1	10
Frame Preemption (802.1Q IET)	9	4	1	18
Energy Efficient Ethernet (LPI)	15	8	0	8
Four-Pair 10/100 PHY Compatibility	15	2	2	15
Half-Duplex Operation (COL)	15	4	2	11
Half-Duplex Late Collision Frame Correlation	4	4	4	24
PLCA Support	13	1	1	17

Options: Mandatory Feature, Optional Feature, Omit Feature

Previous MII Presentations

Previous MII-Related Presentations in 802.3dg

Title	Author	Affiliation	Presentation Date
Modifications to Constant Latency MII Encoding and Ordered Sets Onto 8N/(8N+1) encoder	William Lo	Axonne	Sept 16, 2024 – IEEE 802.3 Interim
Progressing the MII discussion	Jason Potterf	Cisco Systems	July 15, 2024 – IEEE 802 Plenary
Constant Latency MII Encoding and Ordered Sets Onto 8N/(8N+1) encoder (01a)	William Lo	Axonne	July 15, 2024 – IEEE 802 Plenary
Ethernet MII Interfaces Refinement of Previous Proposals (LATE – updated with straw polls)	Jason Potterf	Cisco Systems	March 11, 2024 – IEEE 802 Plenary
MII to SMII Proposal	William Lo	Axonne	March 11, 2024 – IEEE 802 Plenary
Adding Sequence Ordered Set to MII	William Lo	Axonne	March 11, 2024 – IEEE 802 Plenary
802.3 MII Options - Past, Present, and Proposals for the Future	Jason Potterf	Cisco Systems	January 25, 2024 – IEEE 802.3 Interim
Enhanced SMII Proposal	William Lo	Axonne	November 15-16, 2023 – IEEE 802 Plenary
Further Consideration on the new MII	Tingting Zhang, Dongcheng Pan,Yan Zhuang	Huawei	September 13, 2023 – IEEE 802.3 Interim
Thoughts on the new MII	Dongcheng Pan, Tingting Zhang, Yan Zhuang	Huawei Technologies	July 11, 2023 – IEEE 802 Plenary
IEEE 802.3dg – Need for a new MII? (revised v1p1)	Piergiorgio Beruto	On Semiconductor	May 17, 2023 – IEEE 802.3 Interim