OAM for 802.3cg 10BASE-T1S

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147.3.8 Operations, Administration, and Maintenance (OAM)

The 10BASE-T1S PCS level Operations, Administration, and Maintenance (OAM) provides an optional mechanism for exchanging information between PHYs for various purposes. The 10BASE-T1S OAM information is exchanged in-band between two PHYs by replacing 15 bits in the preamble starting at the 34th bit. The 10BASE-T1s OAM is strictly between two 10BASE-T1s PHYs on the physical layer and their associated management entities if present. Passing 10BASE-T1S OAM information to other layers is outside the scope of this standard.

The 10BASE-T1S OAM is operational as long as both PHYs implement this mechanism and the link is up.

147.3.8.1 Definitions

10BASE-T1S OAM frame: A frame consisting of 1 octets of data, an acknowledge bit, and 6-bit CRC6 which is 4B5B encoded and DME modulated.

10BASE-T1S OAM symbol: An 8-bit symbol consisting of one data octet plus a parity bit.

10BASE-T1S OAM message: A message contains a single 1 octet OAM symbol of message data embedded in a 10BASE-T1S OAM frame. The same 10BASE-T1S OAM message shall be repeated on multiple 10BASE-T1S OAM frames.

147.3.8.2 Functional Specifications

147.3.8.2.1 OAM Message Structure

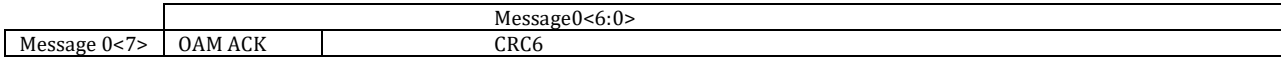

Figure 147-xx

The OAM Message structure is as shown in Figure 147-xx. It consists of a 1 octet Message0, an OAM ACK bit, and a CRC6.

147.3.8.2.4 10BASE-T1S OAM Message Data

The 10BASE-T1S OAM message data is indicated in OAM bits 7:0. The OAM frame maps to the PCS variables oam_txdata and oam_rxdata as specified in 147.3.3.1 and 147.3.2.2.

The octet message data is user-defined and its definition is outside the scope of this standard.

Ack is set by the PHY to let the link partner know that the 10BASE-T1S OAM frame sent by the link partner is successfully received as defined in 147.3.8.2.6.

147.3.8.2.5 CRC6

The CRC6 is indicated in OAM bits 9:15

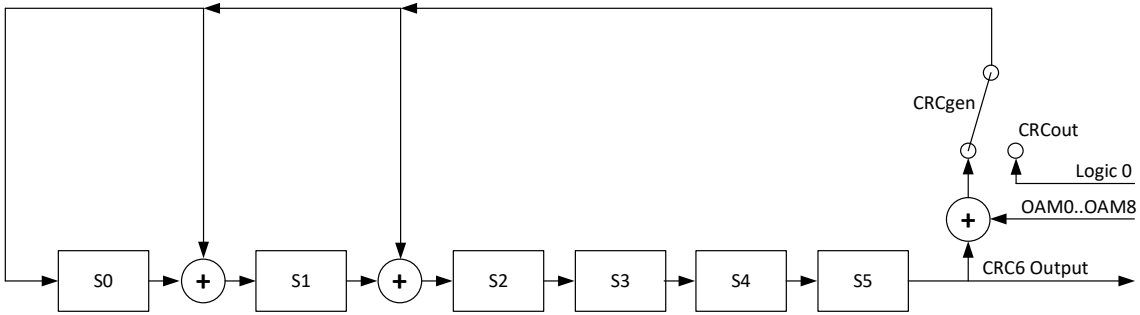

Figure 147-x CRC6

The CRC6 implements the polynomial x^6+x^2+x+1 of the previous 9 bits. The CRC6 shall produce the same result as the implementation shown in figure 147-xx. The 6 delay elements S0,…,S5 shall be initialized to zero. Afterwards the 9 data bits are used to compute the CRC6 with the switch connected (setting CRCgen). After all 9 data bits have been processed, the switch is disconnected (setting CRCout) and the 6 values stored in the delay elements are ordered as illustrated, first S5 followed by S4, then S3, S2, S1 and the final value S0.

147.3.8.2.6 Frame acceptance criteria

All bits of the OAM frame shall be accepted and updated unless the CRC6 is incorrect.

147.3.8.2.7 10BASE-T1S OAM Message Exchange

The 10BASE-T1S OAM message exchange mechanism allows a management entity attached to a PHY and its peer attached to the link partner to asynchronously pass 10BASE-T1S OAM messages and verify their delivery if both PHYs implement this mechanism.

The 10BASE-T1S OAM message is first written into the 10BASE-T1S OAM transmit register 3.2295.7:0 in the PHY. The 10BASE-T1S OAM message is then read out of the 10BASE-T1S OAM transmit register and transmitted to the link partner. After the link partner receives the 10BASE-T1S OAM message it transfers it into the link partner's 10BASE-T1S OAM receive register and also sends an acknowledge back to the PHY indicating that the next 10BASE-T1S OAM message can be transmitted. The transfers between the management entities can be done asynchronously. On the transmit side mr_tx_valid = 0 indicates that the next 10BASE-T1S OAM message can be written into the 10BASE-T1S OAM transmit register. Once the register are written the management entity sets mr_tx_valid to 1 to indicate that the 10BASE-T1S OAM transmit register contains a valid 10BASE-T1S OAM message. Once the message is read out, the state machine clears the mr_tx_valid to 0 to indicate that the register are ready to accept the next 10BASE-T1S OAM message.

On the receive side mr_rx_lp_valid indicates that valid 10BASE-T1S OAM message can be read from the 10BASE-T1S OAM receive register. Once these register are read, the mr_rx_lp_valid should be cleared to 0 to indicate that the register is ready to receive the next 10BASE-T1S OAM message. If mr_rx_lp_valid is not cleared then the 10BASE-T1S OAM message transfer will eventually stall since the sender cannot send new 10BASE-T1S OAM messages if the receiver does not acknowledge that an 10BASE-T1S OAM message has been transferred into the 10BASE-T1S OAM receive register, and the previous message will be resent.

The management entities can asynchronously read mr_tx_valid and mr_rx_lp_valid to know when 10BASE-T1S OAM messages can be transferred in and out of the 10BASE-T1S OAM register.

Table 147-x State Variables to 10BASE-T1S OAM Register Mapping

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
10BASE-T1S OAM Message Valid	10BASE-T1S OAM Transmit Register	3.2294.15	mr_tx_valid
10BASE-T1S OAM Message Received	10BASE-T1S OAM Transmit Register	3.2294.13	mr_tx_received
10BASE-T1S OAM Message 0	10BASE-T1S OAM Message Register	3.2295.7:0	mr_tx_message[7:0]
Link Partner 10BASE-T1S OAM Message Valid	10BASE-T1S OAM Link Partner Receive Register	3.2299.15	mr_rx_lp_valid
Link Partner 10BASE-T1S OAM Message 0	10BASE-T1S OAM Link Partner Message Register	3.2300.7:0	mr_rx_lp_message[7:0]

147.3.8.3 Variables

147.3.8.3 OAM Message Fields Description

mr_rx_lp_message[7:0]

Single octet 10BASE-T1S OAM message from the link partner. The value in this variable is valid only when mr_rx_lp_valid is 1

mr_rx_lp_valid

Indicates whether 10BASE-T1S OAM message in mr_rx_lp_message[7:0],
is valid or not. The clearing of this variable indicates to the state machine that the 10BASE-T1S OAM
message is read by the user and the state machine can proceed to load in the next 10BASE-T1S
OAM message.

Values:

- 0: invalid
- 1: valid

mr_tx_message[7:0]

Single octet 10BASE-T1S OAM message transmitted by the local PHY. The value in this variable
is valid only when mr_tx_valid is 1.

147.3.8.3 continued

mr_tx_valid

Indicates whether 10BASE-T1S OAM message in mr_tx_message[7:0] is valid or not. This register will be cleared by the state machine to indicate whether the next 10BASE-T1S OAM message can be written into the registers.

Reset

Values:

false: 10BASE-T1S OAM circuit not in reset

true: 10BASE-T1S OAM circuit is in reset

rx_ack

Acknowledge from link partner in response to PHY's 10BASE-T1S OAM message.

Values:

0: no acknowledge

1: acknowledge

rx_lp_ack

Acknowledge from PHY in response to link partner's 10BASE-T1S OAM message. Indicates whether valid 10BASE-T1S OAM message from the link partner has been sampled into the PHY's registers.

Values:

0: no acknowledge / not sampled

1: acknowledge / sampled

147.3.8.3 continued

rx_oam<7:0>

Raw 10BASE-T1S OAM frame received from the link partner.

tx_oam<7:0>

Raw 10BASE-T1S OAM transmitted from the PHY to the link partner.

Table 45-220f

Table 45–220f—10BASE-T1S OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2294.15	10BASE-T1S OAM message valid	This bit is used to indicate message data in registers [redacted], 3.2295, [redacted] are valid and ready to be loaded. This bit shall self clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2294.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2294.13	10BASE-T1S OAM message received	This bit shall self clear on read. 1 = 10BASE-T1S OAM message received by link partner 0 = 10BASE-T1S OAM message not received by link partner	RO, LH
3.2294.12	Reserved	Toggle value of message that was received by link partner as indicated in 3.2294.13.	RO
3.2294.11:8	Message number	User-defined message number to send	R/W
3.2294.7:4	Reserved	Value always 0	RO
3.2294.3	Reserved	Value always 0	RO
3.2294.2			R/W
3.2294.1:0			RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

- 45.2.3.58f.15 10BASE-T1S OAM message valid (3.2294.15) Bit 3.2294.15 shall be set to one when the 10BASE-T1S OAM message to be transmitted in register 3.2295 is properly configured to be transmitted. This register shall be cleared by the state machine to indicate whether the next 10BASE-T1S OAM message can be written into the registers.

Table 45-220g

Table 45–220g—10BASE-T1S OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2295.15:8	Reserved	Value always 0	R/W
3.2295.7:0	10BASE-T1S OAM message 0	Message octet 0. LSB transmitted first.	R/W
~~3.2296.15:8~~	~~10BASE-T1S OAM message 3~~	~~Message octet 3. LSB transmitted first.~~	~~R/W~~
~~3.2296.7:0~~	~~10BASE-T1S OAM message 2~~	~~Message octet 2. LSB transmitted first.~~	~~R/W~~
~~3.2297.15:8~~	~~10BASE-T1S OAM message 5~~	~~Message octet 5. LSB transmitted first.~~	~~R/W~~
~~3.2297.7:0~~	~~10BASE-T1S OAM message 4~~	~~Message octet 4. LSB transmitted first.~~	~~R/W~~
~~3.2298.15:8~~	~~10BASE-T1S OAM message 7~~	~~Message octet 7. LSB transmitted first.~~	~~R/W~~
~~3.2298.7:0~~	~~10BASE-T1S OAM message 6~~	~~Message octet 6. LSB transmitted first.~~	~~R/W~~

[a]R/W = Read/Write

Delete OAM registers 3.2296,3.2297,3.3.2298

45.2.3.58g 10BASE-T1S OAM message register (Register 3.2295)
The 10BASE-T1S OAM message register bits 7:0 contains the 1 octet 10BASE-T1S OAM message data to be transmitted. The 1 octet message data is user defined and its definition is outside the scope of this standard. See Table 45–220g. Change 3.2295.15:8 to ‘Reserved’

Table 45-220h

Table 45–220h—Link partner 10BASE-T1S OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2300.15:8	Reserved.	Reserved.	RO
3.2300.7:0	Link partner 10BASE-T1S OAM message 0	Message octet 0. LSB received first.	RO
~~3.2301.15:8~~	~~Link partner 10BASE-T1S OAM message 3~~	~~Message octet 3. LSB received first.~~	~~RO~~
~~3.2301.7:0~~	~~Link partner 10BASE-T1S OAM message 2~~	~~Message octet 2. LSB received first.~~	~~RO~~
~~3.2302.15:8~~	~~Link partner 10BASE-T1S OAM message 5~~	~~Message octet 5. LSB received first.~~	~~RO~~
~~3.2302.7:0~~	~~Link partner 10BASE-T1S OAM message 4~~	~~Message octet 4. LSB received first.~~	~~RO~~
~~3.2303.15:8~~	~~Link partner 10BASE-T1S OAM message 7~~	~~Message octet 7. LSB received first.~~	~~RO~~
~~3.2303.7:0~~	~~Link partner 10BASE-T1S OAM message 6~~	~~Message octet 6. LSB received first.~~	~~RO~~

[a]RO = Read only

- Delete Registers 3.2301, 3.2302, 3.2303
- Change 3.2300.15:8 to ‘Reserved’

Table 45-220i

Table 45–220i—10BASE-T1L OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2299.15	Link partner 10BASE-T1S OAM message valid	This bit is used to indicate message data in registers 3.2299.11:8, 3.2300, ~~3.2301, 3.2302, and 3.2303~~ are stored and ready to be read. This bit shall self clear when register 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2299.14	Reserved	Value always 0	RO
3.2299.13:12			RO
3.2299.11:8			RO
3.2299.7:2			RO
3.2299.1:0	Reserved	Value always 0	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.58h.1 Link partner 10BASE-T1S OAM message valid (3.2299.15) Bit 3.2299.15 shall be set to one when the 10BASE-T1S OAM message from the link partner is stored into register 3.2300. This register shall be cleared when register 3.2300 is read.

- Delete registers 3.2301, 3.2302, 3.2303 & references to these registers in the text.
- Change bits 14, 11:8, 7:2 & 1:0 to ‘Reserved’