IEEE P802.3xx™/D0.2, 14th September 2017
(Amendment of IEEE Std 802.3™-2015)

IEEE P802.3xx™/D0.2

Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation over Single Balanced Twisted-pair Cabling and Associated Power Delivery

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2015 as amended by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bp-2016, IEEE Std 802.3br-2016, IEEE Std 802.3bn-2016, IEEE Std 802.3bz-2016, IEEE Std 802.3bu-2016, and IEEE Std 802.3bv-2017. The purpose of the amendment [complete]. Draft D0.2 is prepared for [review/balloting stage]. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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Abstract: This amendment to IEEE Std 802.3-2015 specifies additions to and appropriate modifications to add 10 Mb/s Physical Layer (PHY) specifications and management parameters for operation, and associated optional provision of power, on single balanced twisted-pair copper cabling.

Keywords: 10BASE-T1; copper; Ethernet; IEEE 802.3cg™; MASTER-SLAVE; MediumDependent Interface; Physical Coding Sublayer; physical layer; Physical Medium Attachment.

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The following individuals were officers and members of the IEEE 802.3 working group at the beginning of the IEEE P802.3xx working group ballot. Individuals may have not voted, voted for approval, disapproval or abstained on this standard.

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Adam Healey, *IEEE 802.3 Working Group Vice-Chair*
Pete Anslow, *IEEE 802.3 Working Group Secretary*
Steven B. Carlson, *IEEE 802.3 Working Group Executive Secretary*
Valerie Maguire, *IEEE 802.3 Working Group Treasurer*

FirstName SecondName*, IEEE P802.3xx Task Force name Task Force Chair*
FirstName SecondName*, IEEE P802.3xx Task Force name Task Force Editor-in-Chief*

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

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Michelle D. Turner
IEEE Standards Senior Program Manager, Document Development

Jonathan Goldberg
IEEE Standards Program Manager, Technical Program Development

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Introduction

This introduction is not part of IEEE Std 802.3xx-20xx, IEEE Draft Standard for Ethernet. Amendment: Amendment title (SHALL match PAR).

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3xx-20xx publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines ser-

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vices and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw™-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by™-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq™-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp™-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br™-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn™-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

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IEEE Std 802.3bz™-2016

Amendment 7—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bu™-2016

Amendment 8—This amendment includes changes to IEEE Std 802.3-2015 to define a methodology for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single twisted-pair interfaces.

IEEE Std 802.3bv™-2017

Amendment 9—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 115 and Annex 115A. This amendment adds point-to-point 1000 Mb/s Physical Layer (PHY) specifications and management parameters for operation on duplex plastic optical fiber (POF) targeting use in automotive, industrial, home-network, and other applications.

IEEE Std 802.3-2015/Cor 1-201x

Corrigendum 1—This corrigendum clarifies which lane of the media dependent interface (MDI) of a multilane Physical Layer entity (PHY) is used as the timestamping reference point.

IEEE Std 802.3xx™-20xx

This amendment includes [complete]

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

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1. Introduction

1.3 Normative references

Insert the following references in alphanumeric order:

1.4 Definitions

Insert the 10BASE-T1 definition into the list after 1.4.9 10BASE-T: as follows:

1.4.9a 10BASE-T1: IEEE 802.3 Physical Layer specification for a 100 Mb/s Ethernet full duplex local area network over a single balanced twisted-pair. (See IEEE Std 802.3, Clause 200.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

ABBR expanded version

[abbreviations use paragraph tag AcrList,ac]

Notes for editors (not to be included in the published draft - not even D1.0!)

Version 2.9
7 April 2017

Editors should do their best to keep up to date with respect to any changes in the IEEE Standards Style Manual https://development.standards.ieee.org/myproject/Public/mytools/draft/styleman.pdf. The style manual should always be consulted for definitive guidance, except where we specifically state that we deviate from it with the agreement of the IEEE-SA Editorial Staff.

Editors should also use the spellings and conventions detailed on the 'IEEE 802.3 words and compound words' web page at http://www.ieee802.org/3/WG_tools/editorial/requirements/words.html.

The Draft version and draft date are changed in all files in the book by editing the files Draft_Version.txt and Draft_Date.txt using Notepad and then updating the book.

It is helpful for the staff applying the amendment to the base standard if the projects all use the same subdirectory structure as is used for this example set of files. All new clauses should be placed in Section_8\Frame.

The copyright year is changed by changing the variable copyright_year in one of the files in the book and while leaving that file open, highlight all of the other files in the book in the left pane, File, Import, Formats, Deselect all, check Variable Definitions, Import.

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In the PICS proforma another variable "PICS_year" is used to show "201x" in the draft versions.

Both revisions and amendments to IEEE Std 802.3 show all five heading levels in the table of contents.

This book contains the frontmatter, a Table of Contents, a file for amending Clause 1, a file for amending Clause 45, a file for a new clause, a file for amending the bibliography in Annex A, and a file for a new annex.

Existing clauses

When creating files for amending other existing clauses, choose a file that uses the Autonumbering format that matches that used in that clause in the base document. One way to do this is to use the file for that clause from the base standard (or amendment that introduced it) with most of the content removed.

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Highlight the marker and open the Marker pod (Special, Marker). The text shown should match the text in the marker in the clause being modified. For the heading "1.5 Abbreviations" above it is:
"72198: H2,1.1: 1.5 Abbreviations".

When an existing heading, figure, table or equation is copied in to the draft as a starting point for a new object to be added to an existing clause, then the original cross-reference marker should be removed from it. If this is not done, then when the new object is pasted into the old clause, Framemaker will remove the marker to avoid creating a duplicate and cross-references to the new object will point to the original object instead.

Editing Instructions use the Paragraph Tag Editing Instruction (as per this paragraph).

Where the text being modified has been changed by another amendment that is expected to be approved before this amendment, the editing instruction is of the form:

Change the second paragraph of 45.2.1.nn (as modified by IEEE Std 802.3yy-20xx) as follows:

Clarification of how this should be done can be found at:
http://www.ieee802.org/3/WG_tools/editorial/requirements/words.html#LIST

The general rule for placement of editing instructions is that if the subclause title is being changed or the entire subclause is being inserted, then the editing instruction comes before the subclause title, otherwise the editing instruction comes after the subclause title.

The convention on inserted clause numbering is:
where a subclause is inserted prior to the existing first subclause it is labeled [existing subclause minus one level].[a through z]. Where a subclause is inserted after an existing subclause (assuming it is not the last) the new subclause is labeled [subclause number][a through z].

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For example to insert two subclauses before 43.2.1 the subclauses would be numbered 43.2.a and 43.2.b. Two subclauses between 43.2.1 and 43.2.2 would be numbered 43.2.1a and 43.2.1b. Two subclauses added after the last subclause 43.2.2 would be numbered 43.2.3 and 43.2.4.

An expanded statement of the scheme (as discussed with IEEE staff) is:

43.2 in base standard
43.2.a inserted by Amendment 1
43.2.b inserted by Amendment 1
43.2.1 in base standard
43.2.1aaa inserted by Amendment 3
43.2.1aa inserted by Amendment 2
43.2.1ab inserted by Amendment 3
43.2.1a inserted by Amendment 1
43.2.1a1 inserted by Amendment 2
43.2.1a2 inserted by Amendment 2
43.2.1b inserted by Amendment 1
...
43.2.1y inserted by Amendment 1
43.2.1z inserted by Amendment 1
43.2.1z1 inserted by Amendment 1
43.2.1z2 inserted by Amendment 1
43.2.2 in base standard
43.2.3 inserted by Amendment 2
43.3 in base standard

Changes between Version 1.0 and Version 2.0

- *Paragraph Tag* DefinitionList added to Clause 200 and Annex 200A
- File structure changed to match that of the base standard
- Text describing existing clause's cross-reference markers added
- Clause 45 file added
- IEEE Std 802.3bk-2013 added to frontmatter

Changes between Version 2.0 and Version 2.1

- file added
- Example register added to Clause 45
- *Paragraph Tag* Editing Instruction added to Clause 1, Clause 45, Clause 200, Annex A, and Annex 200A
- Copyright notice as per 2014 IEEE-SA Standards Style Manual.

Changes between Version 2.1 and Version 2.2

- Changed to be an amendment to IEEE Std 802.3-201x
- Frontmatter updated as per 2014 IEEE-SA Standards Style Manual
- Editor's note regarding frontmatter moved to just after Keywords
- In the PICS, changed the ruling at the bottom of the "Have any Exception items been required?" and the top of the "Date of Statement" rows to "Thin"
- Clause 45 empty pages removed

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Changes between Version 2.2 and Version 2.3

— Moved Clause 200, and Annex 200A to Section_7

Changes between Version 2.3 and Version 2.4

— Updated Introduction section in frontmatter

— Changed 1.4 to have specific subclause numbers

Changes between Version 2.4 and Version 2.5

— base_year variable changed from 201x to 2015

— note regarding the number of levels in the table of contents added

— “A full duplex MAC protocol was added in 1997.” added to the Introduction section in frontmatter.

Changes between Version 2.5 and Version 2.6

— more special characters added

— PICS tables set to start “Anywhere”

— *Paragraph Tag* “Code” added to Clause 200 and Annex 200A

— Expanded scheme for inserted subclauses added

— Ellipsis rows added to Table 45-3

— Annex A editing instruction changed

Changes between Version 2.6 and Version 2.7

— Scheme for inserted subclauses has added examples

— Text regarding figures changed in Clause 200 and Annex 200A

— “arabic” changed to “Arabic” in frontmatter

— Latest amendments added to frontmatter

Changes between Version 2.7 and Version 2.8

— Editing instructions for 1.3 and 1.4 changed to say alphanumeric

— Moved Clause 200 and Annex 200A to Section_8

Changes between Version 2.8 and Version 2.9

— Footer changed so that Copyright statement is centered in FrameMaker 2015

— Corrigendum 1 added to frontmatter

— Editing instruction placement text added

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30. Management

Editor's Note (to be removed prior to publication):
Editor's Instruction template text, "(as modified by IEEE Std 802.3bs-201X, IEEE Std 802.3bt-201X, IEEE Std 802.3ca-201X, IEEE Std 802.3cb-201X, IEEE Std 802.3cc-201X, IEEE Std 802.3cd-201X and IEEE Std 802.3ch-201X)" to be used where needed.

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entries in APPROPRIATE SYNTAX after the entry for "10 Mb/s":

10BASE-T1L Clause 146 10 Mb/s PAM3
10BASE-T1S Clause 147 10 Mb/s PAM3

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in APPROPRIATE SYNTAX after the entry for "1000BASE-T":\

1000BASE-T1L	Single twisted-pair copper cable PHY as specified in Clause 147
1000BASE-T1S	Single twisted-pair copper cable PHY as specified in Clause 148

30.5.1.1.4 aMediaAvailable

Change the third sentence of the third paragraph of BEHAVIOUR DEFINED AS as follows:

For 10BASE-T1L, 10BSE-T1S, and 100BASE-T1, a link_status of OK maps to the enumeration "available". All other states of link_status map to the enumeration "not available".

Change the seventh sentence of the third paragraph of BEHAVIOUR DEFINED AS as follows:

Any MAU that implements management of Clause 28, Clause 73, ~~or~~ Clause 98, Clause 147, or Clause 148 Auto-Negotiation will map remote fault indication to MediaAvailable "remote fault."

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30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

Editor's Note (to be removed prior to publication):

Not sure if change to 30.6.1.1.3 is required. 147.2.1.1 and 148.2.1.1 are placeholder references.

30.6.1.1.3 aAutoNegRemoteSignaling

Change the text of BEHAVIOUR DEFINED AS as follows:

BEHAVIOUR DEFINED AS:
The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts, /C/ ordered sets (see 36.2.4.10) or DME signals (see 73.5, ~~and~~ 98.2.1.1, 147.2.1.1, and 148.2.1.1) were received from the remote end.;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entries in APPROPRIATE SYNTAX after the entry for "10BASE-T":

10BASE-T1L	10BASE-T1L as specified in Clause 147
10BASE-T1S	10BASE-T1S as specified in Clause 148

Editor's Note (to be removed prior to publication):

Not sure if change to Rem Fault is required.

Change the entry for Rem Fault as follows:

Rem Fault	Rem Fault Remote fault bit (RF) as specified in Clause 73, ~~and~~ Clause 98, Clause 147, and Clause 148

Editor's Note (to be removed prior to publication):

Not sure if change to Force MS is required. 147.2.1.2.5 and 148.2.1.2.5 are placeholder references.

Change the entry for Force MS as follows:

Force MS	Force MASTER-SLAVE as specified in Clause 98 (see 98.2.2.5), Clause 147 (see 147.2.1.2.5), and Clause 148(see 148.2.1.2.5)

Change the text of BEHAVIOUR DEFINED AS as follows:

BEHAVIOUR DEFINED AS:
This indicates the technology ability of the local device, as defined in Clause 28, Clause 37, Clause 73, ~~and~~ Clause 98, Clause 147, and Clause 148;

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30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

Change the text of BEHAVIOUR DEFINED AS as follows:

BEHAVIOUR DEFINED AS:
This GET-SET attribute maps to the technology ability of the local device, as defined in Clause 28, Clause 37, ~~and~~ Clause 98, Clause 147, and Clause 148.

30.6.1.1.7 aAutoNegLocalSelectorAbility

Editor's Note (to be removed prior to publication):

147.2.1.2 and 148.2.1.2 are placeholder references.

Insert two new sentences at the end of BEHAVIOUR DEFINED AS as follows:

For Clause 147Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 147.2.1.2). For Clause 148 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 148.2.1.2).

30.6.1.1.8 aAutoNegAdvertisedSelectorAbility

Editor's Note (to be removed prior to publication):

147.2.1.2.1 and 148.2.1.2.1 are placeholder references.

Change the text of BEHAVIOUR DEFINED AS as follows:

BEHAVIOUR DEFINED AS:
This indicates the value of the selector field of the local hardware. The Selector Field is defined in 28.2.1.2.1 for Clause 28 Auto-Negotiation, in 73.6.1 for Clause 73 Auto- Negotiation, ~~and~~ in 98.2.1.2.1 for Clause 98 Auto-Negotiation, in 147.2.1.2.1 for Clause 147, and in 148.2.1.2.1 for Clause 148. The enumeration of the Selector Field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration "ethernet".;

30.6.1.1.9 aAutoNegReceivedSelectorAbility

Editor's Note (to be removed prior to publication):

147.2.1.2.1 and 148.2.1.2.1 are placeholder references.

Change the text of BEHAVIOUR DEFINED AS as follows:

BEHAVIOUR DEFINED AS:
In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector Field of the Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute maps to the- Selector Field of the Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 98 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 98 Auto-Negotiation link codeword (see 98.2.1.2.1). For Clause 147 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 147 Auto-Negotiation link codeword (see 147.2.1.2.1). For Clause 148 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 148 Auto-Negotiation link

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codeword (see 148.2.1.2.1). A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration “ethernet”.

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45. Management Data Input/Output (MDIO) Interface

Editor's Note (to be removed prior to publication):
Editor's Instruction template text, "(as modified by IEEE Std 802.3bs-201X, IEEE Std 802.3bt-201X, IEEE Std 802.3ca-201X, IEEE Std 802.3cb-201X, IEEE Std 802.3cc-201X, IEEE Std 802.3cd-201X and IEEE Std 802.3ch-201X)" to be used where needed.

45.2 MDIO Interface Registers

45.2.1 PMA/PMD register

Editor's Note (to be removed prior to publication):

Subclause references are placeholders.

Change the row for 1.2103 through 1.2303 and add new rows in Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.2103 through 1.2293~~303~~	Reserved	
1.2294	10BASE-T1L PMA control	147.2.1.133
1.2295	10BASE-T1L PMA status	147.2.1.134
1.2296	10BASE-T1L training	147.2.1.135
1.2297	10BASE-T1L link partner training	147.2.1.136
1.2298	10BASE-T1L test mode control	147.2.1.137
1.2299	10BASE-T1S PMA control	148.2.1.133
1.2300	10BASE-T1S MA status	148.2.1.134
1.2301	10BASE-T1S training	148.2.1.135
1.2302	10BASE-T1S link partner training	148.2.1.136
1.2303	10BASE-T1S test mode control	187.2.1.137

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

45.2.1.6.3 PMA/PMD type selection (1.7.5:0)

Change the register bit definitions for values 1 1 1 1 0 0 and 1 1 1 0 1 1 for bits 1.7.5:0 in Table 45–7 as follows (unchanged rows not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 1 1 0 0 = ~~reserved~~10BASE-T1L PMA/PMD 1 1 1 0 1 1 = ~~reserved~~10BASE-T1S PMA/PMD	R/W

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[a]R/W = Read/Write, RO = Read only

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

Change the row for 1.18.15.2 and add new rows in Table 45–19 as follows (unchanged rows not shown):

Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:~~2~~4	Reserved	Value always 0	RO
1.18.3	10BASE-T1L ability	1 = PMA/PMD is able to perform 10BASE-T1L 0 = PMA/PMD is not able to perform 10BASE-T1L	RO
1.18.2	10BASE-T1S ability	1 = PMA/PMD is able to perform 10BASE-T1S 0 = PMA/PMD is not able to perform 10BASE-T1S	RO

[a]RO = Read only

45.2.1.173 BASE-T1 PMA/PMD control register (Register 1.2100)

Change the row for 1.2100.3:0 in Table 45–141 as follows (unchanged rows not shown):

Table 45–141—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2100.3:0	Type Selection	3 2 1 01 x x x = Reserved 0 1 x x = Reserved 0 0 1 ~~x~~0 = ~~Reserved~~10BASE-T1L 0 0 1 1 = 10BASE-T1S 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	RO

[a]RO = Read only, R/W = Read/Write

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Insert 45.2.1.174a through 45.2.1.174j after 45.2.1.174 as follows:

45.2.1.174a10BASE-T1L PMA control register (Register 1.2294)

The assignment of bits in the 10BASE-T1L PMA control register is shown in Table 45–142a.

Table 45–142a—10BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2294.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2294.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2294.13:12	Reserved	Value always 0	RO
1.2294.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2294.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self clearing

45.2.1.174a.1 PMA/PMD reset (1.2294.15)

Resetting the 10BASE-T1L PMA/PMD is accomplished by setting bit 1.2294.15 to a one. This action shall set all 10BASE-T1L PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1L PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self clearing, and the 10BASE-T1L PMA/PMD shall return a value of one in bit 1.2294.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2294.15.

Editor's Note (to be removed prior to publication):

Bits highlighted in yellow should be verified.

During a reset, the 10BASE-T1L PMD/PMA shall respond to reads from register bits 1.2294.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

This operation may interrupt data communication.

Bit 1.2294.15 is a copy of 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PMA/PMD.

45.2.1.174a.2 Transmit disable (1.2294.14)

When bit 1.2294.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2294.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2294.14 is a copy of 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

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45.2.1.174a.3 Low-power (1.2294.11)

When the low-power ability is supported, the 10BASE-T1L PMA/PMD may be placed into a low-power mode by setting bit 1.2294.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1L PMA/PMD. The behavior of the 10BASE-T1L PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2294.11 is zero.

NOTE—This operation interrupts data communication. The data path of the 10BASE-T1L PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2294.11 is a copy of 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1L PMA/PMD in low-power mode.

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45.2.1.174b 10BASE-T1L PMA status register (Register 1.2295)

The assignment of bits in the 10BASE-T1L PMA status register is shown in Table 45–142b.

Table 45–142b—10BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2295.15:12	Reserved	Value always 0	RO
1.2295.11	10BASE-T1L OAM Ability	1 = PHY has 10BASE-T1L OAM ability 0 = PHY does not have 10BASE-T1L OAM ability	RO
1.2295.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2295.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2295.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2295.7:3	Reserved	Value always 0	RO
1.2295.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2295.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2295.0		1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LL = Latching Low

45.2.1.174b.1 10BASE-T1L OAM ability (1.2295.11)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports 10BASE-T1L OAM (see 147.x.x). When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support 10BASE-T1L OAM

45.2.1.174b.2 EEE ability (1.2295.10)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports EEE. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support EEE.

45.2.1.174b.3 Receive fault ability (1.2295.9)

When read as a one, bit 1.2295.9 indicates that the 10BASE-T1L PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2295.9 indicates that the 10BASE-T1L PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.174b.4 Low-power ability (1.2295.8)

When read as a one, bit 1.2295.8 indicates that the 10BASE-T1L PMA/PMD supports the low-power ability. When read as a zero, bit 1.2295.8 indicates that the 10BASE-T1L PMA/PMD does not support the

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low-power feature. If the 10BASE-T1L PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2294.11 or bit 1.0.11.

45.2.1.174b.5 Receive polarity (1.2295.2)

When read as zero, bit 1.2295.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2295.2 indicates that the polarity of receiver is reversed.

45.2.1.174b.6 Receive fault (1.2295.1)

When read as a one, bit 1.2295.1 indicates that the 10BASE-T1L PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2295.1 indicates that the 10BASE-T1L PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2295.9. The 10BASE-T1L PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.174b.7 Receive link status (1.2295.0)

When read as a one, bit 1.2295.0 indicates that the 10BASE-T1L PMA/PMD receive link is up. When read as a zero, bit 1.2295.0 indicates that the 10BASE-T1L PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.174c 10BASE-T1L training register (Register 1.2296)

The assignment of bits in the 10BASE-T1L training register is shown in Table 45–142c.

Table 45–142c—10BASE-T1L training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2296.15:11	Reserved	Value always 0	RO
1.2296.10:4	User field	7-bit user defined field to send to the link partner	R/W
1.2296.3:2	Reserved	Value always 0	RO
1.2296.1	10BASE-T1L OAM advertisement	1 = 10BASE-T1L OAM ability advertised to link partner 0 = 10BASE-T1L OAM ability not advertised to link partner	R/W
1.2296.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.174c.1 User field (1.2296.10:4)

This register is a user defined 7-bit field that is transmitted to the link partner during training.

45.2.1.174c.2 10BASE-T1L OAM advertisement (1.2296.1)

When set as a one, this bit indicates to the link partner that the 10BASE-T1L PHY is advertising 10BASE-T1L OAM capability. When set as a zero, this bit indicates to the link partner that the

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10BASE-T1L PHY is not advertising 10BASE-T1L OAM capability. This bit shall be set to 0 if the 10BASE-T1L PHY does not support 10BASE-T1L OAM.

45.2.1.174c.3 EEE advertisement (1.2296.0)

When set as a one, this bit indicates to the link partner that the 10BASE-T1L PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the 10BASE-T1L PHY is not advertising EEE capability. This bit shall be set to 0 if the 10BASE-T1L PHY does not support EEE.

45.2.1.174d 10BASE-T1L link partner training register (Register 1.2297)

The assignment of bits in the 10BASE-T1L link partner training register is shown in Table 45–142d. The values in this register are not valid until link is up.

Table 45–142d—10BASE-T1L link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2297.15:11	Reserved	Value always 0	RO
1.2297.10:4	Link partner user field	7-bit user defined field received from the link partner	RO
1.2297.3:2	Reserved	Value always 0	RO
1.2297.1	Link partner 10BASE-T1L OAM advertisement	1 = Link partner has 10BASE-T1L OAM ability 0 = Link partner does not have 10BASE-T1L OAM ability	RO
1.2297.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.174d.1 Link partner user field (1.2297.10:4)

This register is a user defined 7-bit field that is received from the link partner during training.

45.2.1.174d.2 Link partner 10BASE-T1L OAM advertisement (1.2297.1)

When read as a one, this bit indicates the link partner is advertising 10BASE-T1L OAM capability. When read as a zero, this bit indicates the link partner is not advertising 10BASE-T1L OAM capability. 10BASE-T1L OAM capability shall be enabled only when both the local device and its link partner are advertising 10BASE-T1L OAM capability.

45.2.1.174d.3 Link partner EEE advertisement (1.2297.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local device and its link partner are advertising EEE capability.

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45.2.1.174e 10BASE-T1L test mode control register (Register 1.2298)

The assignment of bits in the 10BASE-T1L test mode control register is shown in Table 45–142e. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–142e—10BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2298.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	RO
1.2298.12:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.174e.1 Test mode control (1.2298.15:13)

Transmitter test mode operations defined by bits 1.2297.15:13, are described in 97.5.2 and Table 97-12. The default value for bits 1.2298.15:13 is zero.

45.2.1.174f 10BASE-T1S PMA control register (Register 1.2299)

The assignment of bits in the 10BASE-T1S PMA control register is shown in Table 45–142f.

Table 45–142f—10BASE-T1S PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2299.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2299.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2299.13:12	Reserved	Value always 0	RO
1.2299.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2299.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self clearing

45.2.1.174f.1 PMA/PMD reset (1.2299.15)

Resetting the 10BASE-T1S PMA/PMD is accomplished by setting bit 1.2299.15 to a one. This action shall set all 10BASE-T1S PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self clearing, and the

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10BASE-T1S PMA/PMD shall return a value of one in bit 1.2299.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2299.15.

During a reset, the 10BASE-T1S PMD/PMA shall respond to reads from register bits 1.2299.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

This operation may interrupt data communication.

Bit 1.2299.15 is a copy of 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PMA/PMD.

45.2.1.174f.2 Transmit disable (1.2299.14)

When bit 1.2299.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2299.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2299.14 is a copy of 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.174f.3 Low-power (1.2299.11)

When the low-power ability is supported, the 10BASE-T1S PMA/PMD may be placed into a low-power mode by setting bit 1.2294.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1S PMA/PMD. The behavior of the 10BASE-T1S PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2294.11 is zero.

NOTE—This operation interrupts data communication. The data path of the 10BASE-T1S PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2299.11 is a copy of 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1S PMA/PMD in low-power mode.

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45.2.1.174g 10BASE-T1L PMA status register (Register 1.2300)

The assignment of bits in the 10BASE-T1S PMA status register is shown in Table 45–142g.

Table 45–142g—10BASE-T1S PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2300.15:12	Reserved	Value always 0	RO
1.2300.11	10BASE-T1S OAM Ability	1 = PHY has 10BASE-T1S OAM ability 0 = PHY does not have 10BASE-T1S OAM ability	RO
1.2300.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2300.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2300.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2300.7:3	Reserved	Value always 0	RO
1.2300.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2300.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2300.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LL = Latching Low

45.2.1.174g.1 10BASE-T1L OAM ability (1.2300.11)

When read as a one, this bit indicates that the 10BASE-T1S PHY supports 10BASE-T1S OAM (see 147.x.x). When read as a zero, this bit indicates that the 10BASE-T1S PHY does not support 10BASE-T1S OAM

45.2.1.174g.2 EEE ability (1.2300.10)

When read as a one, this bit indicates that the 10BASE-T1S PHY supports EEE. When read as a zero, this bit indicates that the 10BASE-T1S PHY does not support EEE.

45.2.1.174g.3 Receive fault ability (1.2300.9)

When read as a one, bit 1.2300.9 indicates that the 10BASE-T1S PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2300.9 indicates that the 10BASE-T1S PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.174g.4 Low-power ability (1.2300.8)

When read as a one, bit 1.2300.8 indicates that the 10BASE-T1S PMA/PMD supports the low-power ability. When read as a zero, bit 1.2300.8 indicates that the 10BASE-T1S PMA/PMD does not support the low-

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power feature. If the 10BASE-T1S PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2299.11 or bit 1.0.11.

45.2.1.174g.5 Receive polarity (1.2300.2)

When read as zero, bit 1.2300.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2300.2 indicates that the polarity of receiver is reversed.

45.2.1.174g.6 Receive fault (1.2300.1)

When read as a one, bit 1.2300.1 indicates that the 10BASE-T1S PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2300.1 indicates that the 10BASE-T1S PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2300.9. The 10BASE-T1S PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.174g.7 Receive link status (1.2300.0)

When read as a one, bit 1.2300.0 indicates that the 10BASE-T1S PMA/PMD receive link is up. When read as a zero, bit 1.2300.0 indicates that the 10BASE-T1S PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.174h 10BASE-T1S training register (Register 1.2301)

The assignment of bits in the 10BASE-T1S training register is shown in Table 45–142h.

Table 45–142h—10BASE-T1S training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2301.15:11	Reserved	Value always 0	RO
1.2301.10:4	User field	7-bit user defined field to send to the link partner	R/W
1.2301.3:2	Reserved	Value always 0	RO
1.2301.1	10BASE-T1S OAM advertisement	1 = 10BASE-T1S OAM ability advertised to link partner 0 = 10BASE-T1S OAM ability not advertised to link partner	R/W
1.2301.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.174h.1 User field (1.2301.10:4)

This register is a user defined 7-bit field that is transmitted to the link partner during training.

45.2.1.174h.2 10BASE-T1S OAM advertisement (1.2301.1)

When set as a one, this bit indicates to the link partner that the 10BASE-T1S PHY is advertising 10BASE-T1S OAM capability. When set as a zero, this bit indicates to the link partner that the

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10BASE-T1S PHY is not advertising 10BASE-T1S OAM capability. This bit shall be set to 0 if the 10BASE-T1S PHY does not support 10BASE-T1S OAM.

45.2.1.174h.3 EEE advertisement (1.2301.0)

When set as a one, this bit indicates to the link partner that the 10BASE-T1S PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the 10BASE-T1S PHY is not advertising EEE capability. This bit shall be set to 0 if the 10BASE-T1S PHY does not support EEE.

45.2.1.174i 10BASE-T1S link partner training register (Register 1.2302)

The assignment of bits in the 10BASE-T1S link partner training register is shown in Table 45–142i. The values in this register are not valid until link is up.

Table 45–142i—10BASE-T1S link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2302.15:11	Reserved	Value always 0	RO
1.2302.10:4	Link partner user field	7-bit user defined field received from the link partner	RO
1.2302.3:2	Reserved	Value always 0	RO
1.2302.1	Link partner 10BASE-T1L OAM advertisement	1 = Link partner has 10BASE-T1L OAM ability 0 = Link partner does not have 10BASE-T1L OAM ability	RO
1.2302.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.174i.1 Link partner user field (1.2302.10:4)

This register is a user defined 7-bit field that is received from the link partner during training.

45.2.1.174i.2 Link partner 10BASE-T1S OAM advertisement (1.2302.1)

When read as a one, this bit indicates the link partner is advertising 10BASE-T1S OAM capability. When read as a zero, this bit indicates the link partner is not advertising 10BASE-T1S OAM capability. 10BASE-T1S OAM capability shall be enabled only when both the local device and its link partner are advertising 10BASE-T1S OAM capability.

45.2.1.174i.3 Link partner EEE advertisement (1.2302.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local device and its link partner are advertising EEE capability.

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45.2.1.174j 10BASE-T1S test mode control register (Register 1.2303)

The assignment of bits in the 10BASE-T1S test mode control register is shown in Table 45–142j. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–142j—10BASE-T1S test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2298.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	RO
1.2298.12:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.174j.1 Test mode control (1.2303.15:13)

Transmitter test mode operations defined by bits 1.2303.15:13, are described in 97.5.2 and Table 97-12. The default value for bits 1.2303.15:13 is zero.

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45.2.3 PCS Registers

Editor's Note (to be removed prior to publication):
Subclause references are placeholders.

Change the row for 3.1809 through 3.2303 and add new rows in Table 45–168 as follows (unchanged rows not shown)::

Table 45–168—PCS registers

Register address	Register name	Subclause
3.1809 through 3.~~2303~~2277	Reserved	
3.2278	10BASE-T1L PCS control	147.2.3.51
3.2279	10BASE-T1L PCS status 1	147.2.3.52
3.2280	10BASE-T1L PCS status 2	147.2.3.53
3.2281	110BASE-T1L OAM transmit	147.2.3.54
3.2282 through 3.2285	10BASE-T1L OAM message	147.2.3.55
3.2286	10BASE-T1LOAM receive	147.2.3.56
3.2287 through 3.2290	Link partner 10BASE-T1L OAM message	147.2.3.57
3.2291	10BASE-T1S PCS control	148.2.3.51
3.2292	10BASE-T1S PCS status 1	148.2.3.52
3.2293	10BASE-T1S PCS status 2	148.2.3.53
3.2294	10BASE-T1SOAM transmit	148.2.3.54
3.2295 through 3.2298	10BASE-T1S OAM message	148.2.3.55
3.2299	10BASE-T1SOAM receive	148.2.3.56
3.2300 through 3.2303	Link partner 10BASE-T1S OAM message	148.2.3.57

Insert 45.2.3.58a through 45.2.3.58n after 45.2.3.58 as follows:

45.2.3.58a 10BASE-T1L PCS control register (Register 3.2278)

The assignment of bits in the 10BASE-T1L PCS control register is shown in Table 45–220a. The default value for each bit of the 10BASE-T1L PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–220a—10BASE-T1L PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2278.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2278.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2278.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self Clearing

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45.2.3.58a.1 PCS reset (3.2278.15)

Resetting the 10BASE-T1L PCS is accomplished by setting bit 3.2278.15 to a one. This action shall set all 10BASE-T1L PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1L PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1L PCS shall return a value of one in bit 3.2278.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2294.15. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2278.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2278.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PCS.

45.2.3.58a.2 Loopback (3.2278.14)

The 10BASE-T1L PCS shall be placed in a loopback mode of operation when bit 3.2278.14 is set to a one. When bit 3. 2278.14 is set to a one, the 10BASE-T1L PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2278.14 is zero.

Bit 3.2278.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.58b 10BASE-T1L PCS status 1 register (Register 3.2279)

The assignment of bits in the 10BASE-T1L PCS status 1 register is shown in Table 45–220b. All the bits in the 10BASE-T1L PCS status 1 register are read only; a write to the 10BASE-T1L PCS status 1 register shall have no effect.

Table 45–220b—10BASE-T1L PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2279.15:12	Reserved	Value always 0	RO
3.2279.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2279.6:3	Reserved	Value always 0	RO
3.2279.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2279.1:0	Reserved	Value always 0	RO

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[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.58b.1 Tx LPI received (3.2279.11)

When read as a one, bit 3.2279.11 indicates that the transmit 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.11 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.58b.2 Rx LPI received (3.2279.10)

When read as a one, bit 3.2279.10 indicates that the receive 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.10 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.58b.3 Tx LPI indication (3.2279.9)

When read as a one, bit 3.2279.9 indicates that the transmit 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.9 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.58b.4 Rx LPI indication (3.2279.8)

When read as a one, bit 3.2279.8 indicates that the receive 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.8 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.58b.5 Fault (3.2279.7)

When read as a one, bit 3.2279.7 indicates that the 10BASE-T1L PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2279.7 indicates that the 10BASE-T1L PCS has not detected a fault condition.

45.2.3.58b.6 PCS receive link status (3.2279.2)

When read as a one, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link is up. When read as a zero, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link was down since the last read from this register. This bit is a latching low version of bit 3.2280.10. The PCS receive link status bit shall be implemented with latching low behavior.

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45.2.3.58c 10BASE-T1L PCS status 2 register (Register 3.2280)

The assignment of bits in the 10BASE-T1L PCS status 2 register is shown in Table 45–220c. All the bits in the 10BASE-T1L PCS status 2 register are read only; a write to the 10BASE-T1L PCS status 2 register shall have no effect.

Table 45–220c—10BASE-T1L PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2280.15:11	Reserved	Value always 0	RO
3.2280.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2280.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2280.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2280.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2280.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2280.5:0	BER count	BER counter	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.58c.1 Receive link status (3.2280.10)

When read as a one, bit 3.2280.10 indicates that the 10BASE-T1L PCS is in a fully operational state. When read as a zero, bit 3.2280.10 indicates that the 10BASE-T1L PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 97.3.7.1.

45.2.3.58c.2 PCS high BER (3.2280.9)

When read as a one, bit 3.2280.9 indicates that the 10BASE-T1L PCS receiver is detecting a BER of $> 4 \times 10^{-4}$. When read as a zero, bit 3.2280.9 indicates that the 10BASE-T1L PCS is not detecting a BER of $> 4 \times 10^{-4}$. This bit is a reflection of the state of the hi_rfer variable defined in 97.3.7.1.

45.2.3.58c.3 PCS block lock (3.2280.8)

When read as a one, bit 3.2280.8 indicates that the 10BASE-T1L PCS receiver has block lock. When read as a zero, bit 3.2280.8 indicates that the 10BASE-T1L PCS receiver has not achieved block lock. This bit is a reflection of the state of the block_lock variable defined in 97.3.7.1.

45.2.3.58c.4 Latched high BER (3.2280.7)

When read as a one, bit 3.2280.7 indicates that the 10BASE-T1L PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2280.7 indicates that the 10BASE-T1L PCS

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has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the 10BASE-T1L PCS high BER status bit (3.2280.9).

45.2.3.58c.5 Latched block lock (3.2280.6)

When read as a one, bit 3.2280.6 indicates that the 10BASE-T1L PCS has achieved block lock. When read as a zero, bit 3.2280.6 indicates that the 10BASE-T1L PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 10BASE-T1L PCS block lock status bit (3.2280.8).

45.2.3.58c.6 BER count (3.2280.5:0)

The BER counter formed by bits 3.2280.5:0 is a six bit count as defined by RFER_count in 97.3.7.2. These bits shall be reset to all zeros when the 10BASE-T1L PCS status 2 register is read by the management function or upon execution of the 10BASE-T1L PCS reset. These bits shall be held at all ones in the case of overflow.

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45.2.3.58d 10BASE-T1L OAM transmit register (Register 3.2281)

The assignment of bits in the 10BASE-T1L OAM transmit register is shown in Table 45–220d.

Table 45–220d—10BASE-T1L OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2281.15	10BASE-T1L OAM message valid	This bit is used to indicate message data in registers 3.2281.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit shall self clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2281.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2281.13	10BASE-T1L OAM message received	This bit shall self clear on read. 1 = 10BASE-T1L OAM message received by link partner 0 = 10BASE-T1L OAM message not received by link partner	RO, LH
3.2281.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2281.13.	RO
3.2281.11:8	Message number	User-defined message number to send	R/W
3.2281.7:4	Reserved	Value always 0	RO
3.2281.3	Ping received	Received PingTx value from latest good 10BASE-T1L OAM frame received	RO
3.2281.2	Ping transmit	Ping value to send to link partner	R/W
3.2281.1:0	Local SNR	00 = PHY link is failing and will drop link and re-link within 2 to 4 ms after the end of the current 10BASE-T1L OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

45.2.3.58d.1 10BASE-T1L OAM message valid (3.2281.15)

Bit 3.2281.15 shall be set to 1 when the 10BASE-T1L OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2281.11:8 are properly configured to be transmitted. This register shall be cleared by the state machine to indicate whether the next 10BASE-T1L OAM message can be written into the registers.

45.2.3.58d.2 Toggle value (3.2281.14)

The state machine shall assign a value alternating between 0 and 1 to associate with the 8 octet 10BASE-T1L OAM message transmit by the 10BASE-T1L PHY. Bit 3.2281.14 should be read and recorded prior to setting 3.2281.15 to 1. The recorded value can be correlated with 3.2281.12 as a confirmation that the 10BASE-T1L OAM message is received by the link partner.

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45.2.3.58d.3 10BASE-T1L OAM message received (3.2281.13)

Bit 3.2281.13 shall indicate whether the most recently transmitted 10BASE-T1L OAM message with a toggle bit value in 3.2281.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.58d.4 Received message toggle value (3.2281.12)

Bit 3.2281.12 indicates the toggle bit value of the 10BASE-T1L OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2281.13 is 1.

45.2.3.58d.5 Message number (3.2281.11:8)

The 10BASE-T1L OAM message number to be transmitted. This field is user defined but is recommended that it be used to indicate the meaning of the 8 octet 10BASE-T1L OAM message. If used this way, up to 16 different 8 octet messages can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

45.2.3.58d.6 Ping received (3.2281.3)

Bit 3.2281.3 represents the value of the most recent Ping RX received from the link partner (see 97.3.8.2.3).

45.2.3.58d.7 Ping transmit (3.2281.2)

Bit 3.2281.2 represents the value to be sent to the link partner via the Ping TX function (see 97.3.8.2.4).

45.2.3.58d.8 Local SNR (3.2281.1:0)

Bits 3.2281.1:0 are set by the 10BASE-T1L PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.58e 10BASE-T1L OAM message register (Registers 3.2282 to 3.2285)

The 8 octet 10BASE-T1L OAM message data to be transmitted. The 8 octet message data is user defined and its definition is outside the scope of this standard.

Table 45–220e—10BASE-T1L OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2282.15:8	10BASE-T1L OAM message 1	Message octet 1. LSB transmitted first.	R/W
3.2282.7:0	10BASE-T1L OAM message 0	Message octet 0. LSB transmitted first.	R/W
3.2283.15:8	10BASE-T1L OAM message 3	Message octet 3. LSB transmitted first.	R/W
3.2283.7:0	10BASE-T1L OAM message 2	Message octet 2. LSB transmitted first.	R/W
3.2284.15:8	10BASE-T1L OAM message 5	Message octet 5. LSB transmitted first.	R/W
3.2294.7:0	10BASE-T1L OAM message 4	Message octet 4. LSB transmitted first.	R/W
3.2295.15:8	10BASE-T1L OAM message 7	Message octet 7. LSB transmitted first.	R/W
3.2295.7:0	10BASE-T1L OAM message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

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45.2.3.58f 10BASE-T1L OAM receive register (Register 3.2286)

The assignment of bits in the 10BASE-T1L OAM receive register is shown in Table 45–220f

Table 45–220f—10BASE-T1L OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2286.15	Link partner 10BASE-T1L OAM message valid	This bit is used to indicate message data in registers 3.2286.11:8, 3.2287, 3.2288, 3.2289, and 3.2290 are stored and ready to be read. This bit shall self clear when register 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2286.14	Link partner toggle value	Toggle value received with message.	RO
3.2286.13:12	Reserved	Value always 0	RO
3.2286.11:8	Link partner message number	Message number from link partner	RO
3.2286.7:2	Reserved	Value always 0	RO
3.2286.1:0	Link partner SNR	00 = Link partner link is failing and will drop link and re-link within 2 to 4 ms after the end of the current 10BASE-T1L OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.58f.1 Link partner 10BASE-T1L OAM message valid (3.2286.15)

Bit 3.2286.15 shall be set to 1 when the 10BASE-T1L OAM message from the link partner is stored into registers 3.2287, 3.2288, 3.2289, and 3.2290 and the message number in 3.2286.11:8. This register shall be cleared when register 3.2390 is read.

45.2.3.58f.2 Link partner toggle value (3.2286.14)

Bit 3.2286.14 indicates the toggle value associate with the 8 octet 10BASE-T1L OAM message from the link partner.

45.2.3.58f.3 Link partner message number (3.2286.11:8)

The 10BASE-T1L OAM message number from the link partner.

45.2.3.58f.4 Link partner SNR (3.2286.1:0)

Bits 3.2286.1:0 indicate the status of the link partner receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.58g Link partner 10BASE-T1L OAM message register (Registers 3.2287 to 3.2290)

The 8 octet 10BASE-T1L OAM message data from the link partner. Register 3.2286.15 shall be cleared

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when register 3.2290 is read.

45.2.3.58h 10BASE-T1S PCS control register (Register 3.2291)

The assignment of bits in the 10BASE-T1S PCS control register is shown in Table 45–220g. The default value for each bit of the 10BASE-T1S PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–220g—10BASE-T1S PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2291.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2291.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2291.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self Clearing

45.2.3.58h.1 PCS reset (3.2291.15)

Resetting the 10BASE-T1S PCS is accomplished by setting bit 3.2291.15 to a one. This action shall set all 10BASE-T1S PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1S PCS shall return a value of one in bit 3.2291.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2294.15. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2291.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2278.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PCS.

45.2.3.58h.2 Loopback (3.2291.14)

The 10BASE-T1S PCS shall be placed in a loopback mode of operation when bit 3.2291.14 is set to a one. When bit 3. 2291.14 is set to a one, the 10BASE-T1S PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2291.14 is zero.

Bit 3.2291.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.58i 10BASE-T1S PCS status 1 register (Register 3.2292)

The assignment of bits in the 10BASE-T1S PCS status 1 register is shown in Table 45–220h. All the bits in the 10BASE-T1S PCS status 1 register are read only; a write to the 10BASE-T1S PCS status 1 register shall have no effect.

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Table 45–220h—10BASE-T1S PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2292.15:12	Reserved	Value always 0	RO
3.2292.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2292.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2292.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2292.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2292.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2292.6:3	Reserved	Value always 0	RO
3.2292.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2292.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.58i.1 Tx LPI received (3.2292.11)

When read as a one, bit 3.2292.11 indicates that the transmit 10BASE-T1S PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2292.11 indicates that the 10BASE-T1S PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.58i.2 Rx LPI received (3.2292.10)

When read as a one, bit 3.2292.10 indicates that the receive 10BASE-T1S PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2292.10 indicates that the 10BASE-T1S PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.58i.3 Tx LPI indication (3.2292.9)

When read as a one, bit 3.2292.9 indicates that the transmit 10BASE-T1S PCS is currently receiving LPI signals. When read as a zero, bit 3.2292.9 indicates that the 10BASE-T1S PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.58i.4 Rx LPI indication (3.2292.8)

When read as a one, bit 3.2292.8 indicates that the receive 10BASE-T1S PCS is currently receiving LPI signals. When read as a zero, bit 3.2292.8 indicates that the 10BASE-T1S PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

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45.2.3.58i.5 Fault (3.2292.7)

When read as a one, bit 3.2292.7 indicates that the 10BASE-T1S PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2292.7 indicates that the 10BASE-T1S PCS has not detected a fault condition.

45.2.3.58i.6 PCS receive link status (3.2292.2)

When read as a one, bit 3.2292.2 indicates that the 10BASE-T1L PCS receive link is up. When read as a zero, bit 3.2292.2 indicates that the 10BASE-T1L PCS receive link was down since the last read from this register. This bit is a latching low version of bit 3.2293.10. The PCS receive link status bit shall be implemented with latching low behavior.

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45.2.3.58j 10BASE-T1S PCS status 2 register (Register 3.2293)

The assignment of bits in the 10BASE-T1S PCS status 2 register is shown in Table 45–220i. All the bits in the 10BASE-T1S PCS status 2 register are read only; a write to the 10BASE-T1S PCS status 2 register shall have no effect.

Table 45–220i—10BASE-T1S PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2293.15:11	Reserved	Value always 0	RO
3.2293.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2293.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2293.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2293.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2293.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2293.5:0	BER count	BER counter	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.58j.1 Receive link status (3.2293.10)

When read as a one, bit 3.2293.10 indicates that the 10BASE-T1S PCS is in a fully operational state. When read as a zero, bit 3.2293.10 indicates that the 10BASE-T1S PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 97.3.7.1.

45.2.3.58j.2 PCS high BER (3.2293.9)

When read as a one, bit 3.2293.9 indicates that the 10BASE-T1S PCS receiver is detecting a BER of $> 4 \times 10^{-4}$. When read as a zero, bit 3.2293.9 indicates that the 10BASE-T1S PCS is not detecting a BER of $> 4 \times 10^{-4}$. This bit is a reflection of the state of the hi_rfer variable defined in 97.3.7.1.

45.2.3.58j.3 PCS block lock (3.2293.8)

When read as a one, bit 3.2293.8 indicates that the 10BASE-T1S PCS receiver has block lock. When read as a zero, bit 3.2293.8 indicates that the 10BASE-T1S PCS receiver has not achieved block lock. This bit is a reflection of the state of the block_lock variable defined in 97.3.7.1.

45.2.3.58j.4 Latched high BER (3.2293.7)

When read as a one, bit 3.2293.7 indicates that the 10BASE-T1S PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2293.7 indicates that the 10BASE-T1S PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the 10BASE-T1S PCS high BER status bit (3.2294.9).

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45.2.3.58j.5 Latched block lock (3.2293.6)

When read as a one, bit 3.2293.6 indicates that the 10BASE-TS PCS has achieved block lock. When read as a zero, bit 3.2293.6 indicates that the 10BASE-T1S PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 10BASE-T1S PCS block lock status bit (3.2294.8).

45.2.3.58j.6 BER count (3.2293.5:0)

The BER counter formed by bits 3.2293.5:0 is a six bit count as defined by RFER_count in 97.3.7.2. These bits shall be reset to all zeros when the 10BASE-T1S PCS status 2 register is read by the management function or upon execution of the 10BASE-T1S PCS reset. These bits shall be held at all ones in the case of overflow.

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45.2.3.58k 10BASE-T1S OAM transmit register (Register 3.2294)

The assignment of bits in the 10BASE-T1S OAM transmit register is shown in Table 45–220j.

Table 45–220j—10BASE-T1S OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2294.15	10BASE-T1S OAM message valid	This bit is used to indicate message data in registers 3.2281.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit shall self clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2294.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2294.13	10BASE-T1S OAM message received	This bit shall self clear on read. 1 = 10BASE-T1S OAM message received by link partner 0 = 10BASE-T1S OAM message not received by link partner	RO, LH
3.2294.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2281.13.	RO
3.2294.11:8	Message number	User-defined message number to send	R/W
3.2294.7:4	Reserved	Value always 0	RO
3.2294.3	Ping received	Received PingTx value from latest good 10BASE-T1L OAM frame received	RO
3.2294.2	Ping transmit	Ping value to send to link partner	R/W
3.2294.1:0	Local SNR	00 = PHY link is failing and will drop link and re-link within 2 to 4 ms after the end of the current 10BASE-T1S OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

45.2.3.58k.1 10BASE-T1L OAM message valid (3.2294.15)

Bit 3.2294.15 shall be set to 1 when the 10BASE-T1L OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2294.11:8 are properly configured to be transmitted. This register shall be cleared by the state machine to indicate whether the next 10BASE-T1S OAM message can be written into the registers.

45.2.3.58k.2 Toggle value (3.2294.14)

The state machine shall assign a value alternating between 0 and 1 to associate with the 8 octet 10BASE-T1S OAM message transmit by the 10BASE-T1S PHY. Bit 3.2294.14 should be read and recorded prior to setting 3.2294.15 to 1. The recorded value can be correlated with 3.2294.12 as a confirmation that the 10BASE-T1S OAM message is received by the link partner.

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45.2.3.58k.3 10BASE-T1S OAM message received (3.2294.13)

Bit 3.2294.13 shall indicate whether the most recently transmitted 10BASE-T1S OAM message with a toggle bit value in 3.2294.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.58k.4 Received message toggle value (3.2294.12)

Bit 3.2294.12 indicates the toggle bit value of the 10BASE-T1S OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2294.13 is 1.

45.2.3.58k.5 Message number (3.2294.11:8)

The 10BASE-T1S OAM message number to be transmitted. This field is user defined but is recommended that it be used to indicate the meaning of the 8 octet 10BASE-T1S OAM message. If used this way, up to 16 different 8 octet messages can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

45.2.3.58k.6 Ping received (3.2294.3)

Bit 3.2294.3 represents the value of the most recent Ping RX received from the link partner (see 97.3.8.2.3).

45.2.3.58k.7 Ping transmit (3.2294.2)

Bit 3.2294.2 represents the value to be sent to the link partner via the Ping TX function (see 97.3.8.2.4).

45.2.3.58k.8 Local SNR (3.2294.1:0)

Bits 3.2294.1:0 are set by the 10BASE-T1S PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.58l 10BASE-T1S OAM message register (Registers 3.2295 to 3.2298)

The 8 octet 10BASE-T1S OAM message data to be transmitted. The 8 octet message data is user defined and its definition is outside the scope of this standard.

Table 45–220k—10BASE-T1S OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2295.15:8	10BASE-T1S OAM message 1	Message octet 1. LSB transmitted first.	R/W
3.2295.7:0	10BASE-T1S OAM message 0	Message octet 0. LSB transmitted first.	R/W
3.2296.15:8	10BASE-T1S OAM message 3	Message octet 3. LSB transmitted first.	R/W
3.2296.7:0	10BASE-T1S OAM message 2	Message octet 2. LSB transmitted first.	R/W
3.2297.15:8	10BASE-T1S OAM message 5	Message octet 5. LSB transmitted first.	R/W
3.2297.7:0	10BASE-T1S OAM message 4	Message octet 4. LSB transmitted first.	R/W
3.2298.15:8	10BASE-T1S OAM message 7	Message octet 7. LSB transmitted first.	R/W
3.2298.7:0	10BASE-T1S OAM message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

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45.2.3.58m10BASE-T1S OAM receive register (Register 3.2299)

The assignment of bits in the 10BASE-T1S OAM receive register is shown in Table 45–220l

Table 45–220l—10BASE-T1L OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2299.15	Link partner 10BASE-T1S OAM message valid	This bit is used to indicate message data in registers 3.2299.11:8, 3.2287, 3.2288, 3.2289, and 3.2290 are stored and ready to be read. This bit shall self clear when register 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2299.14	Link partner toggle value	Toggle value received with message.	RO
3.2299.13:12	Reserved	Value always 0	RO
3.2299.11:8	Link partner message number	Message number from link partner	RO
3.2299.7:2	Reserved	Value always 0	RO
3.2299.1:0	Link partner SNR	00 = Link partner link is failing and will drop link and re-link within 2 to 4 ms after the end of the current 10BASE-S OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.58m.1 Link partner 10BASE-T1S OAM message valid (3.2299.15)

Bit 3.2299.15 shall be set to 1 when the 10BASE-T1S OAM message from the link partner is stored into registers 3.2287, 3.2288, 3.2289, and 3.2290 and the message number in 3.2299.11:8. This register shall be cleared when register 3.2390 is read.

45.2.3.58m.2 Link partner toggle value (3.2299.14)

Bit 3.2299.14 indicates the toggle value associate with the 8 octet 10BASE-T1S OAM message from the link partner.

45.2.3.58m.3 Link partner message number (3.2299.11:8)

The 10BASE-T1S OAM message number from the link partner.

45.2.3.58m.4 Link partner SNR (3.2299.1:0)

Bits 3.2299.1:0 indicate the status of the link partner receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.58n Link partner 10BASE-T1L OAM message register (Registers 3.2300 to 3.2302)

The 8 octet 10BASE-T1S OAM message data from the link partner. Register 3.2299.15 shall be cleared

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when register 3.2303 is read.

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78. Energy-Efficient Ethernet (EEE)

[Notes for editors (not to be included in the published draft - not even D1.0!)
Insert the headings and changes to Clause 30 below. For any existing heading, figure, table or equation include the cross-reference marker from Clause 30 in the base standard (as has been done for the Clause 30 heading above). If copying an existing heading, figure, table or equation to form the starting point for a new object do not copy the cross-reference marker. Include existing headings for each layer above the heading being inserted or modified.

78.1 Overview

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98. Auto-Negotiation for single differential-pair media

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98.1 Overview

98.1.1 Scope

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146. Physical Coding Sublayer (PCS), type 10BASE-T1

146.1 Overview

146.2 Physical Coding Sublayer (PCS)

146.3 10BASE-T1 Physical Coding Sublayer (PCS) functions

146.4 Protocol implementation conformance statement (PICS) proforma for Clause 146, Physical Coding Sublayer (PCS), type 10BASE-T1[1]

146.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 146, Physical Coding Sublayer (PCS), type 10BASE-T1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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146.4.2 Identification

146.4.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

146.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3xx-201x, Clause 146, Physical Coding Sublayer (PCS), type 10BASE-T1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-201x.)	

Date of Statement	

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146.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] No [ ]
					Yes [ ]

146.4.4 PICS proforma tables for clause title

146.4.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ]
					Yes [ ] No [ ]
					Yes [ ] No [ ] N/A [ ]

146.4.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]
					Yes [ ] No [ ] N/A [ ]

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147. Physical Medium Attachment (PMA) sublayer and baseband medium type 10BASE-T1L

147.1 Overview

147.1.1 10BASE-T1L architecture

147.1.1.1 Physical Medium Attachment (PMA) sublayer

147.1.1.2 Signaling

147.1.2 Conventions in this clause

147.1.2.1 State Diagram Notation

147.1.2.2 State Diagram Timer specifications

147.1.2.3 Service specifications

147.2 10BASE-T1L service primitives and interfaces

147.2.1 PMA service interface

147.2.2 PMA service interface

147.2.2.1 Semantics of the primitive

147.2.2.2 When generated

147.2.2.3 Effect of receipt

147.3 Physical Medium Attachment (PMA) Sublayer

147.4 PMA electrical specifications

147.5 Management interface

147.6 Link segment characteristics

147.7 MDI specification

147.8 Environmental specifications

147.9 Delay constraints

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147.10 Protocol implementation conformance statement (PICS) proforma for Clause 147, Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L[1]

147.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 147, Physical Medium Attachment (PMA) sublayer and baseband medium type 10BASE-T1L, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

147.10.2 Identification

147.10.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

147.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3xx-201x, Clause 147, Physical Medium Attachment (PMA) sublayer and baseband medium type 10BASE-T1L
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-201x.)	

Date of Statement	

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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147.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] No [ ]
					Yes [ ]

147.10.4 PICS proforma tables for clause title

147.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ]
					Yes [ ] No [ ]
					Yes [ ] No [ ] N/A [ ]

147.10.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]
					Yes [ ] No [ ] N/A [ ]

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148. Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S

148.1 Overview

148.1.1 10BASE-T1S architecture

148.1.1.1 Physical Medium Attachment (PMA) sublayer

148.1.1.2 Signaling

148.1.2 Conventions in this clause

148.1.2.1 State Diagram Notation

148.1.2.2 State Diagram Timer specifications

148.1.2.3 Service specifications

148.2 10BASE-T1S service primitives and interfaces

148.2.1 PMA service interface

148.2.2 PMA service interface

148.2.2.1 Semantics of the primitive

148.2.2.2 When generated

148.2.2.3 Effect of receipt

148.3 Physical Medium Attachment (PMA) Sublayer

148.4 PMA electrical specifications

148.5 Management interface

148.6 Link segment characteristics

148.7 MDI specification

148.8 Environmental specifications

148.9 Delay constraints

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148.10 Protocol implementation conformance statement (PICS) proforma for Clause 148, Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S[1]

148.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 148, Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

148.10.2 Identification

148.10.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

148.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3xx-201x, Clause 148, Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-201x.)	

Date of Statement	

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148.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] No [ ]
					Yes [ ]

148.10.4 PICS proforma tables for clause title

148.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ]
					Yes [ ] No [ ]
					Yes [ ] No [ ] N/A [ ]

148.10.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]
					Yes [ ] No [ ] N/A [ ]

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