Cl **120G** *SC* **120G.3.1.5** *P* **263** *L* **8** # 114

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **D** *pattern numbers*

Removing any mention of the pattern numbers that have been used for module testing for 20 years, 40GBASE-CR4 and 100GBASE-CR10, and AUIs 83E and 120E, is not warranted. There is no need for the writer to obstruct module professionals. As this annex uses several test patterns like an optical PMD, it should have a table of test patterns giving the pattern number, which this draft lacks, and description, and reference for definition.

SuggestedRemedy

After
All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q (see 120.5.11.2.1) or PRBS31Q (see 120.5.11.2.2) pattern
add
PRBS13Q is also known as pattern 4 and PRBS31Q is also known as pattern 3.
If it's worth repeating the references to 120.5.11.2.1 and 120.5.11.2.2 in 120G.3.2.2 (and it is, because a module professional doesn't have a specific reason to read 120G.3.1.5 Host output eye height and vertical eye closure (VEC)), add the same sentence there. It could be an informative NOTE. We could assume that someone using a stressed input section will read the section for one of the outputs, so I'm not asking to add the same information to the stressed input sections.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This comment is a restatement of D2.2 comment #119 with a modified suggested remedy. D2.2 comment #119 requested a table listing patterns and providing pattern numbers. There was no consensus by the task force to make the proposed changes.

However, the suggested remedy provides a different approach to resolving the concern.

The reference to pattern numbers is not necessary as this is not an optical interface. However, since the host output signal goes to the module optical output and the module output and comes from the module optical input it may be helpful to relate the pattern number with the pattern name for those interfaces.

Also in 120G.5.2 it might be helpful to point to the subclause that defines PRBS13Q.

For the first instance of PRBS13Q/PRBS31Q in 120G.3.1 and 120G.3.2 add a footnote pointing out that PRBS13Q is also referred to as Pattern 4 and PRBS31Q as Pattern 3 for PAM4 optical PMDs.

In 120G.5.2 on page 277 line 16 change "PRBS13Q" to "PRBS13Q (see 120.5.11.2.1)".

Implement with editorial license.

Cl **120G** *SC* **120G.3.3.5.1** *P* **268** *L* **45** # 118

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *HI SI PG output*

Before listing the impairments, this would be a good place to say that there is a pattern generator with adjustable amplitude, yet the four PAM4 levels are kept nominally (i.e. at low frequency) equally spaced.

SuggestedRemedy

Add sentence per comment. Similarly in 120G.3.3.4.1.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
The referenced Figure 120G-9 shows the presence of a pattern generator.

Adjustable amplitude is implicit in the calibration procedure in 120G.3.3.5.2.

However, it might be appropriate to formally constrain the relative level mismatch.

-- discussion not complete --

Strawpoll #19 (Chicago)
Strawpoll #20 (choose one)
I support using the following to constrain pattern generator level spacing using the following text (or similar):
A: no specification (per D2.2)
B: "The pattern generator output PAM4 levels are assumed to be equally spaced."
C: "The pattern generator output PAM4 levels are equally spaced."
D: "The pattern generator output PAM4 levels are equally spaced and if not the measurement must be appropriately adjusted."
E: "The pattern generator output level separation mismatch ratio R_LM (see 120D.3.1.2) is greater than or equal to TBD%."
F: "The pattern generator output level separation mismatch ratio R_LM (see 120D.3.1.2) is greater than or equal to TBD% and ES is 1/3 (see 120D.3.1.3) or higher."

SP #19: A: 1 B: 10 C: 7 D: 10 E: 10 F: 6
SP #20: A: 1 B: 4 C: 0 D: 6 E: 9 F: 2

Cl **120G** *SC* **120G.3.3.5.1** *P* **269** *L* **2** # 119

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *HI SI PG BW*

This used to say "corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input" because some pattern generators have jitter bandwidths around 100 MHz.

SuggestedRemedy

Before arbitrarily deleting technical content, I would like to hear from the PG companies and users if this is still a problem, and if it is, whether a tactic such as relying on the PG's own response with no extra filter is reasonable, or what to do.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

---- response updated 2021/10/12 ----

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

This comment pertains to the recipe for creating bounded
uncorrelated jitter. The concern is that, while D2.0 recommends a low-pass bandwidth range of 150-300 MHz and requires the BW to be within the frequency range of the test equipment, D2.2 rather requires the range to be in the 150-300 MHz range and says nothing about the test equipment bandwidth.

See slide 37 of the following presentation:
https://www.ieee802.org/3/ck/public/21_09/brown_3ck_02a_0921.pdf

The comment does not indicate that there is any issue with the current draft not does the suggested remedy provide an actionable remedy.

[Editor's note: Changed page from 268 to 269.]

Cl **120G** *SC* **120G.3.3.5.2** *P* **269** *L* **51** # 133

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *HI SI method*

Changing the "pattern generator [pre-]emphasis" in step g will change the pattern generator transition time from step a.
More generally, is asking the pattern generator for a particular edge speed reasonable, or should the calibration be based on the signal at TP4 rather than the signal at TP1 and the tolerances of the mated compliance boards (and the frequency-dependent attenuator, for module stressed input tolerance).

SuggestedRemedy

In step a, say that, exceptionally, this pattern generator transition time is defined for neutral emphasis at the pattern generator output.
Similarly in 120G.3.4.3.2.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

It might make sense to specify the pattern generator output equalization state for the transition time measurement. However, there is no explicit requirement for the pattern generator to support a neutral state as proposed nor is it clear how neutral emphasis is defined.

For task force discussion.

Cl **120G** *SC* **120G.3.4.3.2** *P* **274** *L* **1** # 111

Dawe, Piers
Nvidia

Comment Type **T** *Comment Status* **D** *MI SI FDA*

Table 162-20 contains parameters C0 and C1, which I believe should not be used here.

SuggestedRemedy

Say that parameters C0 and C1 do not apply.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

--- response updated 2021/1012 ---

The referenced equations 93A-13 and 93A-14 provide the s-parameters for only the PCB traces and do not include any variables relating to capacitors. However, it would be helpful to point out the intent to model a PCB transmission line without other impairments.

It was also noted that a value is not provided for the variable R0 which is necessary for calculations using the referenced equations. This is also relevant to 162.11.7.1 which references the same equations.

In 120G.4.3.2, change item ...

Change: "For the high-loss signal calibration, the frequency-dependent attenuator is configured such that the scattering parameters approximate those calculated from Equation (93A–13) and Equation (93A–14) using zp = 464 mm in length and the parameter values given in Table 162–20, representing ILdd from the output of the pattern generator to TP1a of 18.2 dB at 26.56 GHz."

To: "For the high-loss signal calibration, the frequency-dependent attenuator is configured such that the scattering parameters approximate those for a PCB transmission line calculated from Equation (93A–13) and Equation (93A–14) using zp = 464 mm in length and the relevant parameter values given in Table 162–20, representing ILdd from the output of the pattern generator to TP1a of 18.2 dB at 26.56 GHz."

In Table 162-20 add a row for R0 with a value of 50 Ohms.

[Editor's note: CC: 120G, 162]

Cl **120G** *SC* **120G.3.4.3.2** *P* **274** *L* **17** # 131

Dawe, Piers
Nvidia

Comment Type **T** *Comment Status* **D** *MI SI calibration*

This is open to misinterpretation: "For the high-loss case, the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to -13 dB. This restriction does not apply for the low-loss case." Even the previous text, "The CTLE setting, gDC+gDC2, has to be less than or equal to -13 dB" was misinterpreted to mean that there is no constraint on gDC + gDC2 for the low loss case. Yet the limits for the appropriate test point in Table 120G-11 still apply.
Actually, for a stressed signal calibration, we are looking for a signal where the optimum CTLE setting obeys the rules (so that the signal is not low stress but outside the expected range, but right stress and in the expected range).
See another comment for whether -13 dB is the right value.

SuggestedRemedy

Change "Eye height and VEC are measured at TP1a as described in 120G.5.2." to "Eye height and VEC are measured at TP1a as described in 120G.5.2, with an additional constraint for the high-loss case: the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 less than or equal to -13 dB."
Delete "For the high-loss case, the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to -13 dB. This restriction does not apply for the low-loss case."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

However, the proposed change is an improvement to the draft.

Note that the limit on the CTLE peaking gain may be modified by the resolution to comment #72.

Change "Eye height and VEC are measured at TP1a as described in 120G.5.2." to "Eye height and VEC are measured at TP1a as described in 120G.5.2 with the exception for the high-loss case that the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 less than or equal to -13 dB."

Delete "For the high-loss case, the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to -13 dB. This restriction does not apply for the low-loss case."

Cl **120G** *SC* **120G.3.4.3.2** *P* **274** *L* **17** # 72

Dudek, Mike — Marvell

Comment Type **TR** *Comment Status* **D** *MI SI calibration*

The optimum value of CTLE peaking (gdc+gdc2) when calibrating the high loss stressed module receiver test is only 10.5dB. See Dudek_3ck_01_0921. Requiring at least 13dB is degrading the signal making it difficult to generate the signal (see e.g. Snapshot of Receiver Module Input Tests (no convergence on high-loss TP1a channel) and private discussions). Note also that the maximum allowed peaking for testing the host output should not be significantly different from this value. A presentation will be made.

SuggestedRemedy

Change -13dB to -10.5dB. Also in Table 120G-11 change the gdc values for TP1a range for -1<GDC2 <0 to -2 to -11,
the range for -2<GDC2 <-1 to -4 to -10, and
the range for -3<GDC2 <-2 to -4 to -9

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

However, the proposed change is an improvement to the draft.

Comment #131 proposes changes to the wording to the text referenced in this comment.

The following related presentation was provided for review…
https://www.ieee802.org/3/ck/public/21_09/dudek_3ck_01_0921.pdf

Implement the suggested remedy.

For task force discussion.

Cl **120G** *SC* **120G.5.2** *P* **277** *L* **29** # 115

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **D** *EO RR gdc*

In D2.1, max gDC for TP4 near-end was increased from -2 to -1. While hosts typically have bigger packages and more trace loss than modules, neither is required (e.g. an on-board repeater).

SuggestedRemedy

Consider if max gDC for TP1a should be increased similarly.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The comment does not provide sufficient justification to implement the proposed changes nor does the suggested remedy provide sufficient detail to implement.

Cl **120G** *SC* **120G.5.2** *P* **277** *L* **32** # 100

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **D** *EO RR bbmax*

My recent simulations don't use gDC as strong as the table allows, but occasionally, the first DFE tap hits the limit of 0.4

SuggestedRemedy

Increase bbmax(1) from 0.4 to 0.5, increase the minimum for gDC at TP1a and TP4 long far end.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

The comment provides only annecdotal evidence for the bbmax change.

For related changes to gdc see responses to comments 72 and 99.

For task force discussion.

Cl **120G** *SC* **120G.5.2** *P* **277** *L* **38** # 98

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **D** *EO RR gdc*

The limits for TP4 gDC, gDC2 should not be the same for short and long output modes. Obviously, different channels will need different CTLE settings. Obviously, CTLE settings that only signals outside what the spec is designed for use, should be excluded, to make implementers set up their product correctly.

SuggestedRemedy

Create separate limits for TP4 short and long output modes, so 4 sets for TP4+, in the style of TP1a. If you don't have any better numbers, create them anyway with the same numbers in each set - but see another comment.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This comment is a restatement of D2.1 comment #103 and D2.0 comment #183, which were rejected on the basis of providing insufficient justification and detail.

This comment provides expanded justification.

Slides 7, 8, 11, 12 of the following presentation for a representation we reviewed by the task force.
https://www.ieee802.org/3/ck/public/21_09/kochuparambil_3ck_01a_0921.pdf

Slides 7, 8, and 11 of kochuparambil_01a provide a view the suggested remedy if implemented.

Task force discussion on the technical changes in the suggested remedy.

However, some related editorial changes as follows are an improvement to the draft.

Update style of the TP4 gdc specifications in Table 120G-11 as shown in the referenced slide 12 of kochuparambil_01a.

Cl **120G** *SC* **120G.5.2** *P* **277** *L* **46** # 99

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **D** *EO RR gdc*

As a lot of the channel for TP4 far-end is known exactly and the max loss to TP4 far end is less than to TP1a, the range of gDC, gDC2 combinations should be a subset of the TP1a ones.

SuggestedRemedy

For Continuous time filter, DC gain for TP4 far-end (gDC), change to sets of limits that depend on gDC2 in the same style as for TP1a. The allowed values should be subsets of those for TP1a. For TP4 long far end, use minimum gDC 1 dB higher than allowed for TP1a; for TP4 short far end, 3 dB higher than for TP1a.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This comment is a restatement of D2.1 comment #104 and D2.0 comment #178, which were rejected on the basis of providing insufficient justification and detail.

This comment provides no new justification, but does provide more details for implementation.

Cl **162B** *SC* **162B.1.3.4** *P* **298** *L* **30** # 136

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **D** *MTF RLcc*

Just as for the cable RLcc spec: this 3 dB becomes useless when the MCB trace loss is half of 3 = 1.5 dB (16 GHz).

SuggestedRemedy

As for the cable RLcc spec but 1 dB lower to 30 GHz, easing up to 50 GHz: 12 -9f dB 0.01 <= f <1, 3 dB 0.5<= f <= 4 GHz, 2.6+0.1*f dB 4< f <= 30 GHz, 9.5-1.3*f dB 30< f <= 50 GHz. f is in GHz.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This comment was reopened on 2021/10/5.

There appeared to be a major error in the suggested remedy referenced in the accepted resolution.

Slide 9 in the following presentation illustrates the correct equation.
https://www.ieee802.org/3/ck/public/21_09/diminico_3ck_01b_0921.pdf

?Implement the equation provided in the bottom right of slide 19 in the referenced presentation.?

For task force discussion.

Straw poll #xxx. (direction)
For the MTF RLcc specification, I support
A: no change (same as draft 2.2)
B: revised equation in slide 9 of diminico_01b
C: other revised equation TBD
A: B: C:

Straw poll #xxx (decision)
I support closing comment 136 using <TBD>.

--- reopened ---

Per straw poll #7 there is sufficient consensus to make the proposed changes in the suggested remedy.

Implement the suggested remedy with editorial license.

Straw poll #7 (decision)
I support adopting the suggested remedy in comment #136.
Yes: 12
No: 10