100 Gb/s/lane chip-to-module interface simulation analysis

Adam Healey and Cathy Liu

IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force
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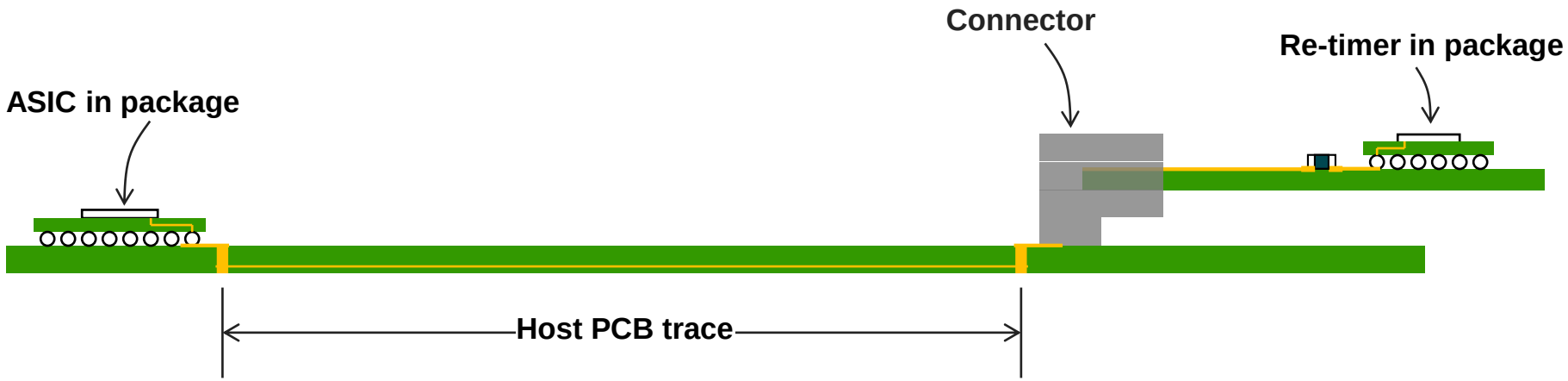
Key attributes of previous chip-to-module interfaces



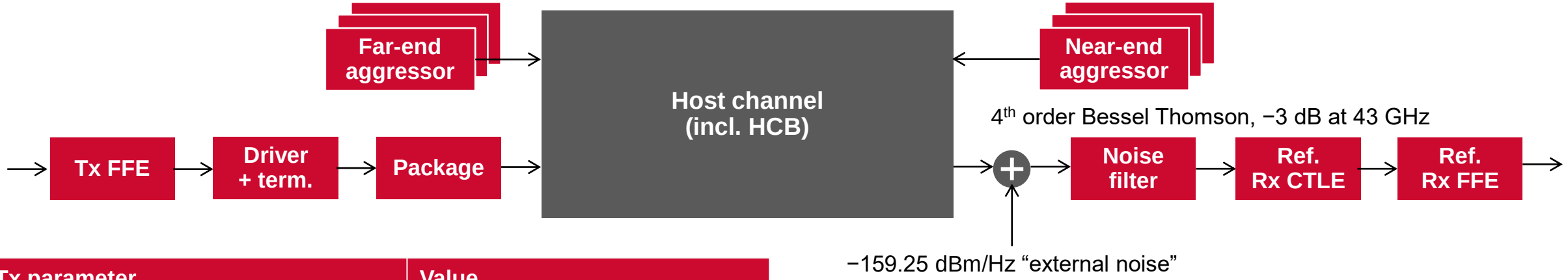
- Module reference receiver is a simple continuous-time linear equalizer (CTLE)
  - Low-power interface seen as critical to meeting stringent module power budgets
- Interface is symmetric in that the same reference receiver is used for module and host
  - Enables lower-power hosts
- Interface target BER supports “end-to-end” forward error correction with optical PMDs
- Host channel is compatible with passive “direct attach” copper cable medium

100 Gb/s/lane chip-to-module interface

- Low-power host interface is critical to meeting stringent module power budgets
  - However, there is a demand for a larger host insertion loss budget as a consequence of the higher (2x) signaling rate
  - More complex reference receivers are being considered [1].
- There is continued value in having a symmetric interface
- Support for the “end-to-end” FEC model supported by the Annex 120E interface is strongly desired
- A simulation model will be used to explore whether or not these key attributes of previous chip-to-module interfaces can be preserved for 100 Gb/s/lane

[1] Miyaoka and Sakai, “Consideration on 100Gb/s C2M SerDes Equalizer”, May 2018.

Simulation model



Tx parameter	Value
FFE number of coefficients	2 pre, 1 post
FFE coefficient ranges	[0, 10%], [−25%, 0], [−25%, 0]
FFE coefficient step size	2.5%
Differential output voltage, pk-to-pk	800 mV [a]
Level separation mismatch ratio	0.95
Signal-to-Noise-and-Distortion ratio	33 dB (at TP0 [b])
Even-odd jitter, pk-to-pk	19 mUI
Bounded uncorrelated jitter, pk-to-pk	40 mUI (sinusoid)
Random jitter, RMS	10 mUI
Termination	Design extracted
Package	Design extracted, 3 dB and 5 dB

Reference Rx parameter	Value
CTLE reference	Annex 120D
CTLE gDC	0 to -15 dB, 1 dB steps
CTLE gDC2	0 to -4 dB, 1 dB steps
Normalized poles, zeros	[1/2.5, 1/80, 2], [1/2.5, 1/80]
FFE number of coefficients	0 pre, 4 post
FFE coefficient ranges	+/-20%, +/-20%, +/-10%, +/-10%
FFE coefficient step size	2%

[a] At driver and termination output with no equalization.

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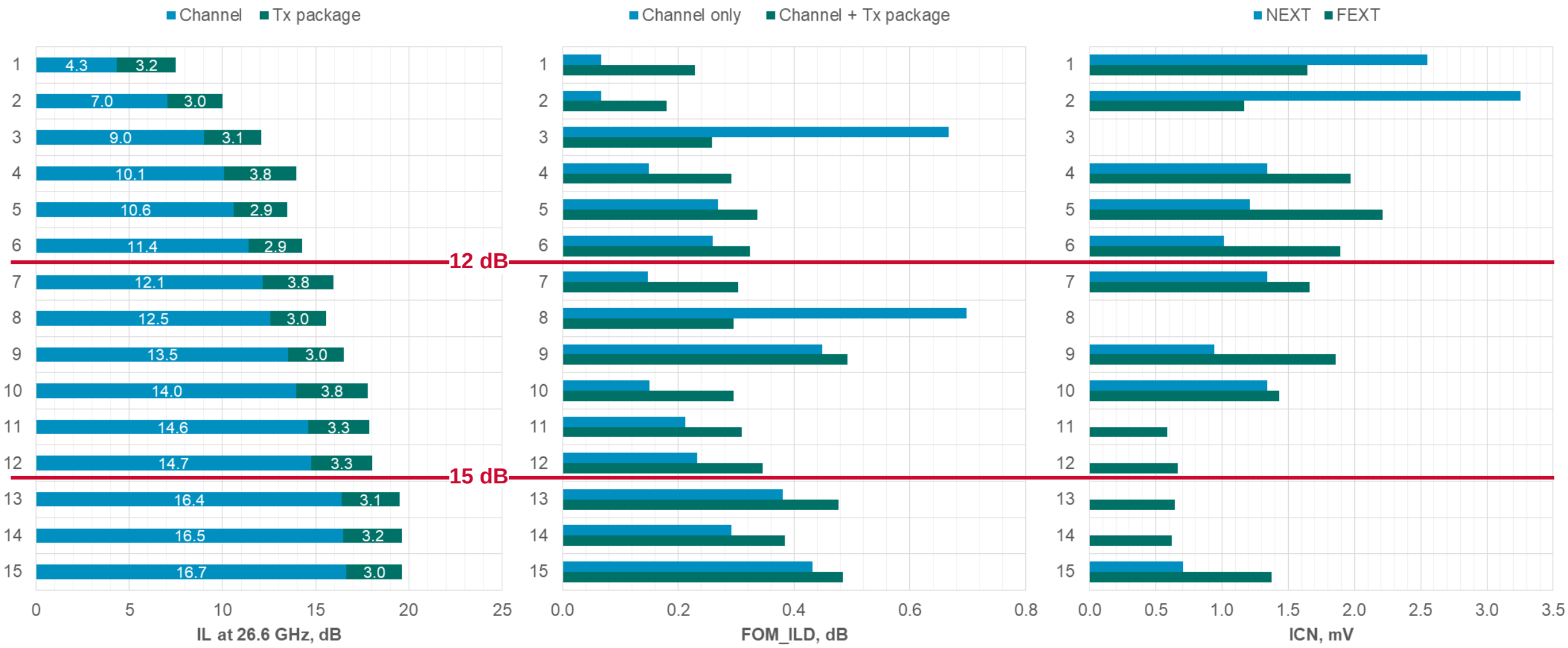
Host-to-module channels considered

#	Description
1	MCB
2	5” host PCB
3	No information
4	Lim, 10 dB channel (link)
5	QSFP-DD, 9” 34AWG cable
6	QSFP-DD, 12” 34AWG cable
7	Lim, 12 dB channel (link)
8	No information
9	QSFP, 22” 30 AWG cable
10	Lim,14 dB channel (link)
11	Tracy, 8.5” PCB, micro-via, Rx6 (link)
12	Tracy, 8.5” PCB, micro-via, Rx5 (link)
13	Tracy, 8.5” PCB, “long barrel”, Tx6 (link)
14	Tracy, 8.5” PCB, “long barrel”, Tx5 (link)
15	QSFP, 40” 30AWG cable

Channel information: 3 dB package trace



NOTE: Tx package FEXT is included in the SNDR parameter.

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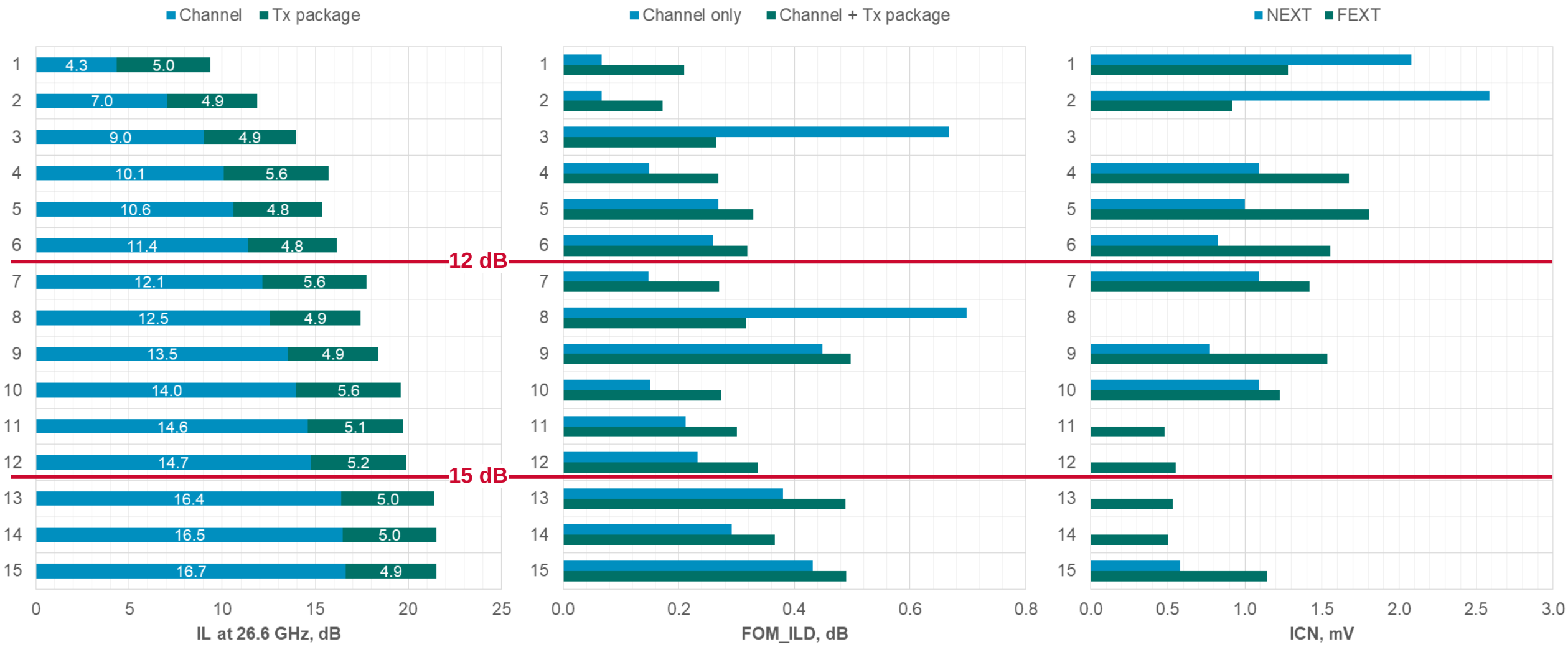
Channel information: 5 dB package trace



NOTE: Tx package FEXT is included in the SNDR parameter.

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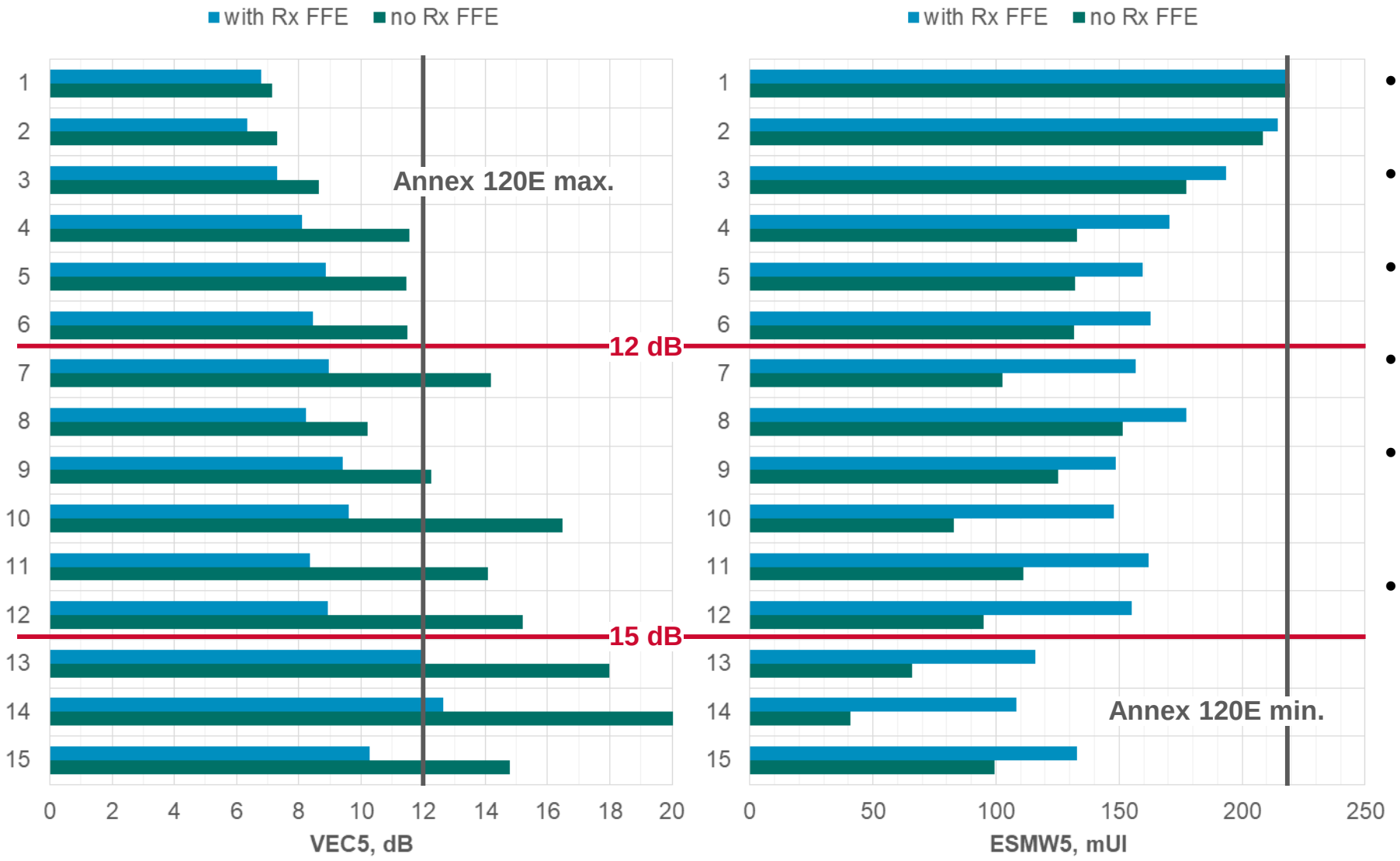
Eye quality metrics and equalizer optimization

- Eye height and eye width measured at PAM4 symbol error ratio = 1e−5
- Eye quality metrics
  - Vertical eye closure (VEC) instead of eye height since eye height is a strong function of the gain of reference receiver
  - Eye symmetric mask width (ESMW) is always less than or equal to eye width
- The test pattern is random data
- Tx FFE and Rx FFE are optimized to minimize ISI
- Rx CTLE optimized to maximize the product of 10^(−VEC/20) and ESMW

Impact of removing Rx FFE: 3 dB package trace



- The “no Rx FFE” case reduces the CTLE gain step to 0.5 dB
- This aligns with the Annex 120E reference receiver
- Annex 120E ESMW limit is not met for most cases
- A new limit may be needed for 100 Gb/s/lane
- Annex 120E VEC limit met for insertion loss up to 12 dB even without Rx FFE
- Rx FFE is needed to meet the VEC limit for insertion loss up to 15 dB

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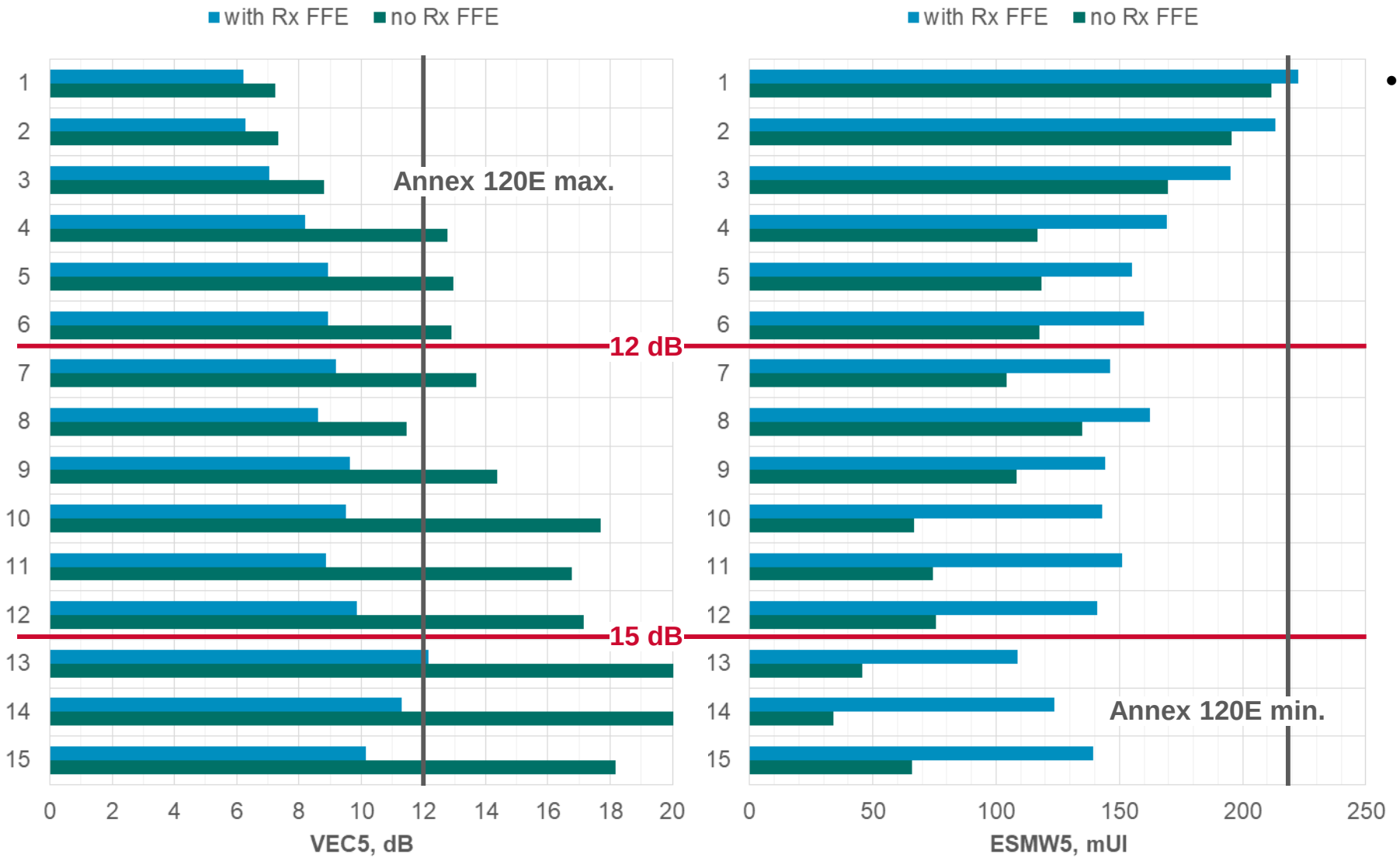
Impact of removing Rx FFE: 5 dB package trace



- The higher host package loss causes to “CTLE only” case to exceed the VEC limit for some channels with insertion loss in the vicinity of 12 dB

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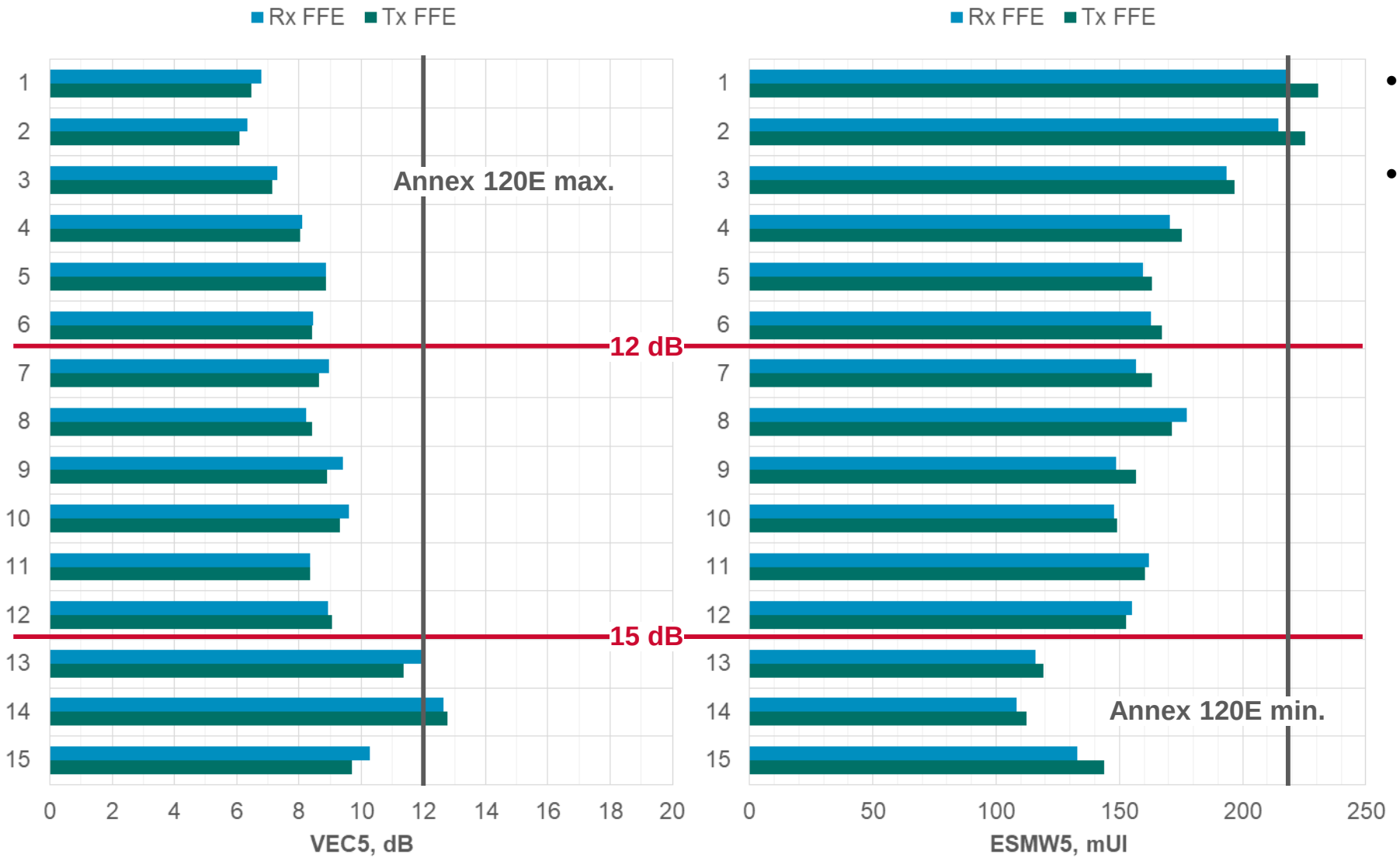
Equalizer optimization and eye quality metrics

- Rx FFE improves the quality of the eye produced by the reference receiver
- It does not necessarily align with low-power implementation as desired
- Can the performance be recovered with extension of the Tx FFE?
- Remove the Rx FFE and change the Tx FFE configuration as follows
  - FFE number of coefficients: 2 pre, 4 post
  - FFE coefficient ranges: [0, 10%], [−20%, 0], +/−20%, +/−20%, +/−10%, +/−10%
  - FFE coefficient step size: 2%

Comparison of Tx and Rx FFE: 3 dB package trace



- The “Tx FFE” case reduces the CTLE gain step to 0.5 dB
- Partly responsible for “Tx FFE” slightly outperforming “Rx FFE” for most of the cases

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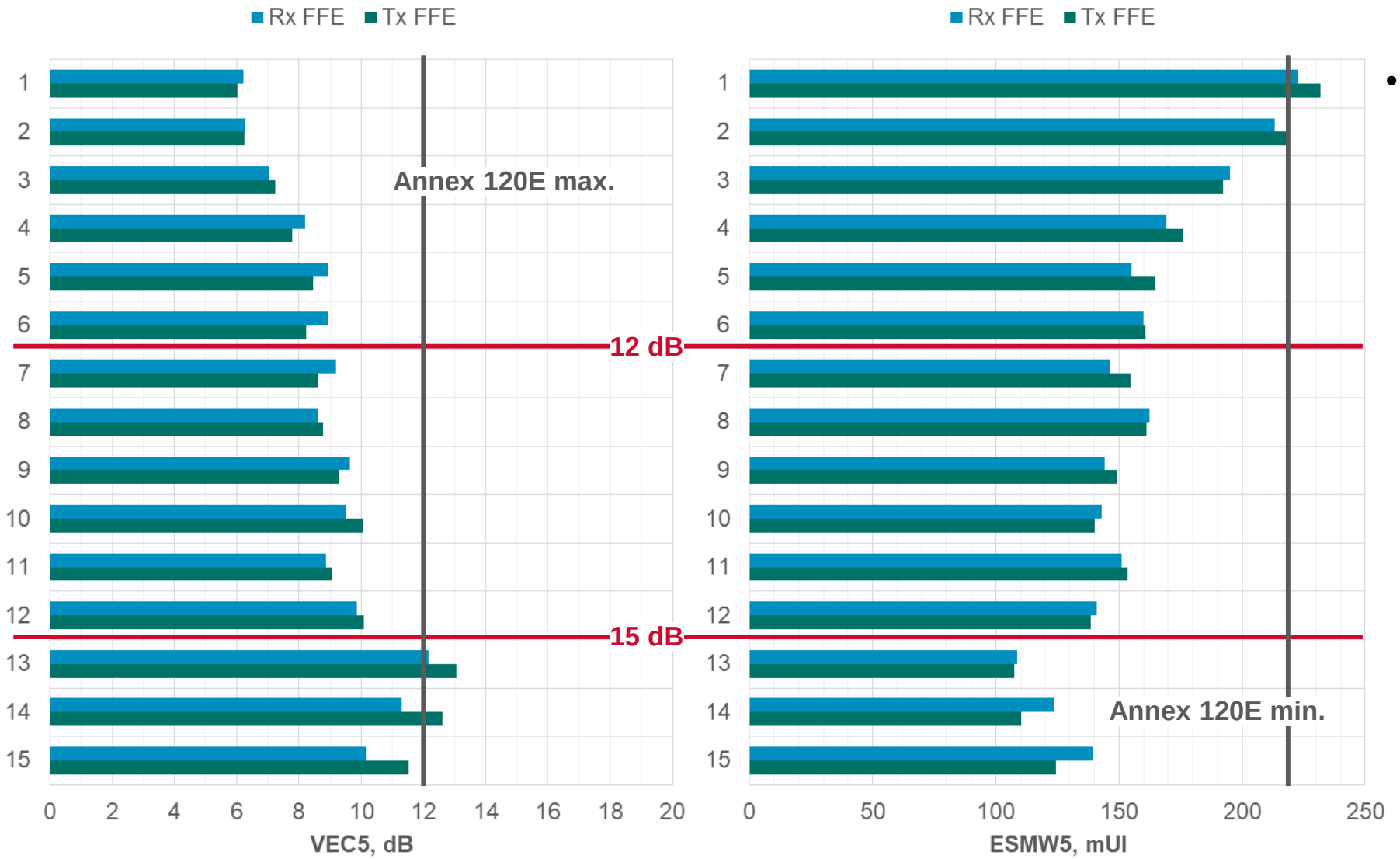
Comparison of Tx and Rx FFE: 5 dB package trace



- For both cases, reduced impact from higher package loss

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Summary and conclusions

- IEEE P802.3ck should define a reference receiver for chip-to-module that is conducive to a low-power implementation
  - Minimize the impact of the interface on the module power budget
- The chip-to-module interface should also be symmetric to enable a similar low-power implementation in the host
- Simulations suggest that these objectives can be satisfied under appropriate constraints
  - E.g., ~12 dB host channel insertion loss with ~3 dB Tx package allocation [2]
  - Constraints also serve to extend reach for “direct attach” passive copper cable
- Extensions to the Tx FFE can improve margin and/or increase the loss budget (channel and/or package) while keeping a simpler reference receiver

[2] Lim et al., “100GEL C2M Channel Reach Options & System Design Impacts”, May 2018.

Next steps

- Eye opening sensitivity to the Tx FFE coefficient values must be assessed
- Additional work must be done to determine the appropriate limits for the eye opening at TP1a