

Reference Architecture Proposals and Channel Data

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Outline

- ❑ 4 COM architectures
- ❑ Data for each architecture vs a collection of channels
- ❑ Next steps

4 Signal Architecture Approaches

1. Zero Forced DFE
2. Quantized Forced DFE
3. One DFE tap and a number of (Rx)FFE taps
4. One DFE tap and a number of (Rx)FFE taps with gain at cursor

COM is based on the pulse response (Annex 93A)

- Thru (ISI) channel response is $h^{(0)}(t)$ i.e. the pulse response

The pulse response $h^{(k)}(t)$ is derived from the voltage transfer function $H^{(k)}(f)$ (see 93A.1.4) using Equation (93A-24).

$$h^{(k)}(t) = \int_{-\infty}^{\infty} X(f)H^{(k)}(f)\exp(j2\pi ft)dt \quad (93A-24)$$

- The following uses pulse response plots to describe COM equalization

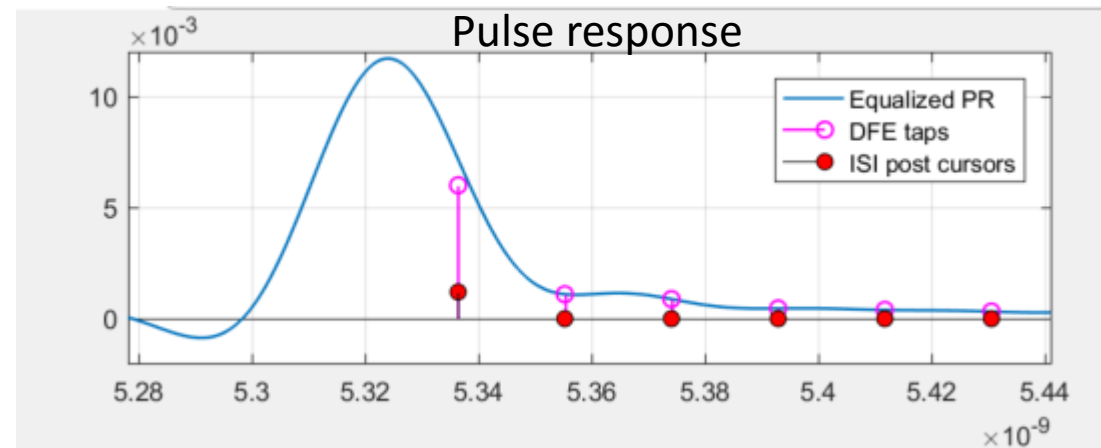
Zero Forced (ZF) DFE

$$FOM = 10\log_{10}\left(\frac{A_s^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2}\right) \quad (93A-36)$$

The FOM is calculated for each permitted combination of $c(-1)$, $c(1)$, and g_{DC} values per Table 93A-1. The combination of values that maximizes the FOM, including the corresponding value of t_s , is used for the calculation of the interference and noise amplitude in 93A.1.7 and the calculation of COM in 93A.1.

- ❑ All legal Tx FFE and CTF (continuous time function) settings are considered
 - Called a full grid search
 - Caveat: Very often CTF settings dominate over the Tx FFE post cursor.
- ❑ Exception: Samples corresponding to DFE cursor of is $h^{(0)}(t)$ greater than certain values (b_{max}) are converted in to ISI noise

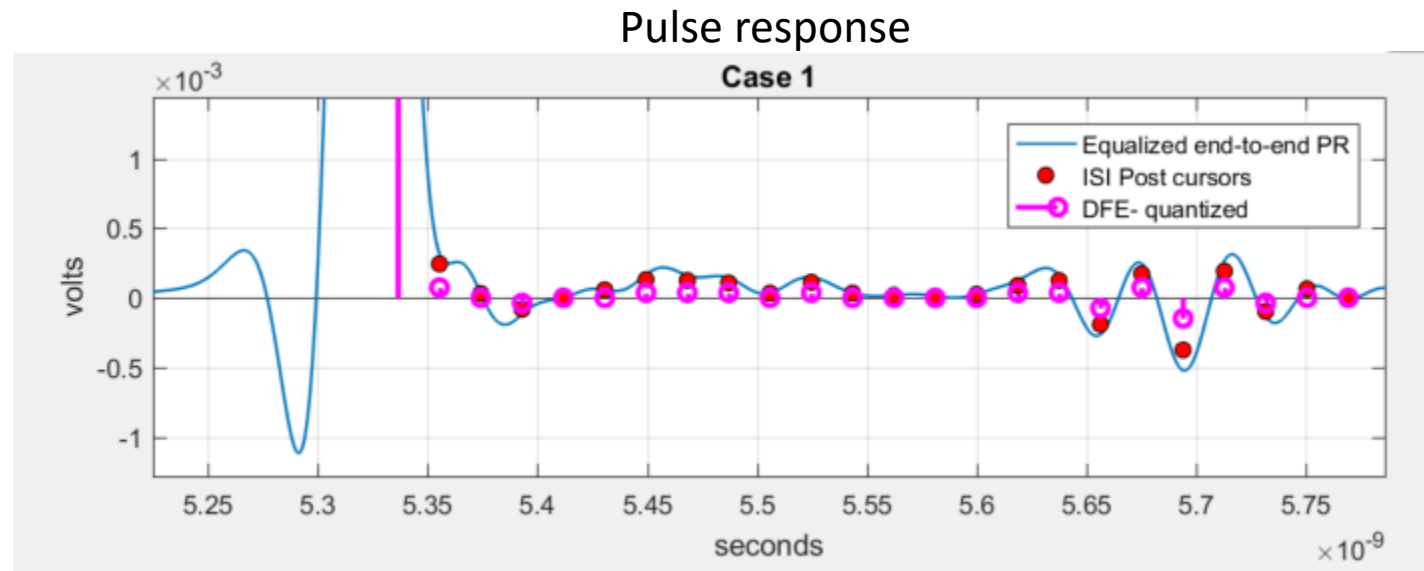
Example where 1st DFE tap reach limit creating ISI noise



Quantized DFE

□ Same as Zero force except:

- Samples corresponding to a DFE cursor $h^{(0)}(t_n)$ greater than the DFE quantization step size are also converted into ISI noise



One DFE tap + (Rx)FFE

□ Same full grid as for zero forced DFE except

- 1 tap of DFE w/ an Rx FFE of a specified number and resolution of pre-cursors and post-cursors are determined from a vector forced optimization.
 - The cursor for the vector forcing is $h^{(0)}(t_s)$ where t_s is the sample point and
 - The first post cursor is set the maximum allowed setting (b_{\max})
- $C = ((HH' * HH) ^{-1} * HH')' * FV'$;
 - C are the Rx FFE taps HH is derived from $h^{(0)}(t)$
 - FV is the forcing vector , $FV = [\dots 0, 0, A_s, b_{\max}(1)*A_s, 0, 0, 0, 0\dots]$
- FOM is computed from each CTF and Tx FFE setting with
- $h_{\text{fferx}}(f)$ is computed from the C found as in eq 93A-32

$$H_{\text{ffe}}(f) = \sum_{i=-1}^1 c(i) \exp(-j2\pi(i+1)(f/f_b)) \quad (93A-21)$$

□ FFE(3,32) used here for now

- 3 precursors and 32 post cursors

One DFE tap + (Rx) FFE w/ Cursor Gain

□ Same as one DFE tap and a number of Rx FFE taps (pre and post cursor) except:

- The cursor for the vector forcing ($h^{(0)}(t_s)$ where t_s is the sample point) has some gain
- $C = (HH' * HH)^{-1} * HH' * FV'$;
 - C are the Rx FFE taps HH is derived from $h^{(0)}(t)$
 - FV is the forcing vector , $FV = [\dots 0, 0, A_s * 10^{\frac{gain}{20}}, b_{max}(1) * A_s, 0, 0, 0, 0 \dots]$
 - 3 dB gain seems to work best

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 30]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.28:0.025:0]		[min:step:max]
c(-2)	[0:0.05:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	[-0.05:0.025:0]		[min:step:max]
g_DC	[-20:1:10]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
A_v	0.41	V	tdr selected
A_fe	0.41	V	tdr selected
A_ne	0.6	V	tdr selected
L	4		
M	32		
N_b	32	UI	
N_b_step	0		normalized
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	8.20E-09	V ² /GHz	
SNR_TX	32.5	dB	tdr selected
R_LM	0.95		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100G_Study_Group_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_Study_Group	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	6.16E-03	ns
FORCE_TR	1	logical

Non standard control options		
COM_CONTRIBUTION	0	logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.0189	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.18	
fixture delay time	0	
Rx FFE		
ffe_pre_tap_len	0	UI
ffe_post_tap_len	0	UI
ffe_tap_step_size	0.01	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.1	

N_b	32	UI	
N_b_step	0.0115		normalized

Q DFE

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)

Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

COM config sheet for ZF or Q DFE

Set to zero

For reference

Table 93A-1 parameters

Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 30]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.28:0.025:0]		[min:step:max]
c(-2)	[0:0.05:0.1]		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	[-0.05:0.025:0]		[min:step:max]
g_DC	[-20:1:10]	dB	[min:step:max]
f_z	21.25	GHz	
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f_p2	53.125	GHz	
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M	32		
N_b	1	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	8.20E-09	V^2/GHz	
SNR_TX	32.5	dB	tdr selected
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Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2

g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100G_Study_Group_(date)\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CK_100GEL	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	6.16E-03	ns
FORCE_TR	1	logical

Non standard control options		
COM_CONTRIBUTION	0	logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.0189	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.18	
fixture delay time	0	

Rx FFE		
ffe_pre_tap_len	3	UI
ffe_post_tap_len	32	UI
ffe_tap_step_size	0.01	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.1	
crusor_gain	0:1:4	dB

Set to zero for no gain

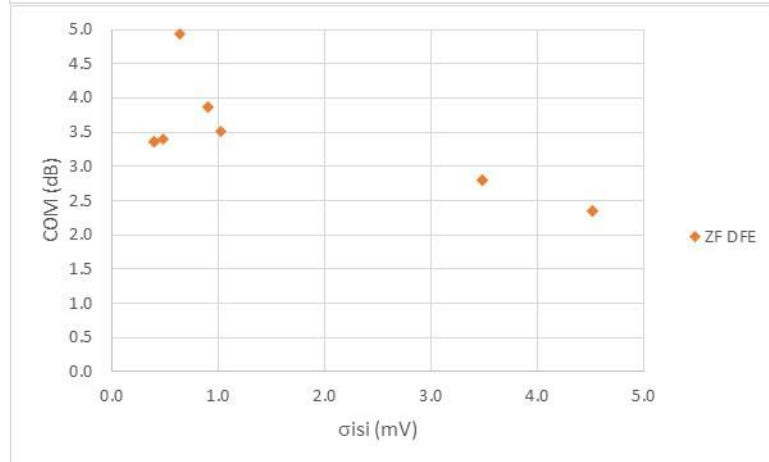
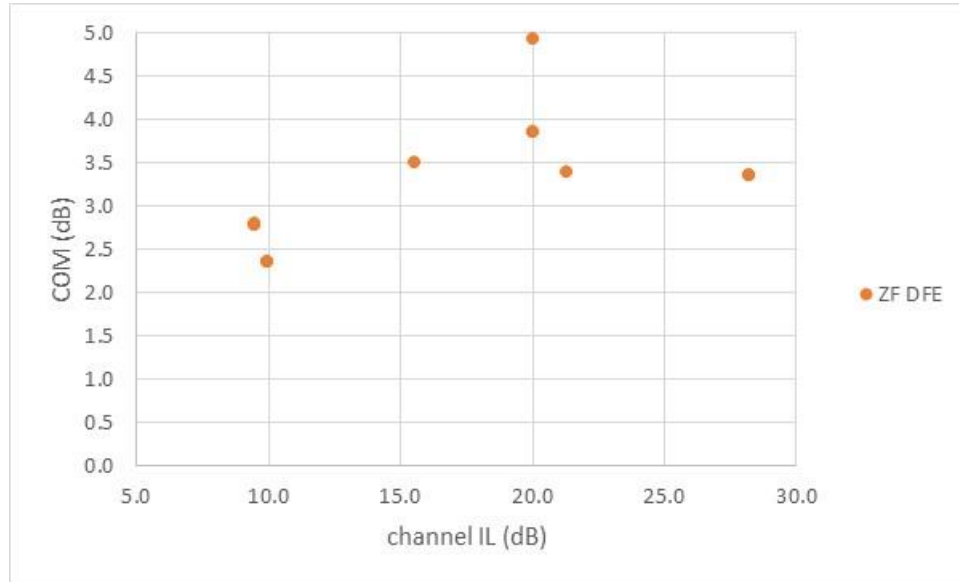
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z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

COM config sheet for FFE and w/wo gain

For reference

Reference: ZF DFE



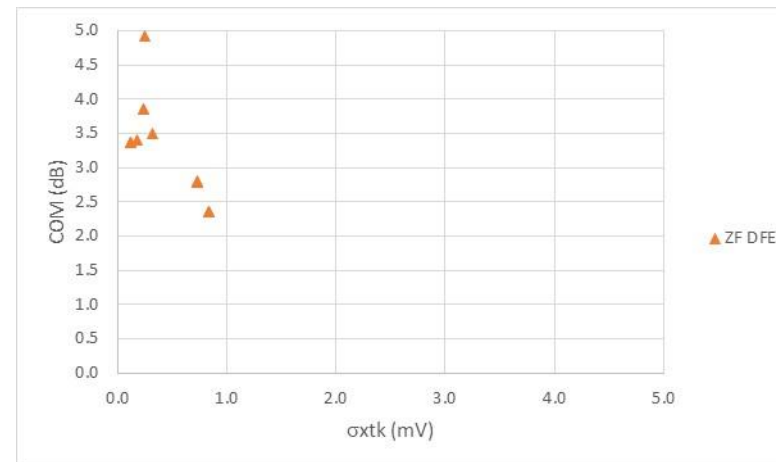
Channels:

- Cabled backplane (2)
- Cabled fabric switch (12)

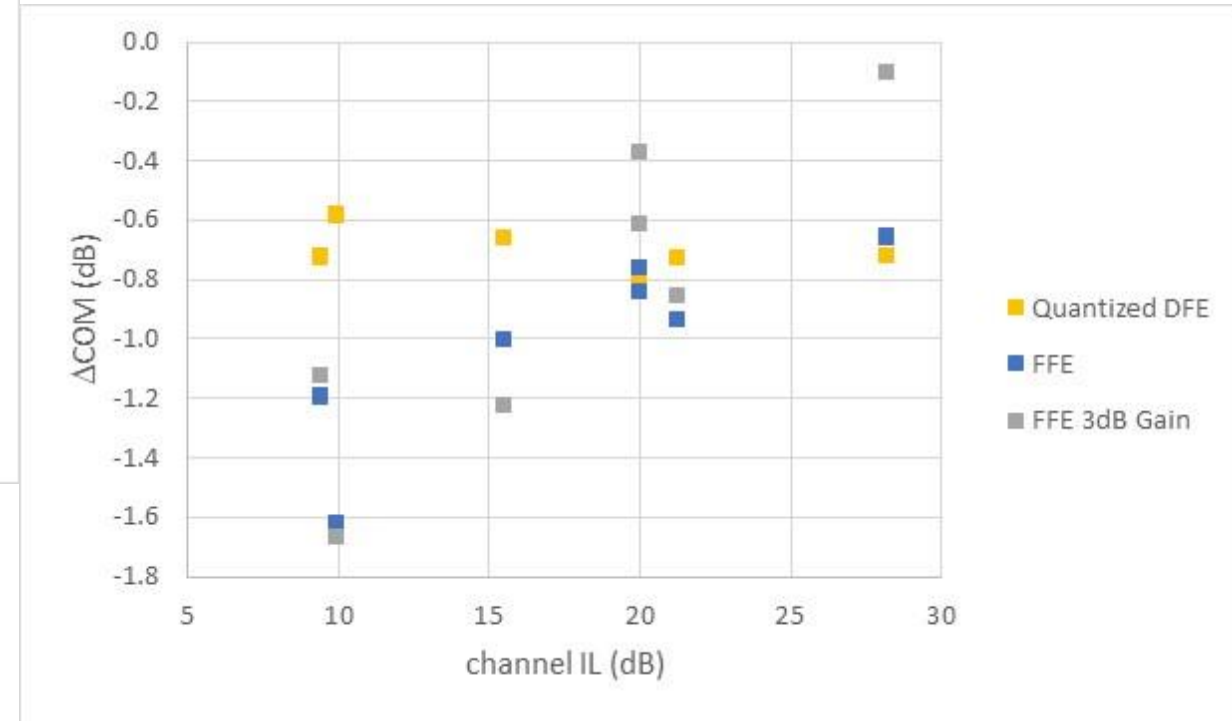
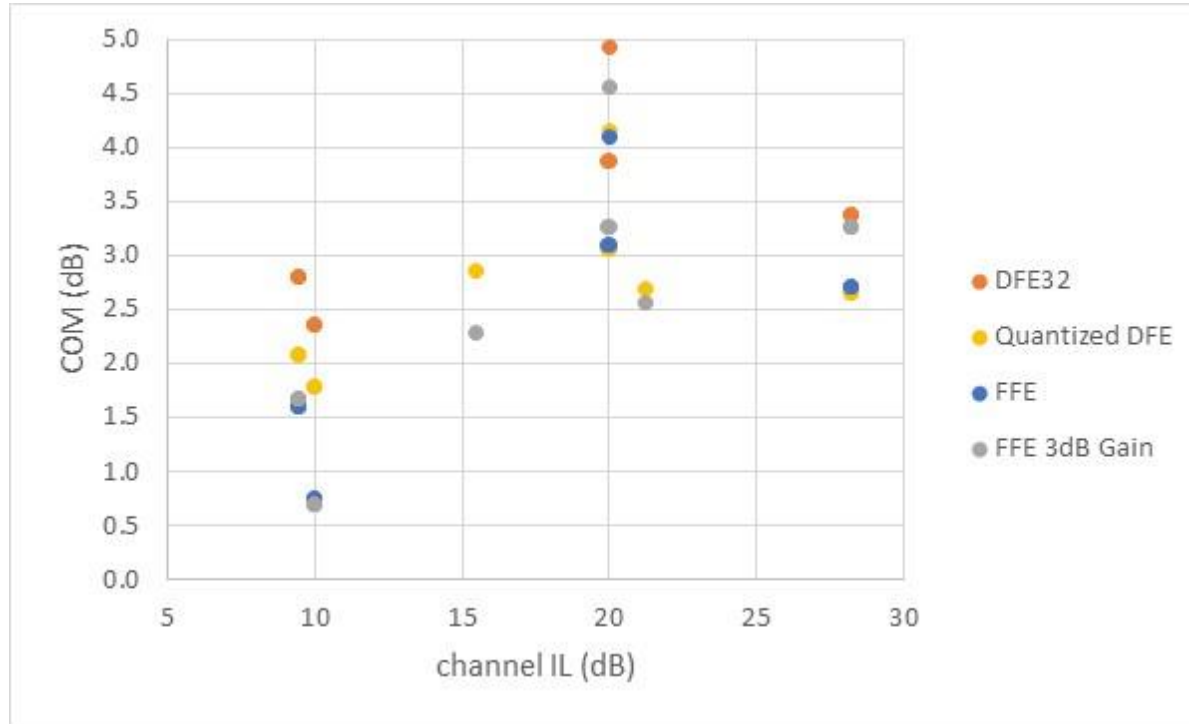
Used channels with $COM \geq 2.3\text{dB}$

Analysis used 32 taps total (DFE+FFE or DFE-only)

- Is the ZF DFE too optimistic
- Does the implication of the ZF DFE require too much power



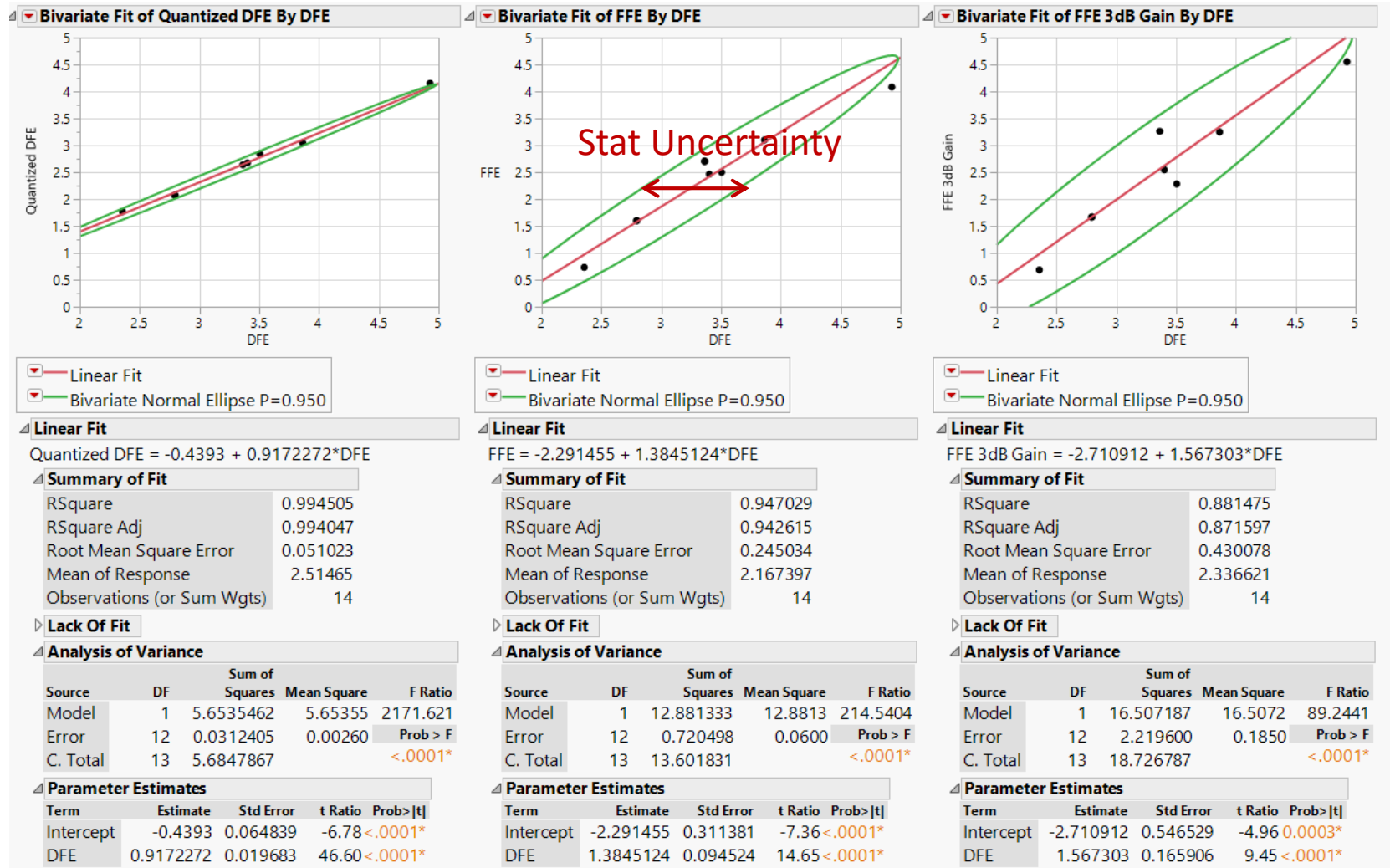
Data Summary



- Quantized DFE seems like just derating COM of the ZF DFE
- FFE with gain seems to get closer to ZF DFE for high loss

COM Correlations to DFE-based COM

More variability
for the FFE based
COM



X and Y
axis are dB
of COM

Summary & Next Steps

- ❑ Reference EQ architecture choices impact on COM results
- ❑ More variability in results with DFE+FFE-based reference EQ
- ❑ Is a quantized DFE good enough?
 - It seems like it is the same as raising the COM threshold
- ❑ Follow-on work
 - Assess the sensitivity to # of taps in the Rx Equalizer
 - Look at algorithm to better optimize gain in FFE; goal being to reduce uncertainty in results
- ❑ Follow-work for channels: Address PCB manufacturing to further reduce the channel ISI.

Backup

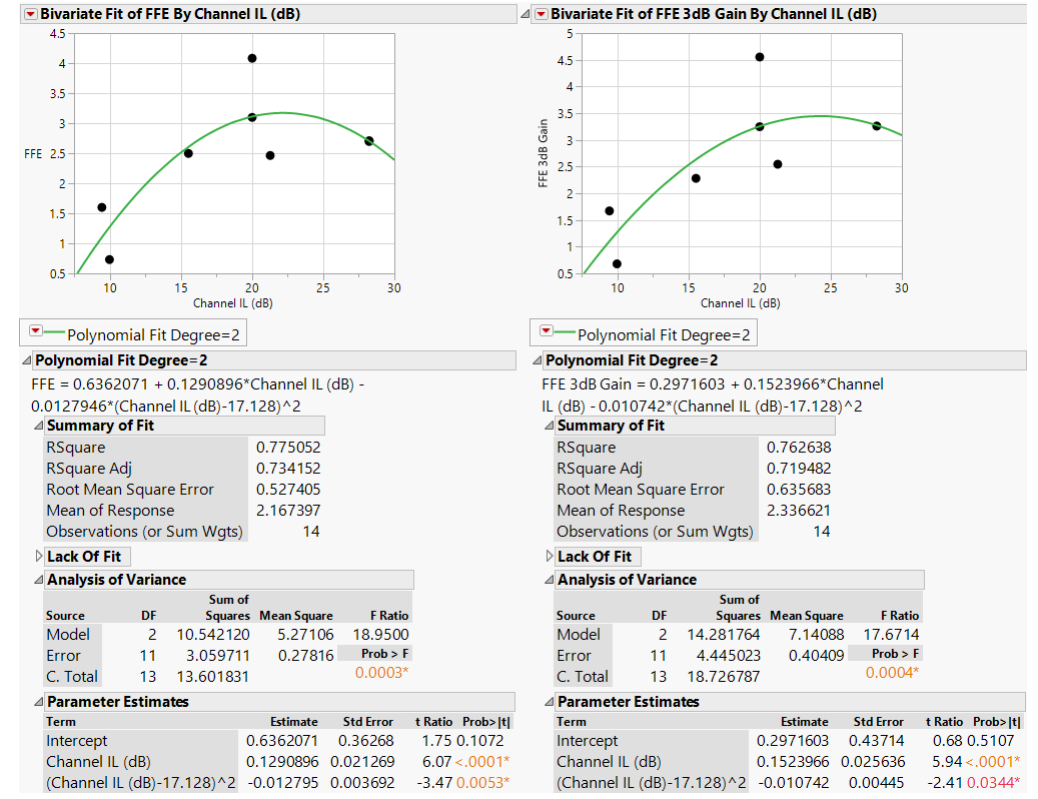
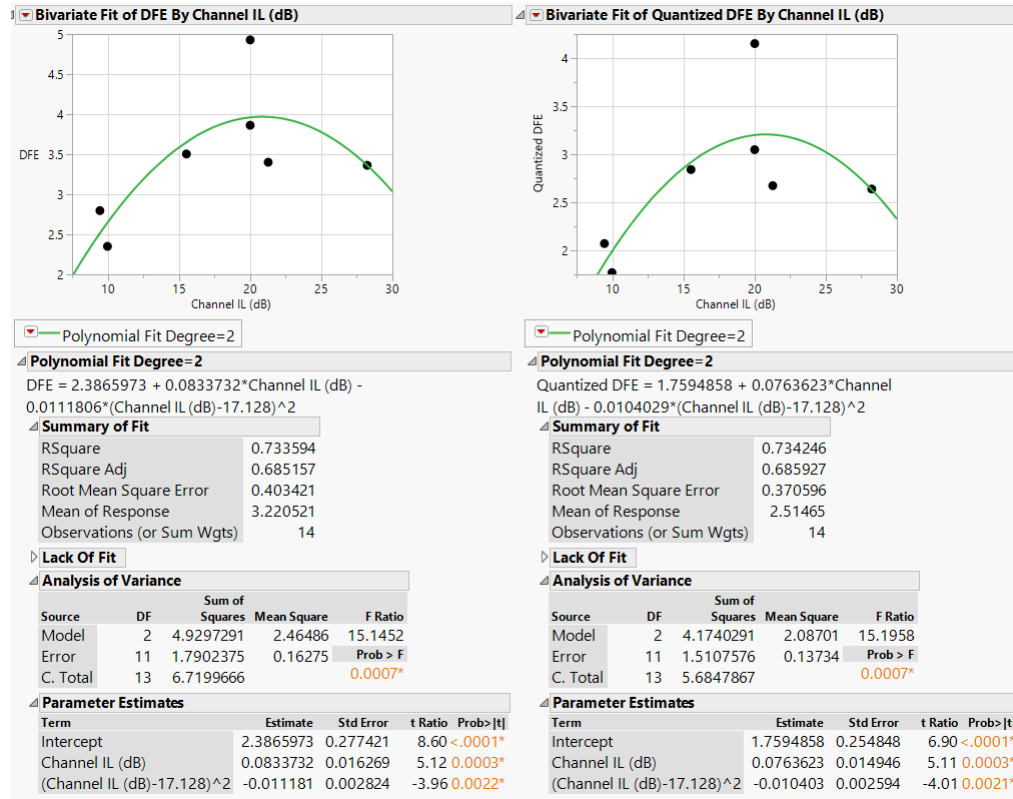
COM vs Channel IL

ZF DFE

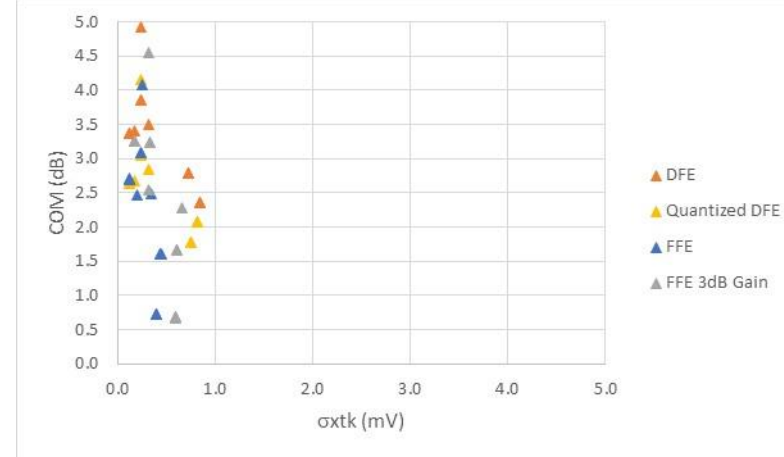
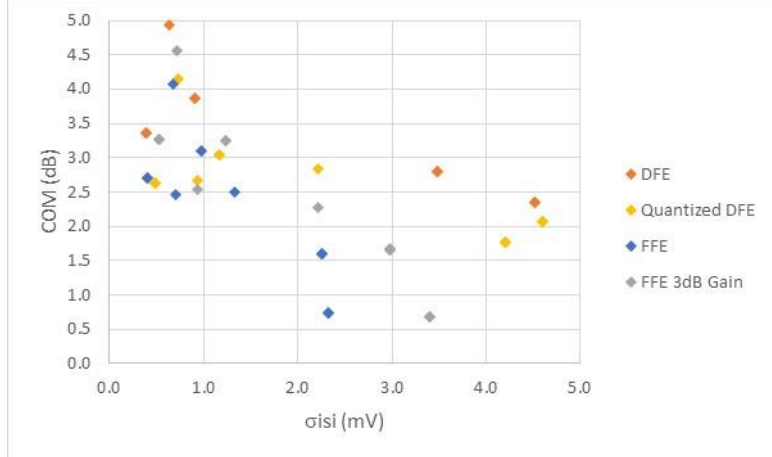
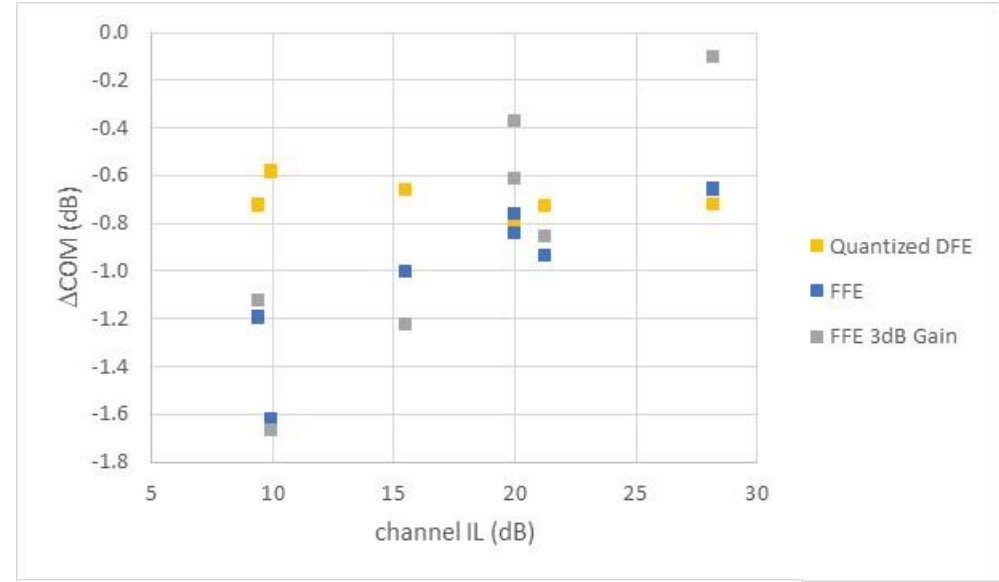
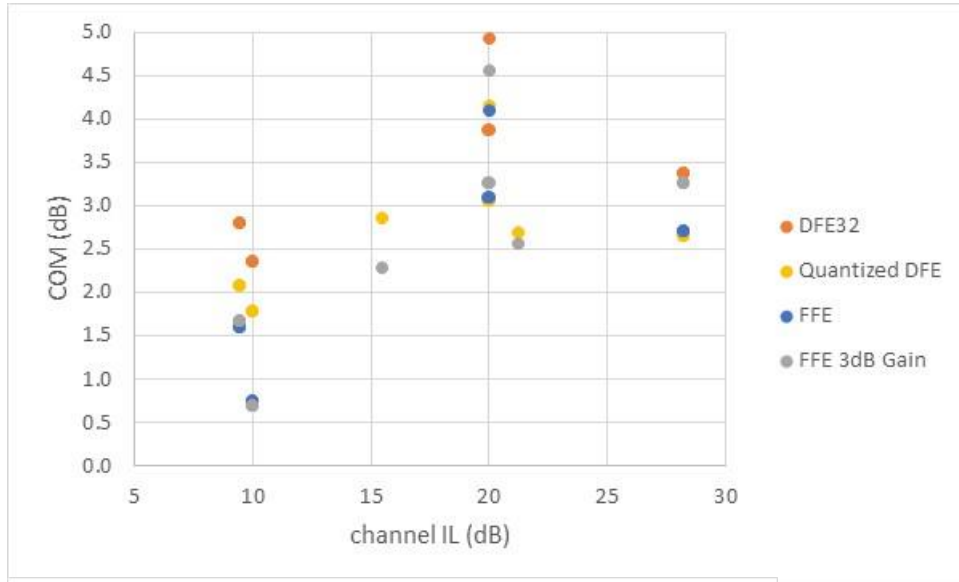
Quantized ZF DFE

DFE+FFE

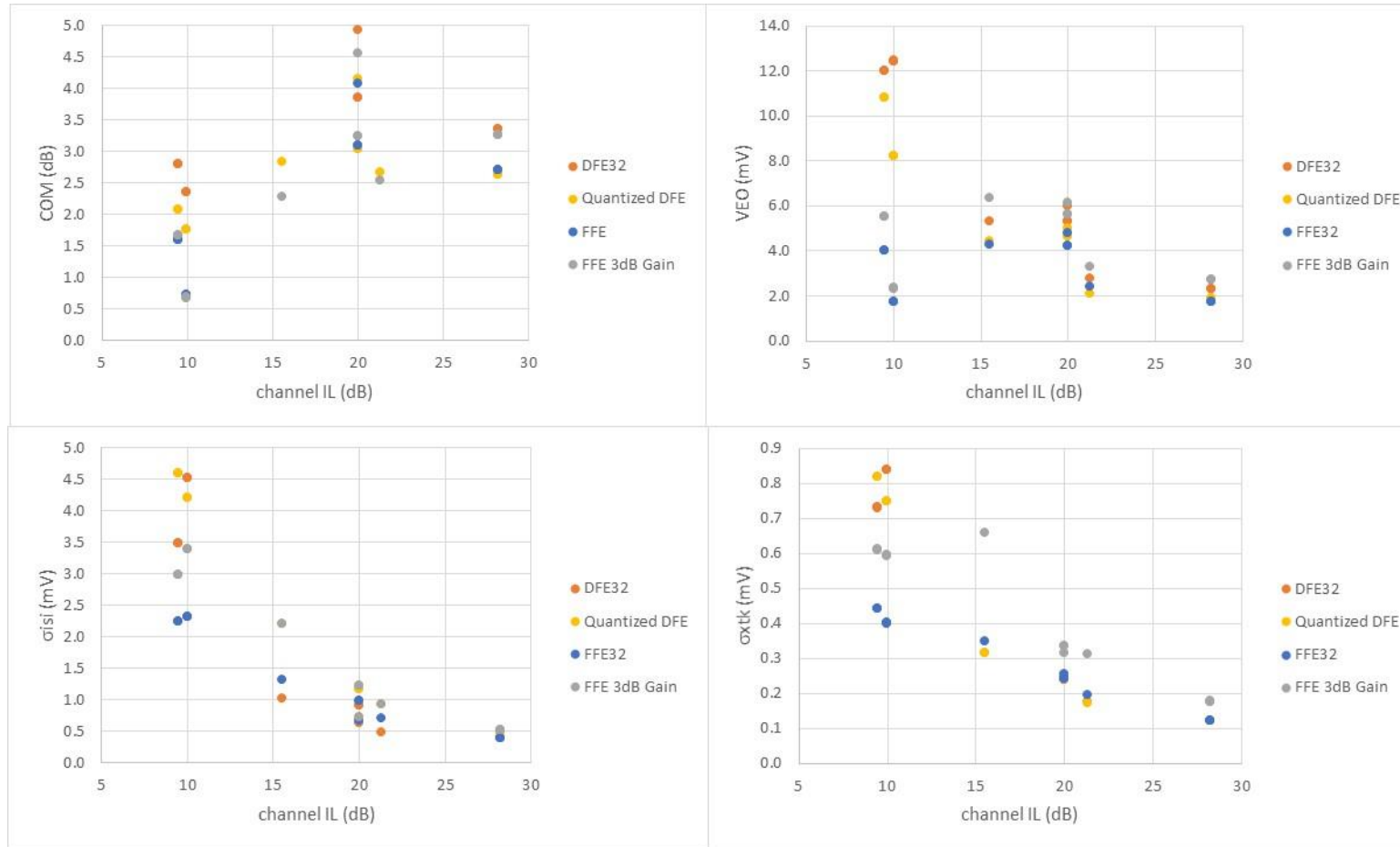
DFE+FFE w/ Gain



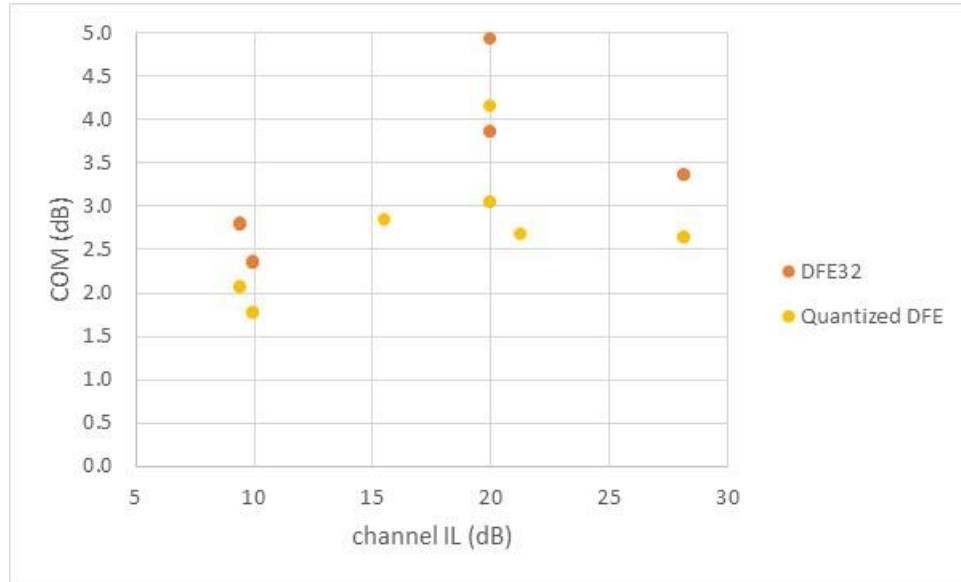
Consolidated Data



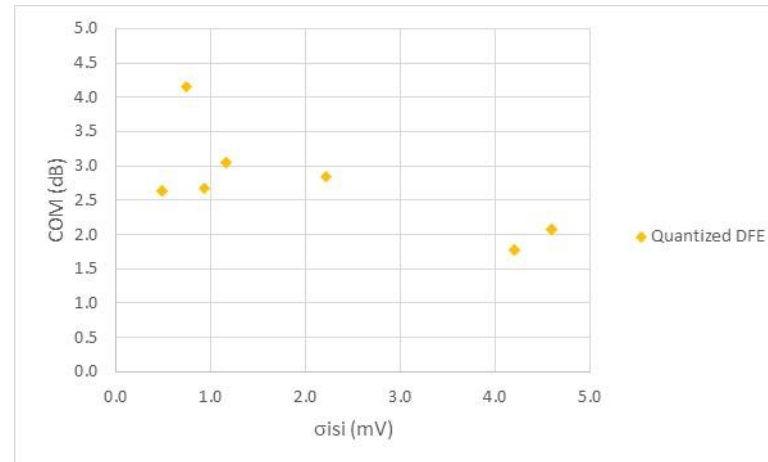
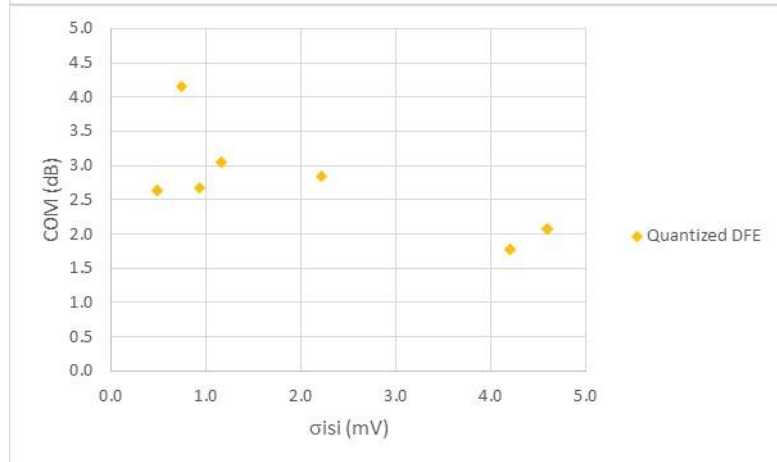
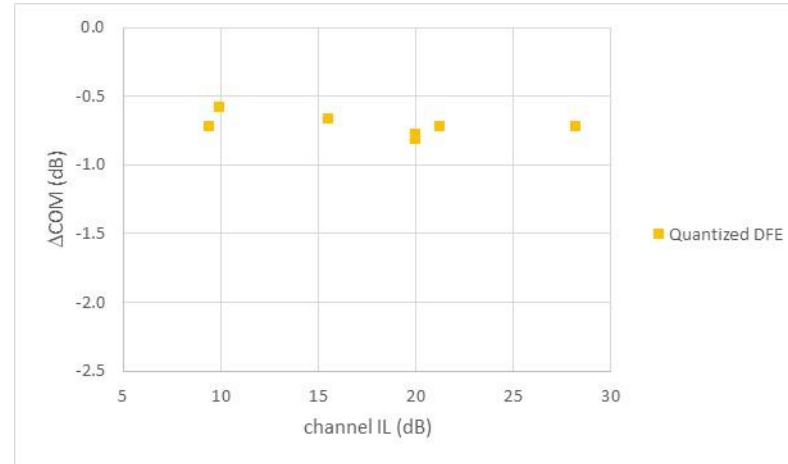
Consolidated Data #2



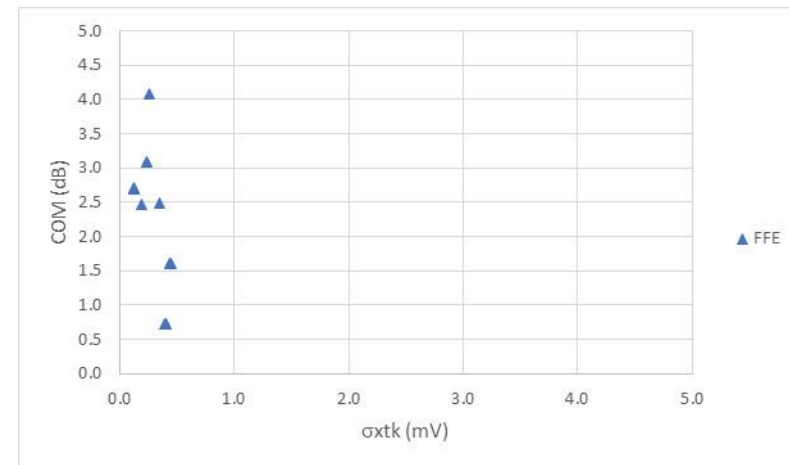
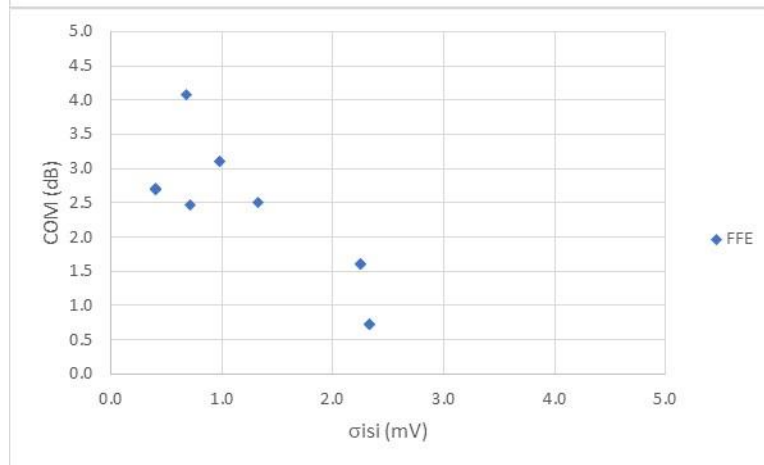
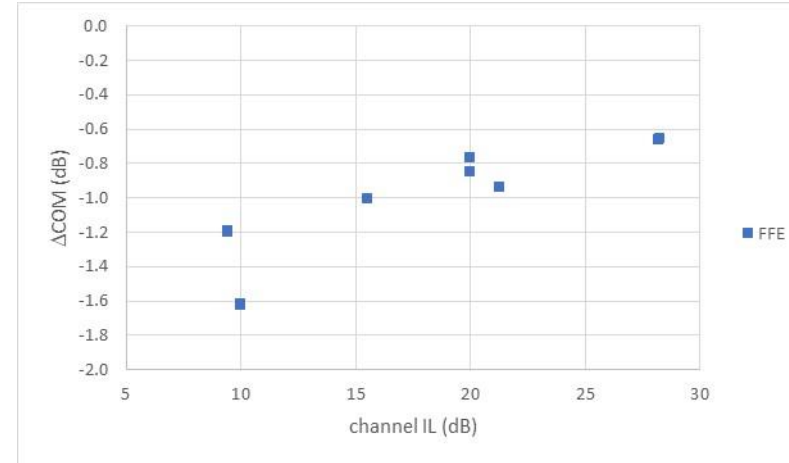
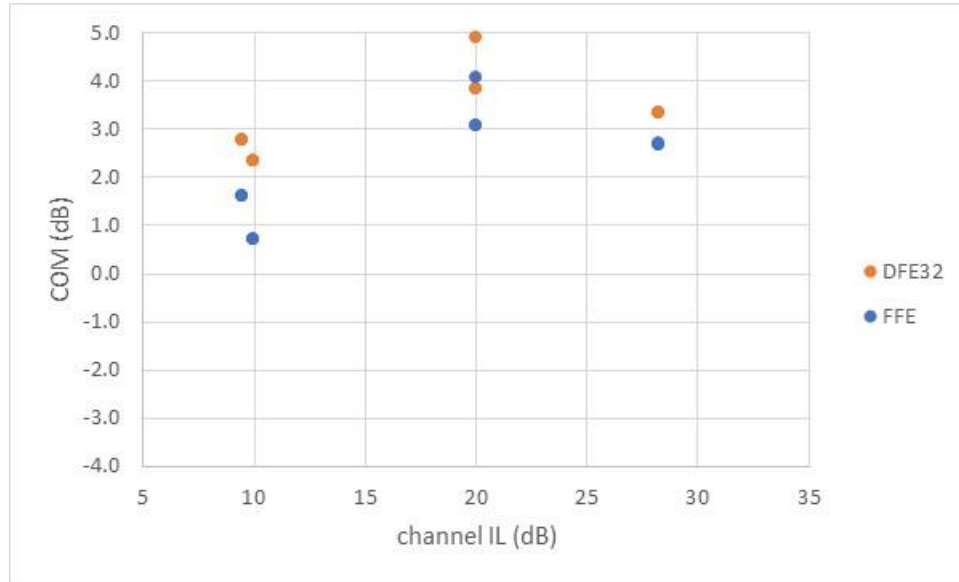
Quantized DFE



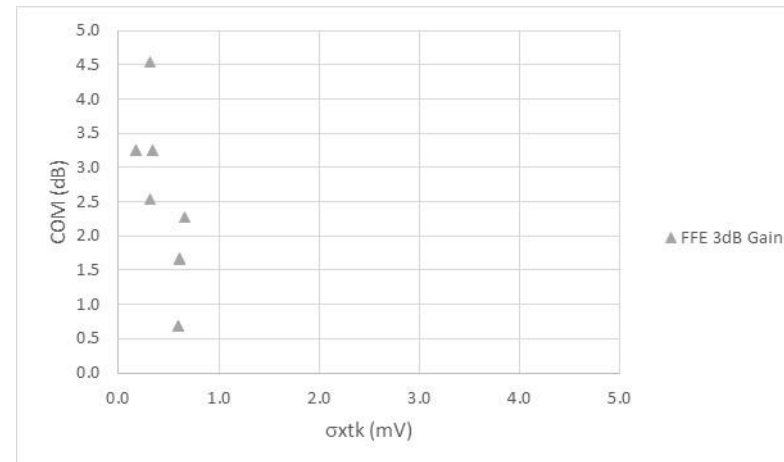
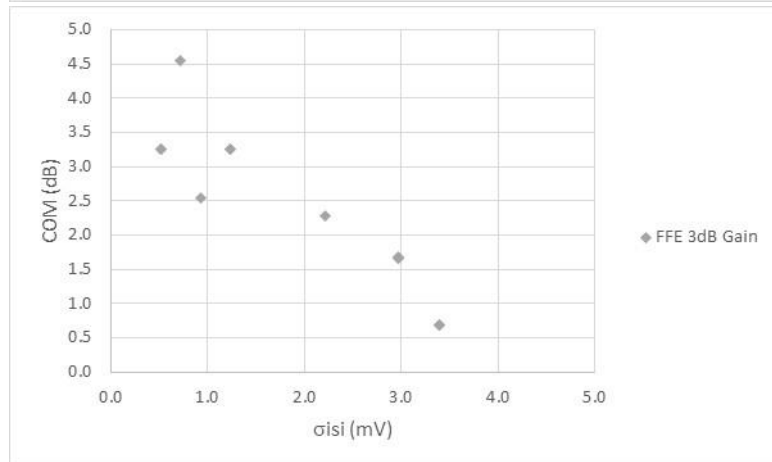
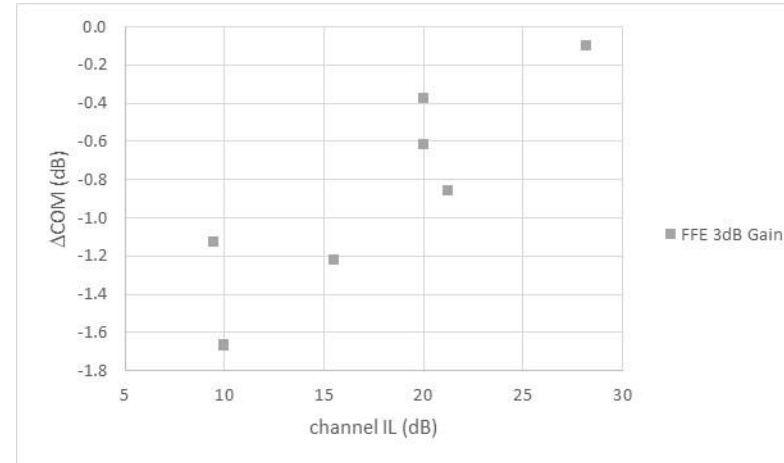
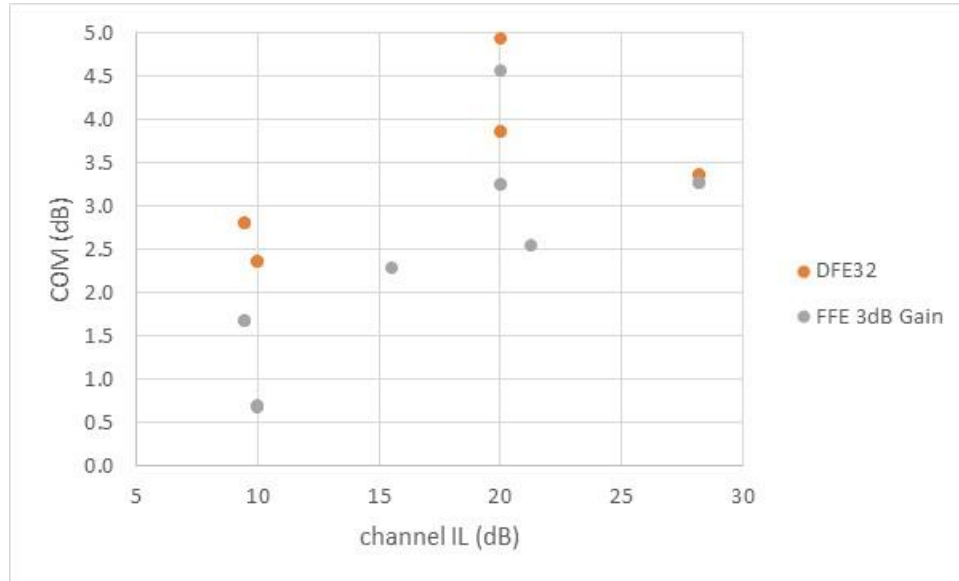
Delta calculated relative to ZF-DFE.



DFE + FFE



DFE + FFE w/ 3dB Cursor Gain



Correlation to COM with DFE

