Backplane Discussion Direction Check

Beth Kochuparambil, Cisco

Supporters:

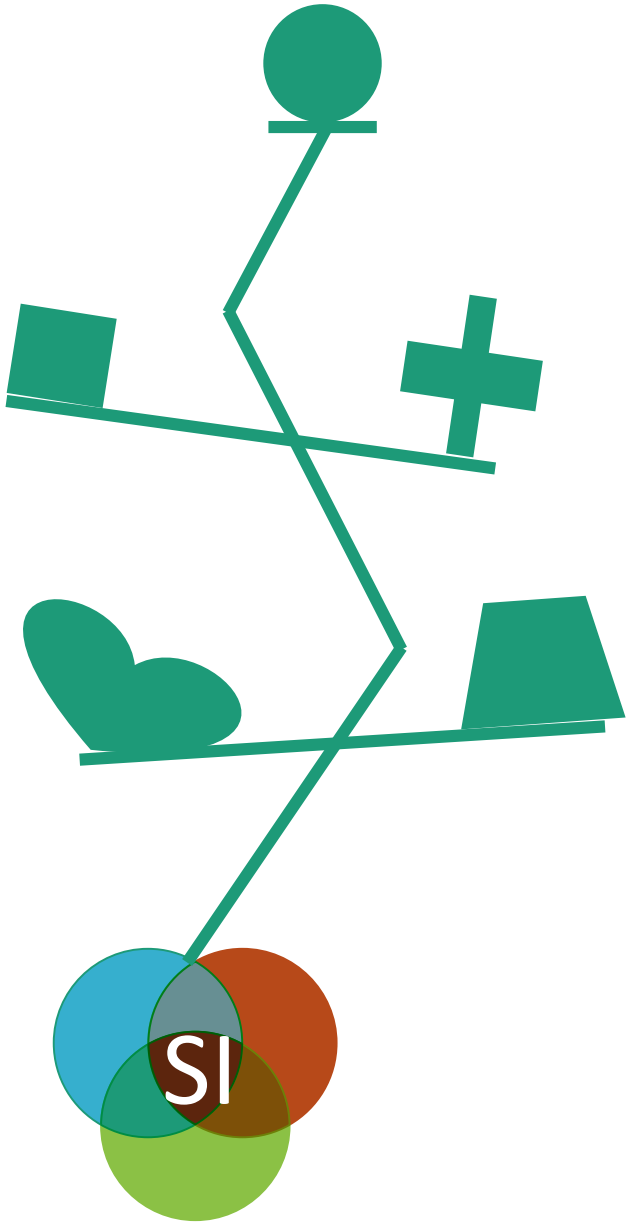
- Howard Heck, Intel
- Dave Chengson, Juniper
- Arturo Pachon, TE
- Brandon Gore, Samtec
- Kent Lusted, Intel

Backplane Analysis – 3 Step Approach

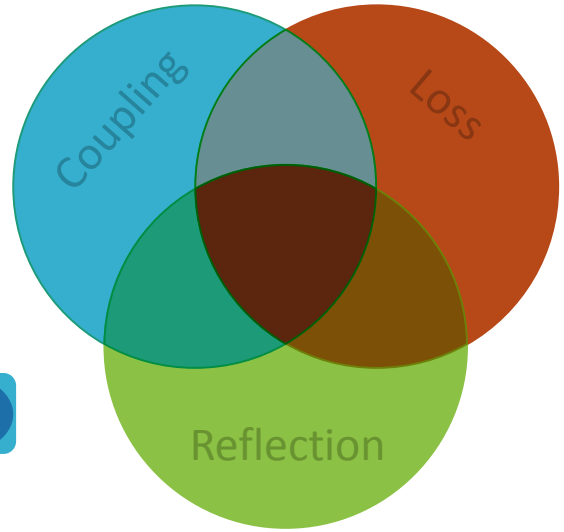
1. Ideal channels → High level sanity
   “Are we in the ballpark?”
   “Is the TX/RX architecture appropriate at this data rate?”
2. Reasonable channels → Coming into reality
   “Does the architecture still hold?”
   “What are reasonable settings?”
   “Start holding some ‘tools’ still”
3. Many, many, many channels
   → Fine tune and validation

System Implementation

- Loss only PART of the puzzle
  - BGA breakout
  - Connector footprint
  - Manufacturing tolerance
- Balancing act with ***multiple*** axis
  - Architecture
  - System Complexity
  - Signal Integrity
  - Design Cost
  - Etc
- **MANY** causes of Signal Integrity effects



Everything has a Range!
Therein Lies the SI Balancing Act.



BGA pitch – 2.0 - 0.7mm

Backdrill/stub length – 2-12mil

Board thickness/Via Length – LC: 110-180mil, BP: 200-250

Cu Roughness – Foil + Treatment – Rz = 0.9-5.0um

Manufacturing tolerance – 5-10%

PCB Technology of today vs tomorrow

Trace Width – 3.5-6.5mil

P/N Skew (often length-based) – 4-12ps

Capacitors → On-die only

Identifying Worst Case

- Various application spaces rely on different constraints
  - Likely not to have the worst of all metrics at once
  - Margins are tight
  - Various causes of signal integrity effects
  - Concept of “Golden Channel” is unrealistic
- Working to select 3-5 channels that MUST work
  - Similar to “Golden Channel” concept
  - Test multiple boundaries
  - Can include more, but if you’re only doing a few…

Call to Action

1. Ideal channels → High level sanity
   - *"Are we in the ballpark?"*
   - *"Is the TX/RX architecture appropriate at this data rate?"*
2. Reasonable channels → Coming into reality
   - *"Does the architecture still hold?"*
   - *"What are reasonable settings?"*
   - *"Start holding some 'tools' still"*
3. Many, many, many channels
   → Fine tune and validation

Past & Present

January - March

After Baselines

Questions?

Backup

7 channels previously submitted

Channels by Upen this meeting

Channels by Howard this meeting

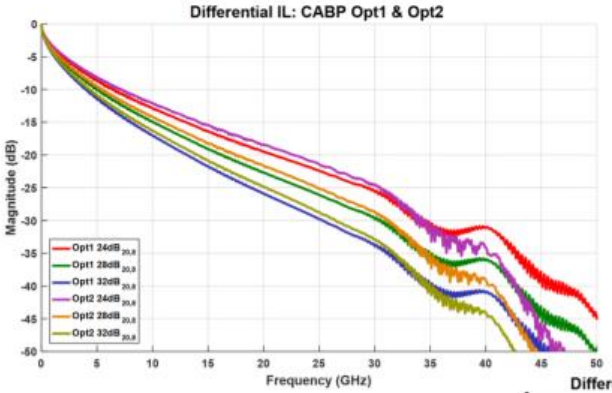
http://www.ieee802.org/3/ck/public/adhoc/aug15_18/mellitz_3ck_adhoc_02_081518.pdf

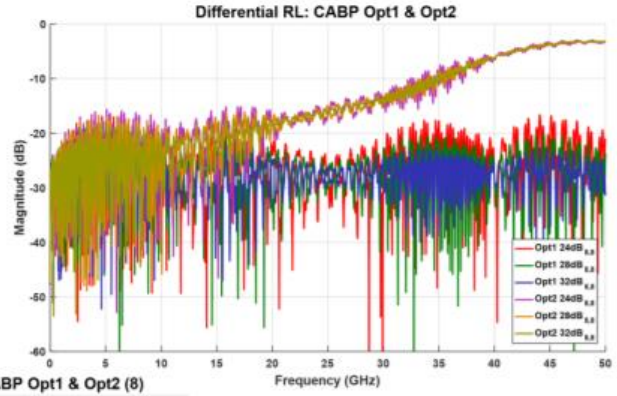
Cabled Backplane Channel

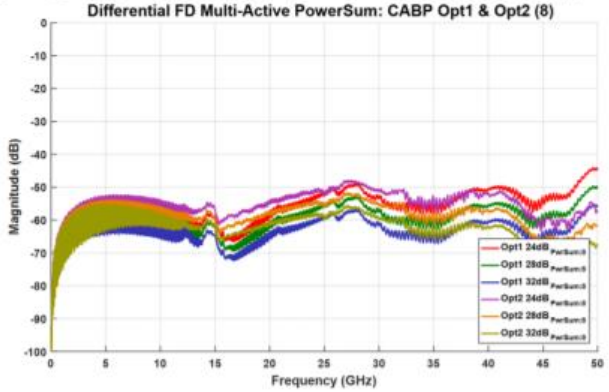
6 channels
2 PCB Via Options
- Opt1, Opt2

3 Loss targets
- 24dB / 28dB / 32dB IL @28GHz

Insertion Loss, Return Loss & Powersum Crosstalk

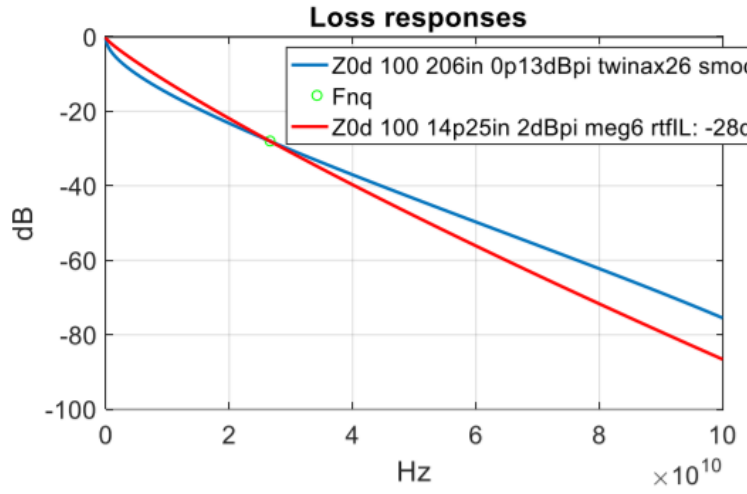


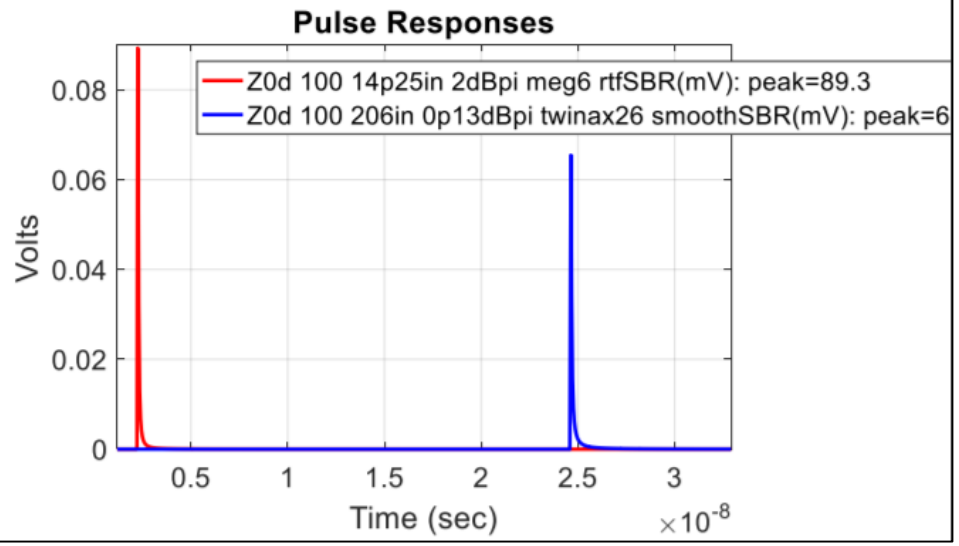




http://www.ieee802.org/3/ck/public/adhoc/july25_18/mellitz_3ck_adhoc_02_072518.pdf

Two Ideal Transmission Lines IL and PR

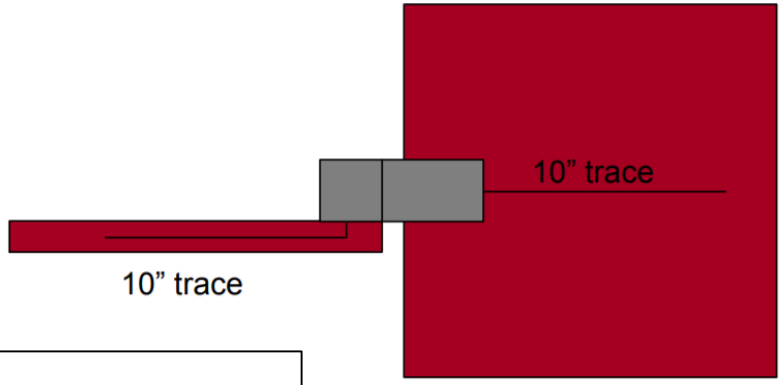




Two Ideal 28 dB transmission lines

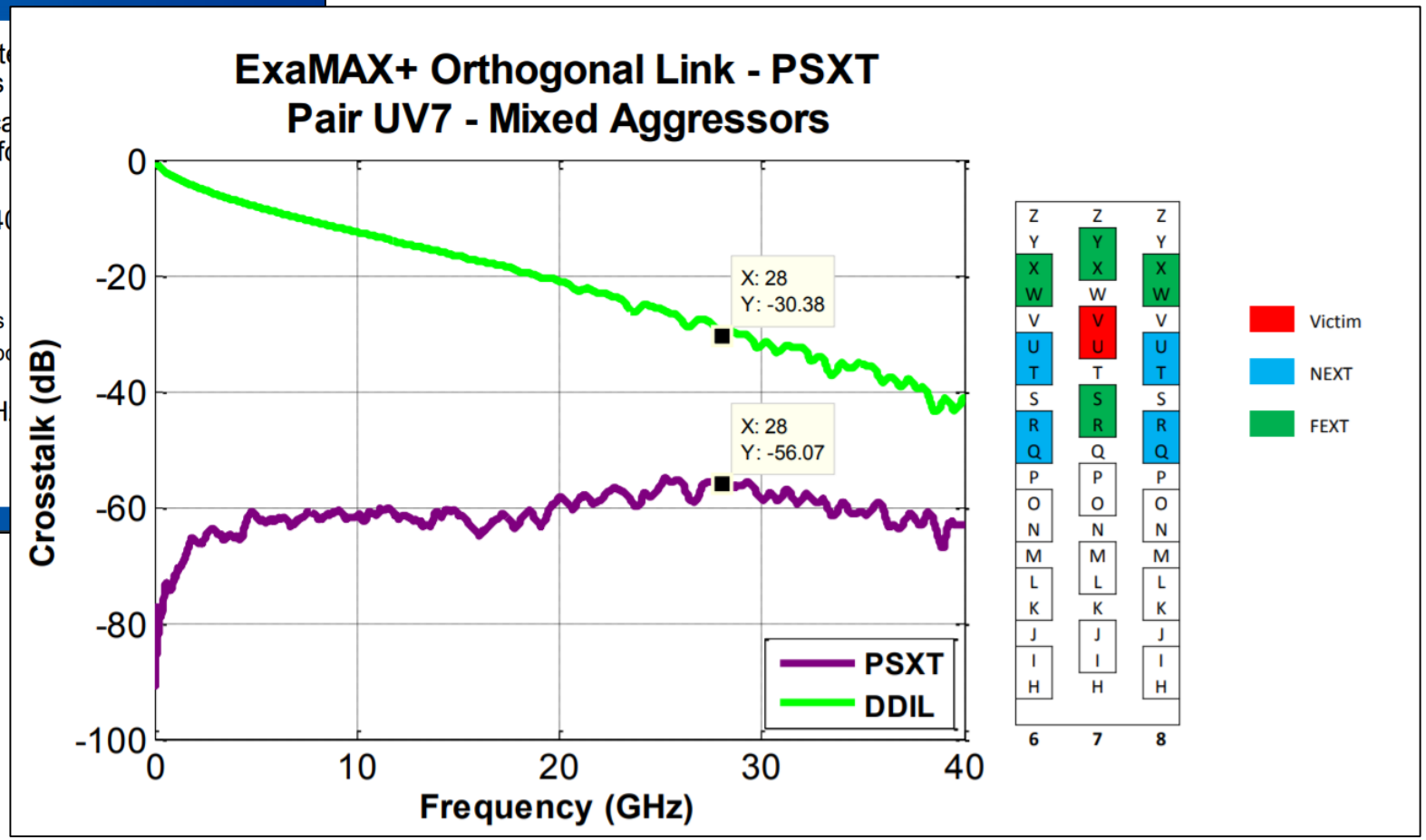
- ❑ Megtron 6 like
- ❑ 26 AWG cable like
- ❑ No reflections
- ❑ Just as good as the channel can be
- ❑ Serves to bound losses better than a number

http://www.ieee802.org/3/100GEL/public/18_03/zambell_100GEL_01a_0318.pdf



Details

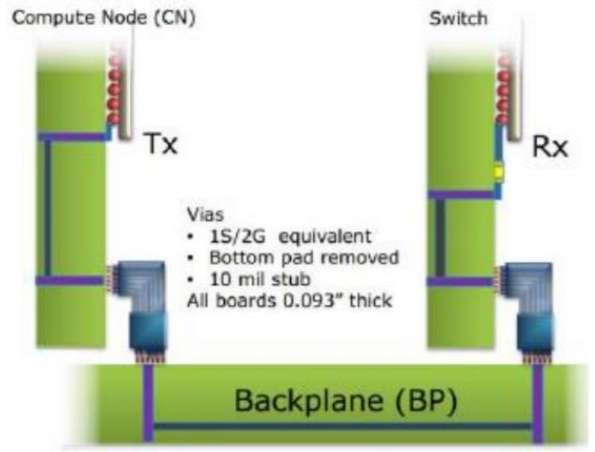
- A connector was measured on t
  de-embedded to be used in this
- A 10” simulated trace was conca
  the de-embedded connector & f
  channel length of 20”.
- Board material is Doosan DS74
  - Dk = 3.25 & Dk = 0.0015
  - Board thickness = 77 mils
  - Trace width \ spacing = 9.6 \ 6.5 mils
  - This is the material used in the test b
    traces.
- Touchstone files go from 10 MH
  steps



http://www.ieee802.org/3/100GEL/public/18_01/heck_100GEL_01_0118.pdf

Physical Description

- Trace Route
  - CN: 2” mid-loss
  - Switch 3” mid-loss
  - BP: 3.25” low loss
- 85ohm nominal impedance
- 3 FEXT, 4 NEXT
- Routes include breakout, vias
- More work to be done to optimize
  - Crosstalk
  - Vias

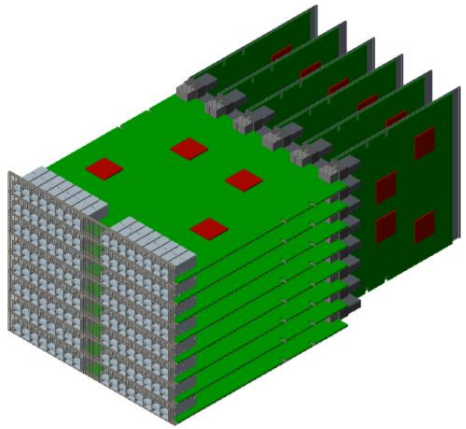


Mid-loss: ~3.6dB/in @ 26GHz
Low loss: ~1.9dB/in @ 26GHz

nse

http://www.ieee802.org/3/100GEL/public/18_01/tracy_100GEL_03_0118.pdf

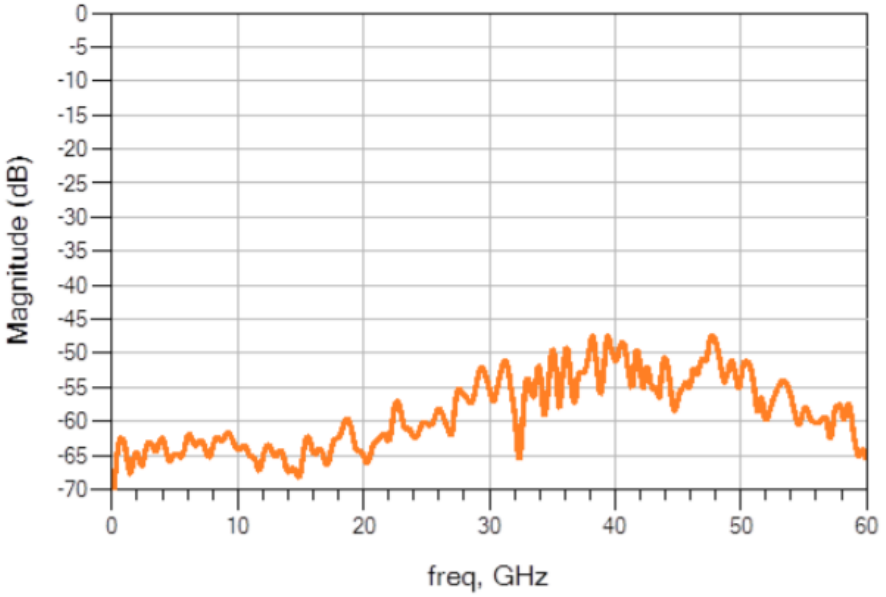
Orthogonal Backplane Channel



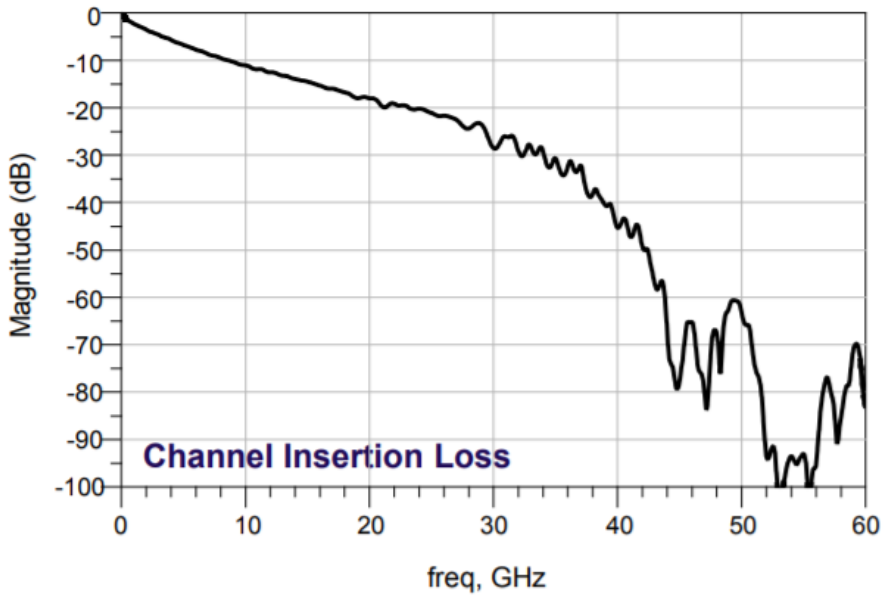
- 18” PCB Trace Total
  - 9” Trace per board
  - 6/6/6 trace geometry
  - Meg7N Laminates
  - HVLP Foils
- 140mil (3.56mm) Thick PCBs
  - Victim pair uses layer 2 routing
  - Victim pair: 15mil Stub w/ Shallow EON Technology
  - Aggressor Pairs are thru board to bottom layer
- Next-Gen STRADA Whisper Connector Model
  - Direct-Plug Orthogonal
  - Stub resonance has been addressed
  - Additional noise control features
- S-Parameter files: tracy_100GEL_04_0118.zip

Orthogonal Backplane Channel R

TX/RX 8-Aggressor PowerSum Crosstalk

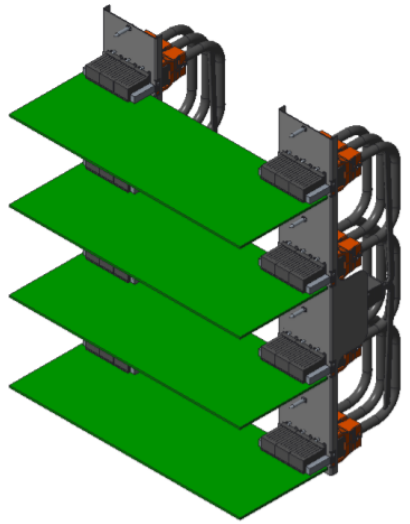


Differential Insertion Loss



http://www.ieee802.org/3/100GEL/public/18_01/tracy_100GEL_03_0118.pdf

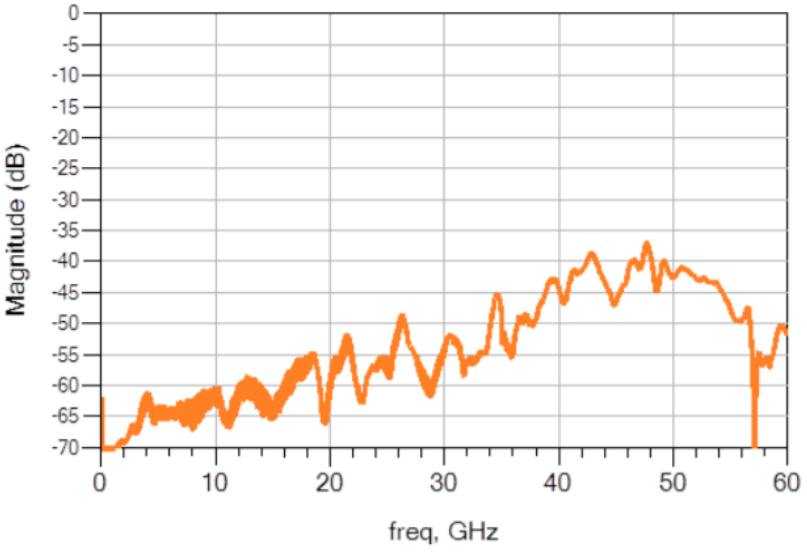
Cabled Backplane Channel



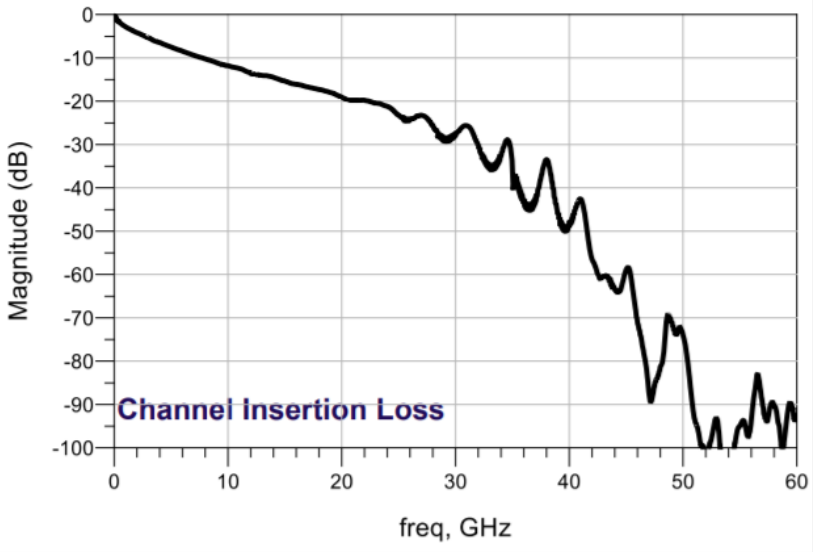
- 12” PCB Trace Total
  - 6” Trace per Board
  - 6/6/6 Geometry
  - Meg7N Laminates
  - HVLP Foils
- 140mil (3.56mm) Thick Footprints
  - Victim pair uses layer 2 routing
  - Victim pair: 15mil stub w/ shallow EON technology
  - Aggressor Pairs are thru board to bottom layer
- Next-Gen STRADA Whisper Connector Model
  - Cabled header to R/A receptacle
  - Additional noise control features
  - Stub resonance addressed
- 1m Cable Length
  - 30AWG TurboTwin twinax cable
- S-Parameter files: tracy_100GEL_05_0118.zip

Cabled Backplane Channel R

TX/RX 8-Aggressor PowerSum Crosstalk

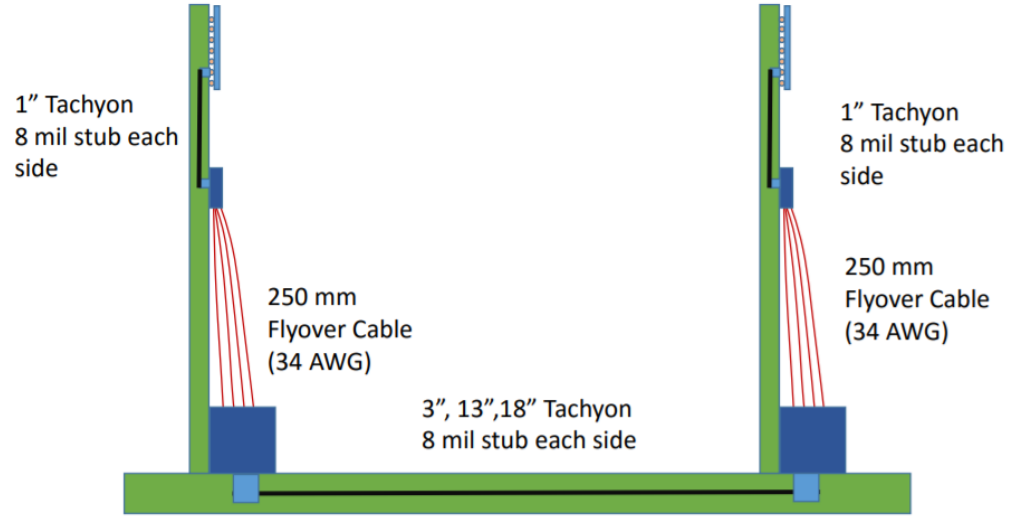


Differential Insertion Loss



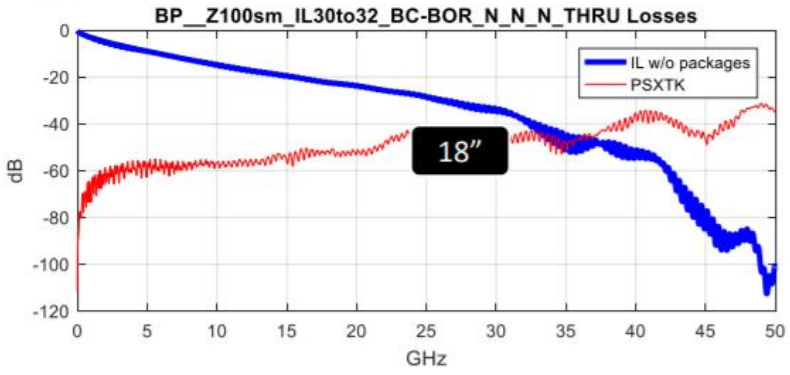
http://www.ieee802.org/3/100GEL/public/adhoc/jan03_18/mellitz_100GEL_adhoc_01_010318.pdf

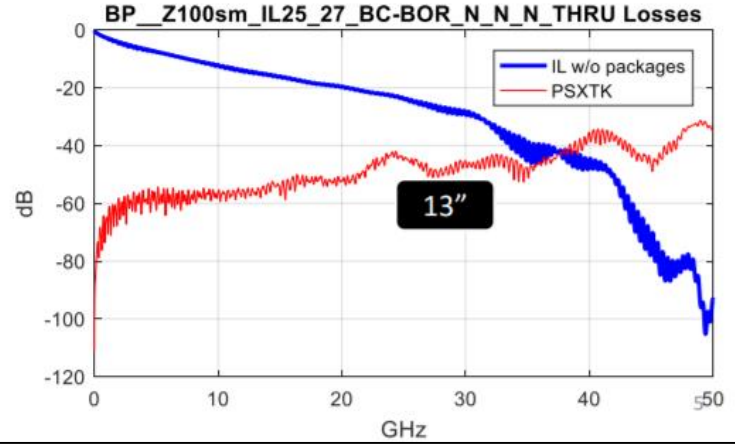
Three Flyover Tachyon Backplane Channels



IEEE 802.3 100 Gb/s per Lane Electrical Study Group

er Sum





* Routed length on backplane

IEEE 802.3 100 Gb/s per Lane Electrical Study Group