

# Further Study on RS(544, 514) FEC - Symbol Interleaving and Bit Muxing

Authors: Xiang He, Alex Nicolescu  
January, 2019

[www.huawei.com](http://www.huawei.com)

# Introduction

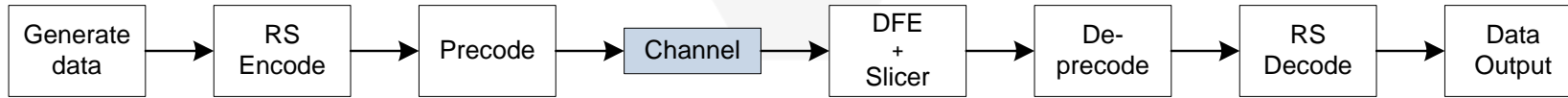
- [he\\_3ck\\_adhoc\\_01a\\_010219](#) showed some simulation results on different FEC schemes for 100G FEC sublayer.
- This presentation added one more case, where 2 FEC codewords are symbol interleaved into two lanes, and the 100G lane is formed by 2:1 bit multiplexing in the PMA.

# Background

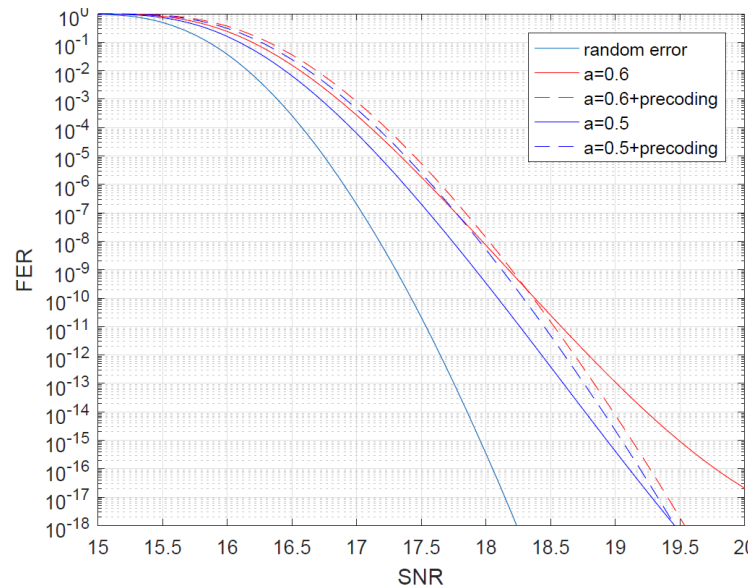
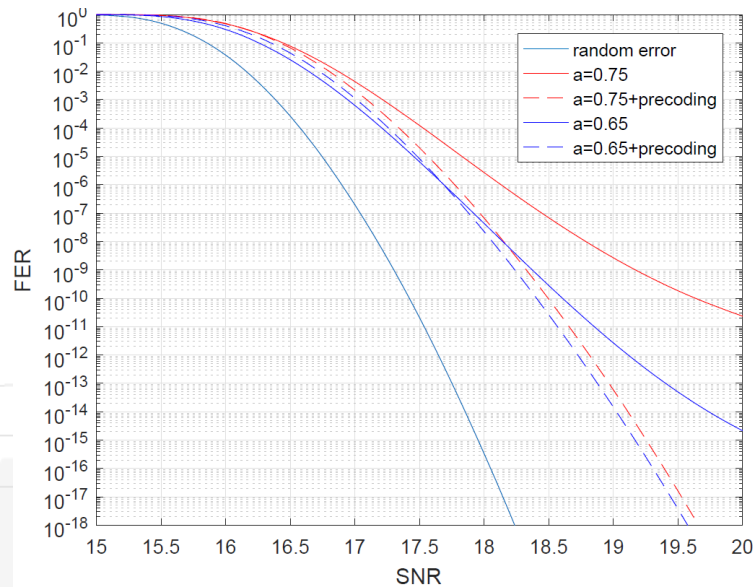
- FEC interleaving was discussed in [gustlin\\_3ck\\_01\\_1118](#).
- [anslow\\_3ck\\_01\\_1118](#) & [anslow\\_3ck\\_01\\_0918](#) compared many options including interleaving two FEC codewords to form a 100G lane, and 2:1 and 4:1 bit-muxing.
  - It was shown that symbol interleaving outperformed 2:1 or 4:1 bit muxing.
- Precoding effects for DFE based model was also studied ([zhang\\_3ck\\_01a\\_0918](#)).
- We did some more analysis based on the contributions above and some measured channel data provided in previous meetings, to show the benefit of symbol interleaving.

# Precoding Disabled

- We did some analysis based on different possibilities of burst continuing “a” values.
  - The model was based on the block diagram below.



- Precoding only helps when “a” is greater than 0.6, as shown in the calculated data below:



\* In these figures, (SNR – 6.99) is the SNR as defined in [anslow 3ck 01 1118](#).

- Our simulation in the following slides was performed on ADC-based model with low tap values, so we disabled precoding.

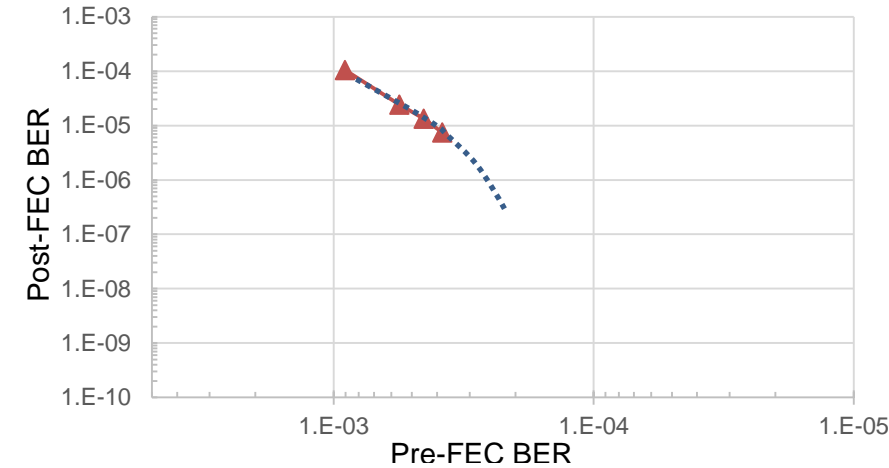
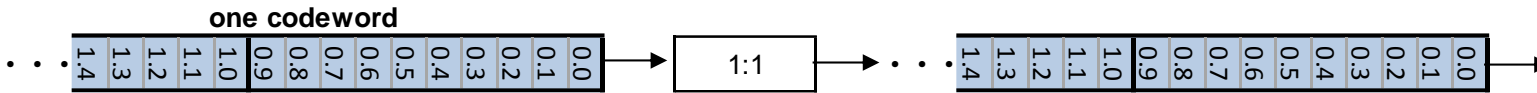
# Simulation Setup

- The simulations were done based on one channel data provided in [mellitz\\_3ck\\_adhoc\\_02\\_081518](#).
  - The first set of data shown in this contribution was based on “CaBP\_BGAVia\_Opt2\_28dB”.
  - More channels will be simulated, including [mellitz\\_3ck\\_adhoc\\_02\\_081518](#) & [kareti\\_3ck\\_01a\\_1118](#)
  - This work is done with ADC-based SerDes model\*.
- **TX side:**
  - Matlab environment generates the RS(544,514) FEC codewords;
  - Perform the distribution and interleaving/bit-muxing;
  - Modulates the signal stream and sends them over channels that suffer of insertion loss and cross talk.
- **RX side:**
  - Equalization is provided by the CTLE whose output is connected to the ADC, followed by the FFE/DFE equalization.
  - The received demodulated codewords are error corrected and statistics extracted.
- 1000 codewords per encoder is simulated for each data point.

\* No precoding. DFE: Tap 1 = 0.3, Tap 2 = 0.05

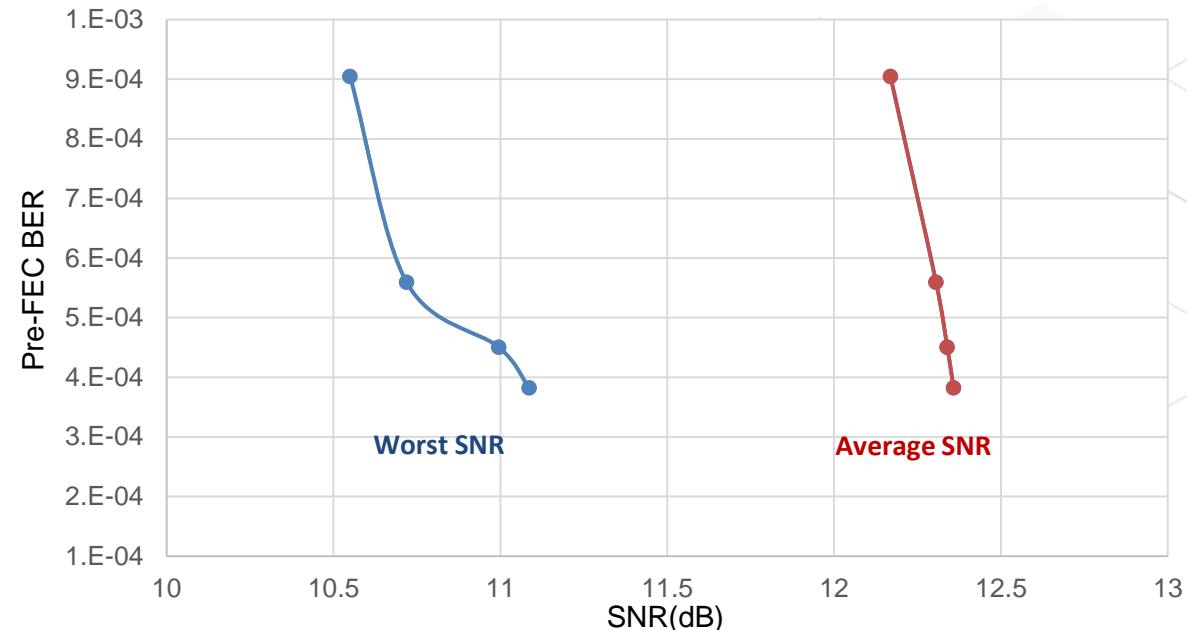
# Case 1 – 1 codeword, 1 lane, direct symbol output.

- This case is provided as a reference.
  - It shows the performance of a native RS(544,514) FEC without any symbol interleaving or bit-muxing.



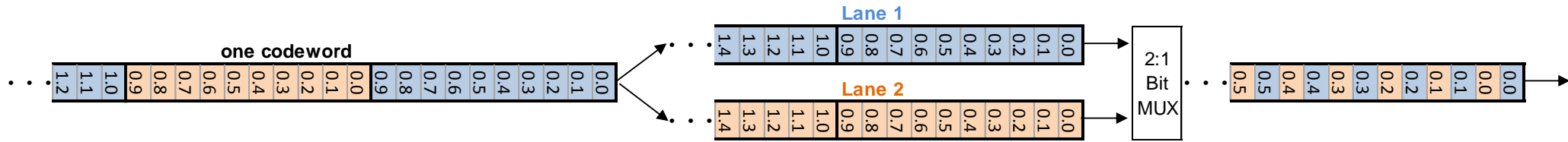
- The data was taken on different ICN values.
  - Pre-FEC and post-FEC BER values were extracted.
  - The average and worse SNR at FEC decoder for each run were recorded.
  - Two different flavors of plots were tried
    - post-FEC BER vs Pre-FEC BER
    - Pre-FEC BER vs SNR(worst) & SNR (average)

ICN(mV)	preFEC BER	SNR (dB) (Worst)	SNR (dB) (Average)	postFEC BER
1.6	9.04E-04	10.549892	12.169264	1.05E-04
1.2	5.59E-04	10.719422	12.305772	2.43E-05
1.0	4.50E-04	10.995735	12.339306	1.33E-05
0.8	3.82E-04	11.086742	12.358319	7.45E-06



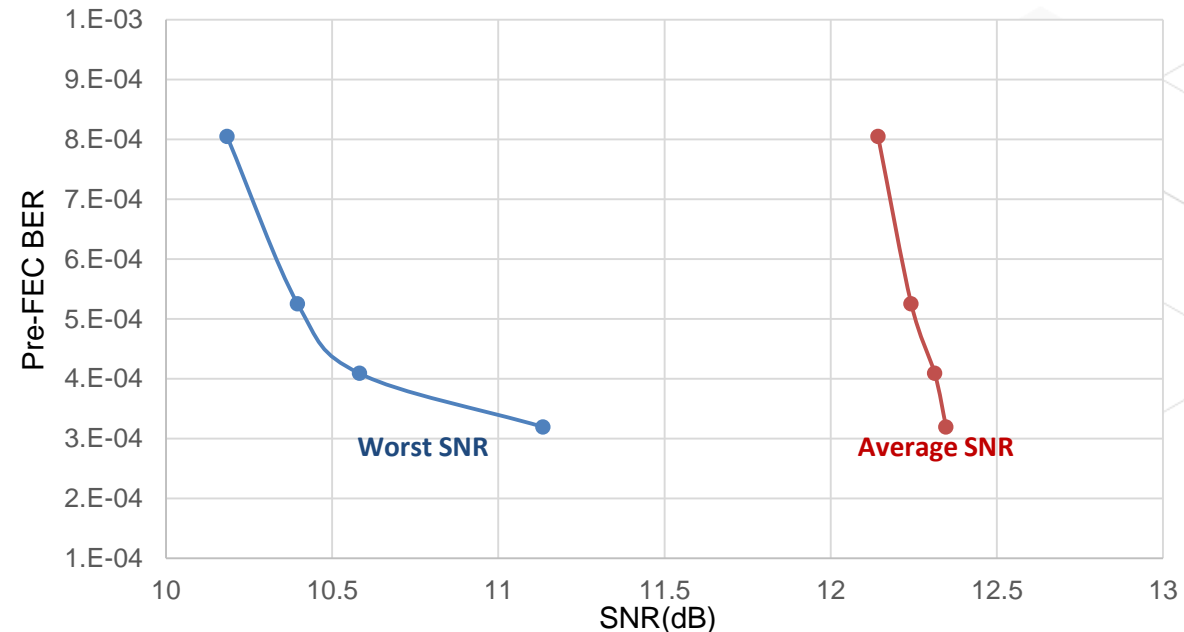
# Case 2 – 1 codeword, 2 lanes, bit mux

Round robin distribution of FEC symbols from 1 FEC codeword to two lanes. 2:1 bit multiplexing in the PMA.



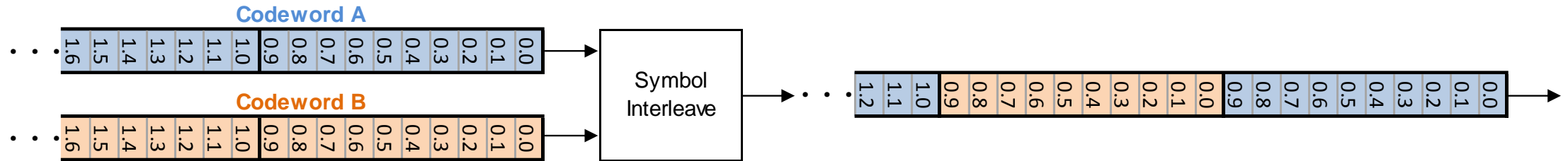
- This is equivalent to 802.3cd defined FEC
- Plotting the pre-FEC BER and SNR makes a clearer comparison.
  - Worst SNR is directly related to the number of error bits in a codeword.
  - Average SNR does not reflect the real situation where many error bits are located in one codeword (burst cases).

ICN(mV)	preFEC BER	SNR (dB) (Worst)	SNR (dB) (Average)	postFEC BER
1.6	8.05E-04	10.184004	12.142603	8.31E-05
1.2	5.26E-04	10.396164	12.242248	3.15E-05
1	4.09E-04	10.58238	12.312874	1.40E-05
0.8	3.20E-04	11.134963	12.347067	4.41E-06



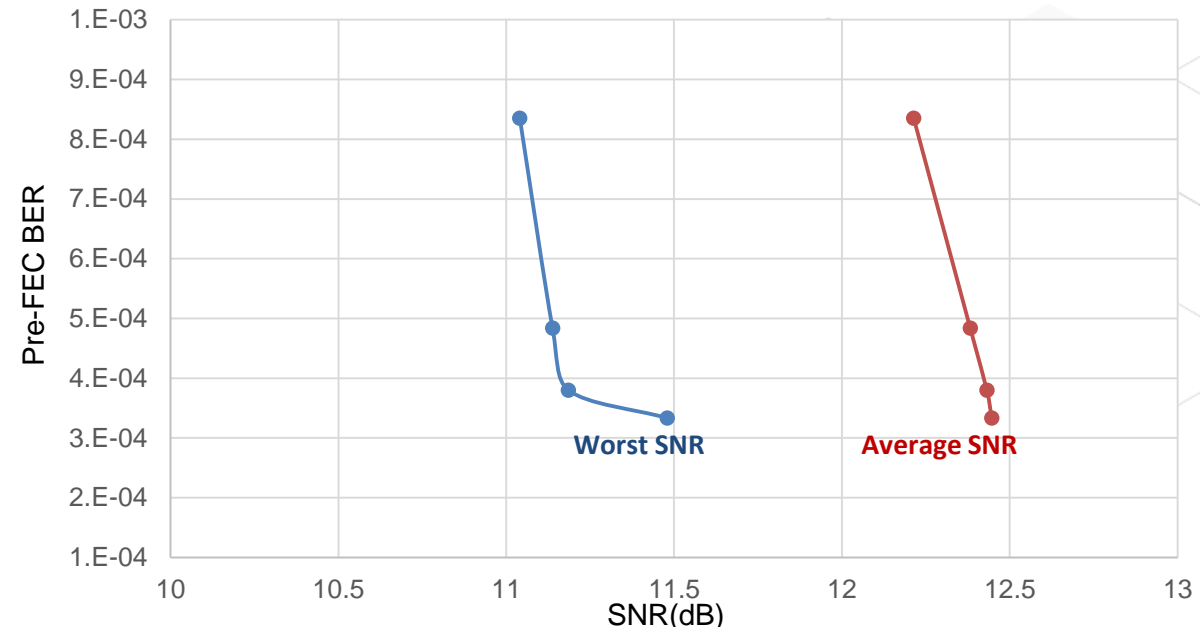
# Case 3 – 2 codewords, 1 lane, symbol mux

2:1 Symbol interleave from 2 FEC codewords to a single 100G lane.



- Symbol interleaving improves FEC performance.
  - No post-FEC errors were detected for ICN  $\leq 1.2\text{mV}$ .
  - The result is almost  $0.8\text{mV}$  better than the reference case in terms of ICN value.

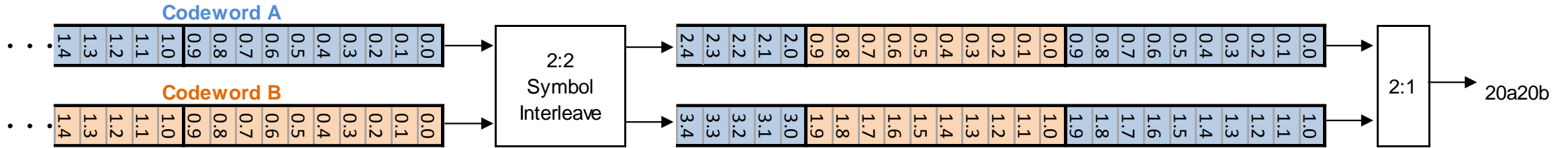
ICN(mV)	preFEC BER	SNR (dB) (Worst)	SNR (dB) (Average)	postFEC BER
1.6	8.35E-04	11.040394	12.213918	4.60E-06
1.2	4.84E-04	11.137942	12.382493	0
1	3.80E-04	11.185276	12.431798	0
0.8	3.33E-04	11.479653	12.446318	0





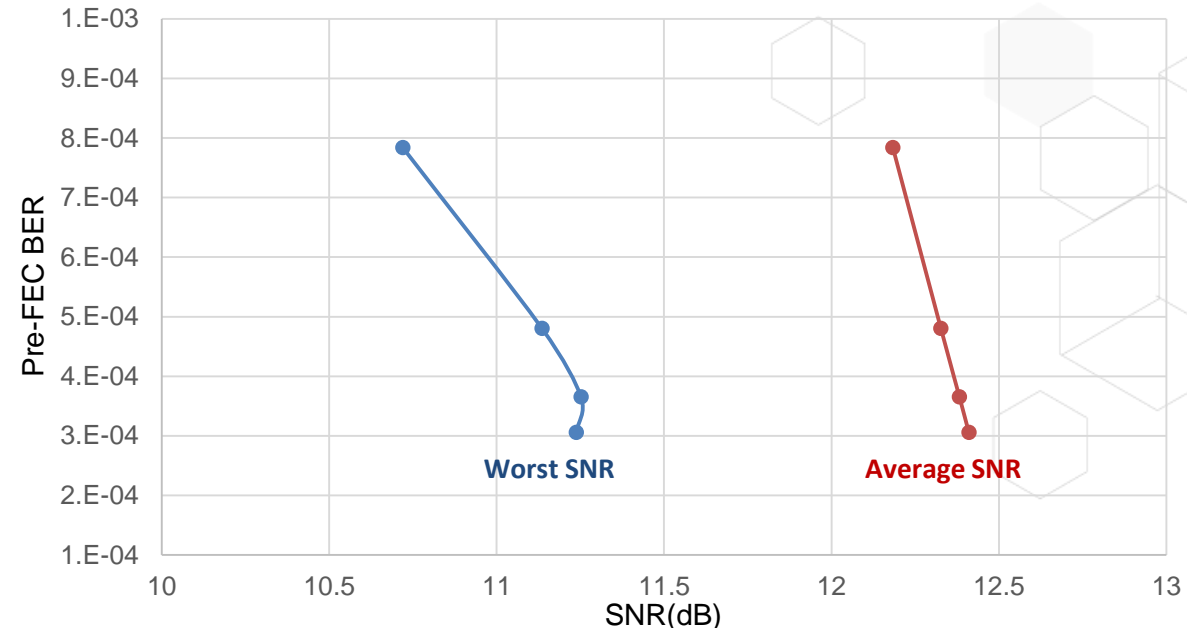
# Case 4 – 2 codewords, 2 lanes, bit mux

2 FEC codewords symbol interleaved into two lanes. 2:1 bit multiplexing in the PMA.

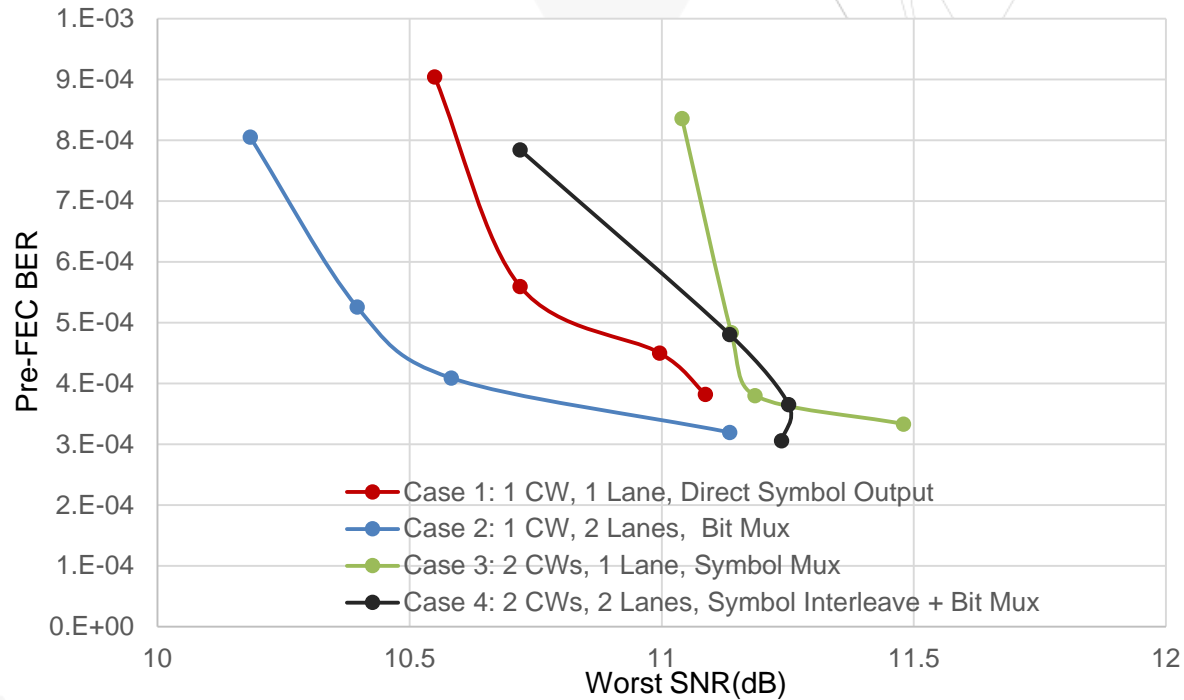


- Only “20a20b” is simulated.
  - No post-FEC errors were detected for ICN  $\leq 1.0\text{mV}$ .
  - Slightly worse than 2 codewords, 1 lane, symbol mux case.
  - “10ab10ba” could be slightly better.

ICN(mV)	preFEC BER	SNR (dB) (Worst)	SNR (dB) (Average)	postFEC BER
1.6	7.84E-04	10.719422	12.183344	3.37E-05
1.2	4.81E-04	11.134963	12.326718	3.86E-06
1	3.66E-04	11.251666	12.382125	0
0.8	3.06E-04	11.237942	12.410276	0



# Case Study Summary



- Preliminary conclusion:
  - 2 codewords performs better based on the channel simulated.
  - The performance of 802.3cd type of bit-muxing is not as good as native RS(544,514) FEC.
- Table below shows some example codewords with error bits that may be corrected by one case but failed in another.

Codeword # with > 15 errored bits	Number of error bits	Adjacent errored bit positions	Number of error symbols	Correctable by 1 CW, 2 Lanes, Bit Mux	Correctable by 1 CW, 1 Lane, Direct Symbol Output
369	22	3	15	NO	YES
817	19	2	14	NO	YES
1160	22	2	14	NO	YES
1499	31	2	14	NO	YES
1549	46	4	24	NO	NO

# Conclusions and Questions

- This contribution compares different RS(544,514) FEC options against a reference RS(544,514) FEC with direct symbol output.
  - Performance ranking high to low:
    - 2 codewords, 1 lane, symbol mux
    - 2 codewords, 2 lanes, bit mux
    - 1 codeword, 1 lane, direct symbol output
    - 1 codeword, 2 lanes, bit mux
    - *1 codeword, 4 lanes, but mux (pending update)*
- PCS/FEC/PMA: How many codewords? How many lanes? PMA mux at bit level or symbol level?
  - 2 codewords – 2x50G FEC encoders
    - Better performance than 1 codeword.
  - 1 codeword – 1x100G FEC encoder
    - Backward compatible.

**THANK YOU**