Suggested change in Module Input and Host Input tests stressed eye calibration

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KEYSIGHT TECHNOLOGIES

Background

- Similar test setup for C2M stressed input has been used for years
  - Only significant changes have been in reference receiver topology

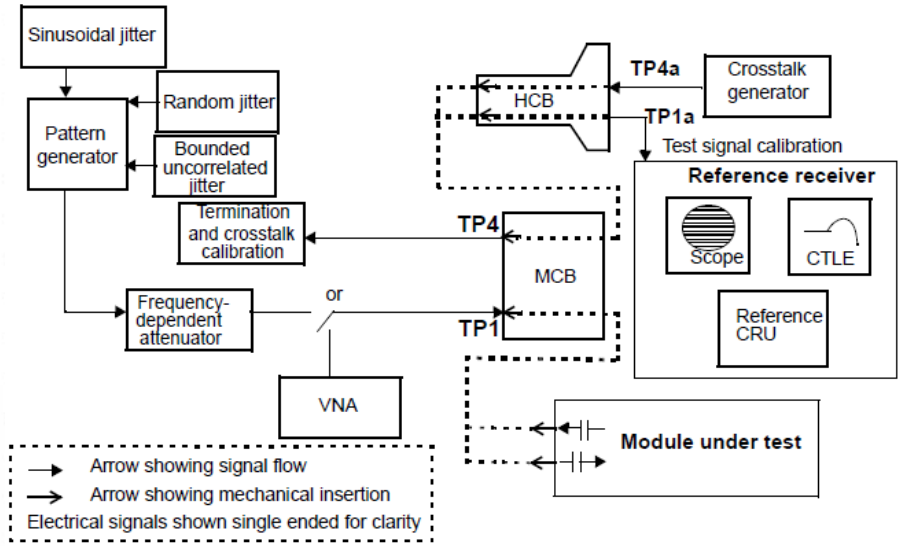

Figure 120E–12—Example module stressed input test

From Annex 120E

- Assumptions used to set stress calibration targets (EW and EH) no longer work with the edge speeds we are targeting

Setup assumption through Annex 120E

- Test channel (MCB/HCB TP1-TP1A + Frequency Dependent Attenuator + cabling) = maximum targeted channel + (package loss in Tx).
- This assumes the pattern generator is able to emulate the transition time of the Tx at the bump.

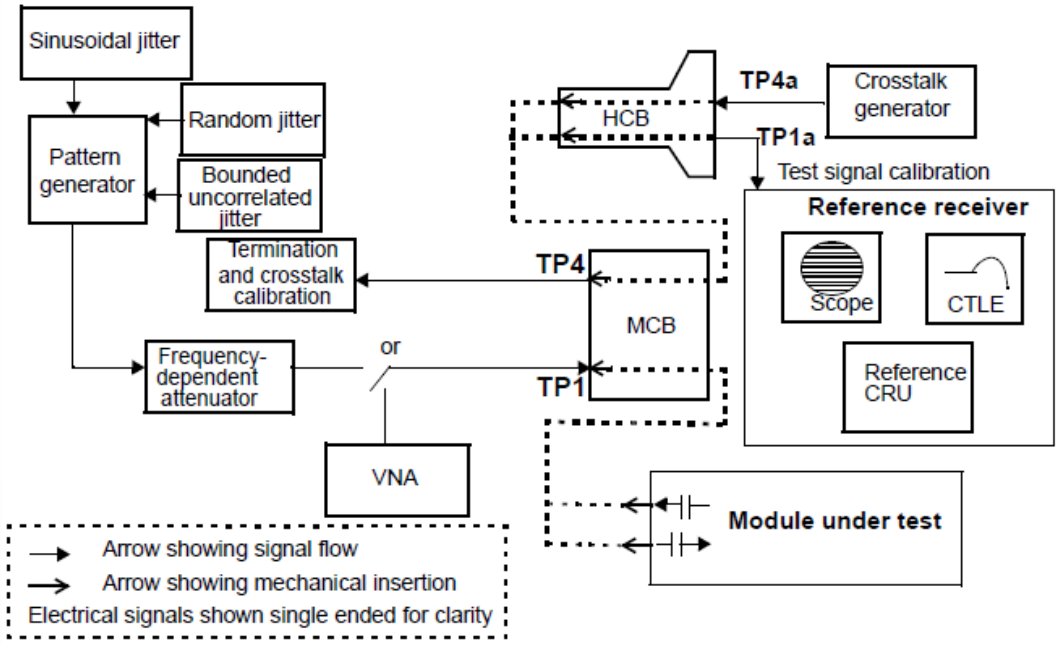

Figure 120E–12—Example module stressed input test

From Annex 120E

Challenge at > 100 Gb/s

- Transition times in recent link simulation models (Li_3ck_00_1118 and others) use 6 ps.
- This is considerably faster than current and likely future pattern generators can deliver
  - While a faster process is used (InP), the PT instrument output stage has more transistors, still has a package, and output cables to drive.
  - Currently available pattern generator output transition times are in the 8.0 – 9.0 ps range
- Experience has shown that eye calibration is extremely difficult or impossible when the PG output speed is only slightly slower than assumed speed at bump.

Recommendation for 802.3ck

- Rather than calculating the eye closure calibration targets assuming the PG is emulating the Tx die at the bump, then adding extra channel loss to emulate the Tx package…
- Calibrate assuming the transition time is as measured at the package ball, and do not include additional channel loss to emulate the Tx package
- Essentially: The test setup is now configured and calibrated using the Tx signal at the package ball

Questions?