100G C2M Study Results

Phil Sun, Credo Semiconductor

IEEE 802.3ck Task Force

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Adam Healey, Broadcom
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Introduction

- Up to 16dB channel insertion loss is proposed for C2M interface. Whole link insertion loss can be more than 20dB.

- This contribution studies feasibility of supporting these channels. Whole link Simulations to investigate required receiver capability in a module. TP1a Simulations to study TP1a reference model and electrical characteristics.

- Because of implementation and power considerations, 4 short equalizers covering 5 UI span are studied.

Receiver	Configuration
A	4-tap DFE (b1max=0.5)
B	5-tap FFE with 4 postcursor taps + 1-tap DFE
C	5-tap FFE with 4 postcursor taps
D	4-tap DFE with low b1max (b1max=0.1)

- Simulations are performed with COM tool 2.58.

802.3ck C2M Channels

Channel ID	Channel Description	Insertion Loss at 26.5625GHz (dB)	ERL* (dB)	ICN (mV)
1	mellitz_3ck_01_0518_C2M\9dB	8.95	10.97	2.28
2	mellitz_3ck_01_0518_C2M\10dB	9.96	6.48	4.53
3	mellitz_3ck_01_0518_C2M\11dB	11.16	11.03	1.93
4	mellitz_3ck_01_0518_C2M\12dB	12.18	6.93	3.99
5	mellitz_3ck_01_0518_C2M\13dB	13.12	11.13	1.68
6	mellitz_3ck_01_0518_C2M\14dB	13.87	7.34	3.19
7	tracy_100GEL_02_0118\long_barrel_via\TX5	16.48	8.03	0.91
8	tracy_100GEL_02_0118\long_barrel_via\TX6	16.08	9.66	0.90
9	tracy_100GEL_06_0118\Microvia\RX6	14.59	8.42	0.83
10	tracy_100GEL_06_0118\Microvia\RX5	14.57	9.69	0.93
11	lim_3ck_01_0918_QDD_legacy_pairs\12dB	12.75	11.08	2.70
12	lim_3ck_01_0918_QDD_legacy_pairs\14dB	14.02	11.49	2.50
13	lim_3ck_01_0918_QDD_legacy_pairs\16dB	15.83	11.94	2.14
14	llim_3ck_01_0918_QDD_new_pairs\12dB	12.19	11.02	3.37
15	llim_3ck_01_0918_QDD_new_pairs\14dB	13.99	11.59	2.76
16	llim_3ck_01_0918_QDD_new_pairs\16dB	15.96	11.70	2.65
17	ito_3ck_01\QSFP \bottom normal\	15.10	9.43	1.20
18	ito_3ck_01\QSFP \bottom worst\	15.58	8.25	1.14
19	ito_3ck_01\QSFP \top normal\	14.53	9.50	1.25
20	ito_3ck_01\QSFP \top worst\	14.49	8.20	1.21

- Parameters highlighted in red exceed 16dB IL, 8.5dB ERL, or 2.5mV ICN. Improvement is recommended.
- ERL is reported with the settings for reference receiver A.

COM Baseline Configuration for Whole Link Simulation

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5; 100 100 ; 100 100]	Ohm
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[1]		[test cases to run]		Port Order	[1 3 2 4]			Table 92–12 parameters		
z_p (TX)	[30 20; 1.8 1.8 ; 0 0 ; 0 0]	mm	[test cases]		RUNTAG	C2M_1218			Parameter	Setting	
z_p (NEXT)	[15 15; 1.8 1.8 ; 0 0 ; 0 0]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (FEXT)	[30 20; 1.8 1.8 ; 0 0 ; 0 0]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (RX)	[15 15; 1.8 1.8 ; 0 0 ; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
C_p	[0.87e-4 0.6e-4]	nF	[TX RX]		ERL Pass threshold	10.5	dB		z_bp (TX)	7	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	0	mm
R_d	[45 45]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	0	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	7	mm
A_fe	0.41	V									
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.6		min		N	300					
c(-1)	[-0.3:0.02:0]		[min:step:max]		TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(1)	[-0.1:0.05:0]		[min:step:max]		rho_x	0.3					
N_b	4	UI			fixture delay time	0					
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:1:-3]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	12.5	GHz									
f_p1	20	GHz			Noise, jitter						
f_p2	28	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:1:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.328125	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	32.5	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
Include PCB	0	logical									
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	0										

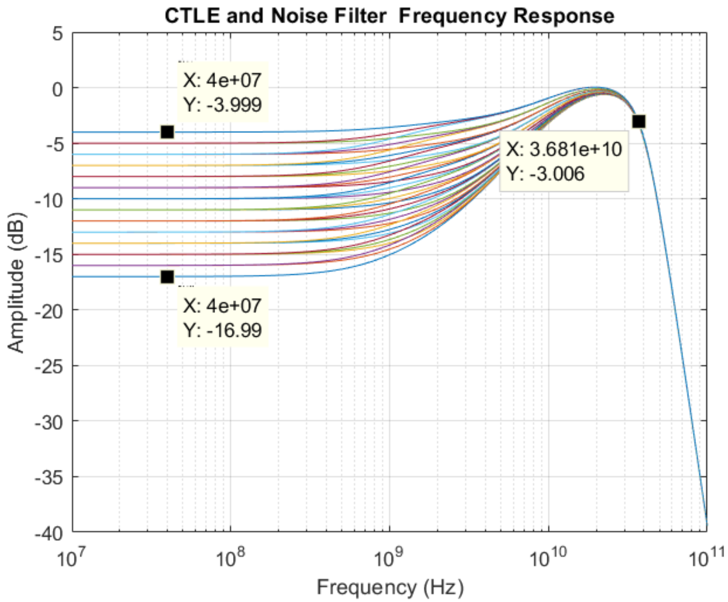
- This spread sheet is for whole link simulation with 4-tap DFE

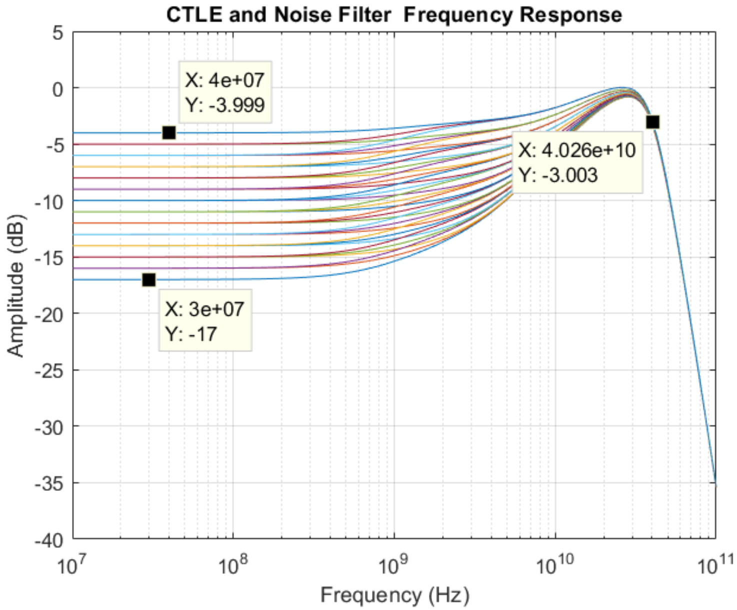
COM Baseline Configuration for TP1a Simulation

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5; 100 100 ; 100 100]	Ohm
C_d	[1.1e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[1]		[test cases to run]		Port Order	[1 3 2 4]			Table 92–12 parameters		
z_p (TX)	[30 15; 1.8 1.8 ; 0 0 ; 0 0]	mm	[test cases]		RUNTAG	C2M_1218			Parameter	Setting	
z_p (NEXT)	[0 0; 0 0 ; 0 0 ; 0 0]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (FEXT)	[30 15; 1.8 1.8 ; 0 0 ; 0 0]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (RX)	[0 0; 0 0 ; 0 0 ; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
C_p	[0.87e-4 0]	nF	[TX RX]		ERL Pass threshold	10.5	dB		z_bp (TX)	7	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	0	mm
R_d	[45 45]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	0	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	7	mm
A_fe	0.41	V									
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.6		min		N	300					
c(-1)	[-0.3:0.02:0]		[min:step:max]		TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(1)	[-0.1:0.05:0]		[min:step:max]		rho_x	0.3					
N_b	4	UI			fixture delay time	0					
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:1:-3]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	12.5	GHz									
f_p1	20	GHz			Noise, jitter						
f_p2	28	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:1:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.328125	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	32.5	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
Include PCB	0	logical									
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	0										

- This spread sheet is for TP1a simulation with 4-tap DFE

CTLE Curves



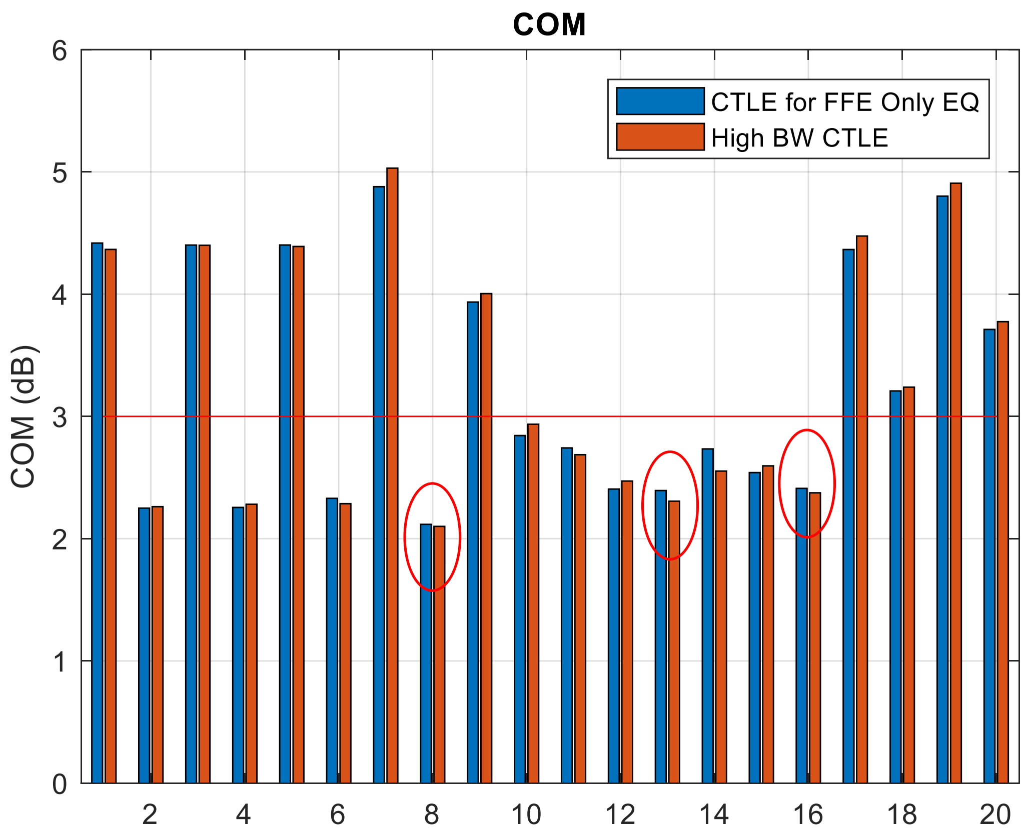


CTLE and Noise Filter for Receivers with DFE		
f_r	0.75	*fb
g_DC	[-14:1:-3]	dB
f_z	12.5	GHz
f_p1	20	GHz
f_p2	28	GHz
g_DC_HP	[-3:1:-1]	dB
f_HP_PZ	1.328125	GHz

CTLE and Noise Filter for Receivers with FFE Only		
f_r	0.75	*fb
g_DC	[-14:1:-3]	dB
f_z	18.88	GHz
f_p1	28	GHz
f_p2	53.125	GHz
g_DC_HP	[-3:1:-1]	dB
f_HP_PZ	1.328125	GHz

- With DFE, CTLE bandwidth can be relaxed.

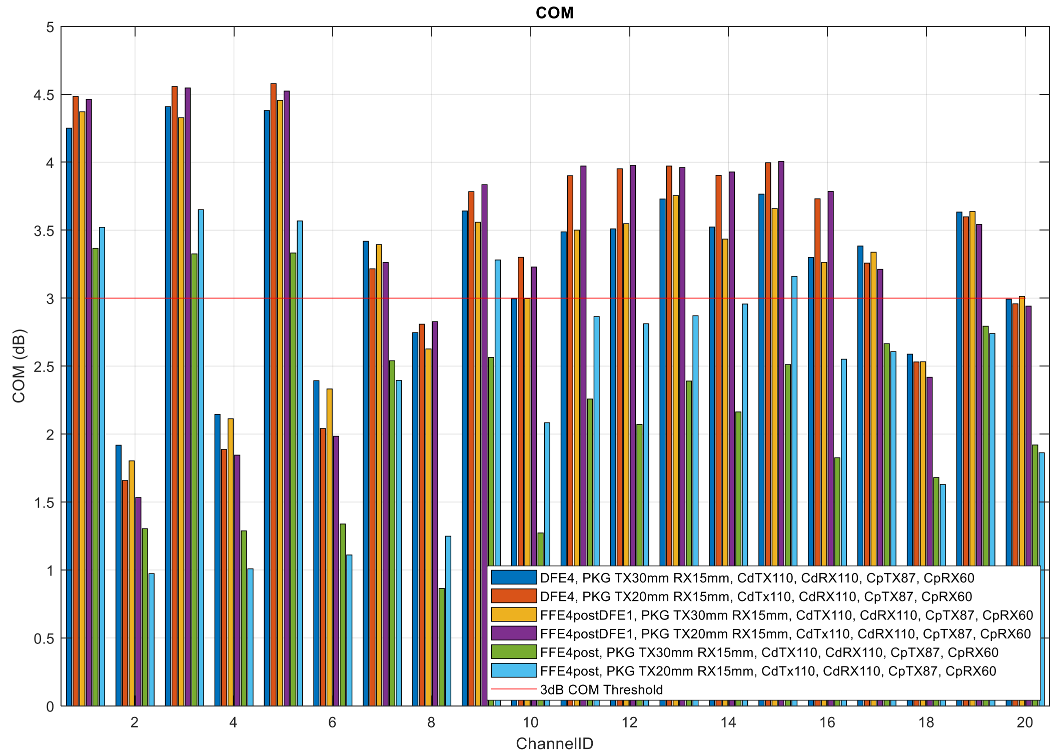
CTLE Analysis



High BW CTLE Zeros/Poles ghiasi_3ck_03a_1118		
f_r	1	*fb
f_z	18.56219427	GHz
f_p1	53.125	GHz
f_p2	28.21327684	GHz

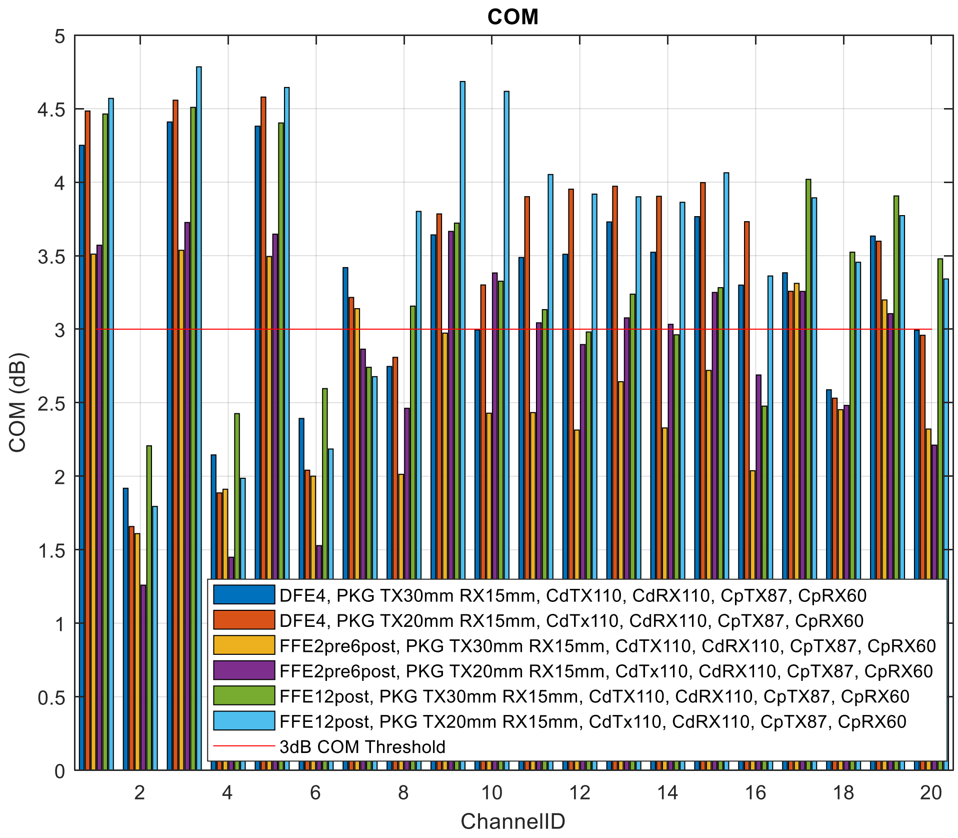
- The proposed FFE CTLE has lower bandwidth than ghiasi_3ck_03a_1118 proposal.
- Average COM difference is 0.03dB for FFEpost4 receiver at TP1A with 15mm package. The proposed FFE CTLE performs slightly better on difficult channels.

Whole Link Channel Simulation



- This is channel simulation including both TX and RX packages.
- Three short equalizers are simulated.
- **DFE4 and FFE4postDFE1 achieve similar performance; FFE4post is not sufficient for most of the end-to-end channels.**
  - DFE4 tail provides a tool for multiple-tap DFE burst error analysis.

Simulation with More Receivers

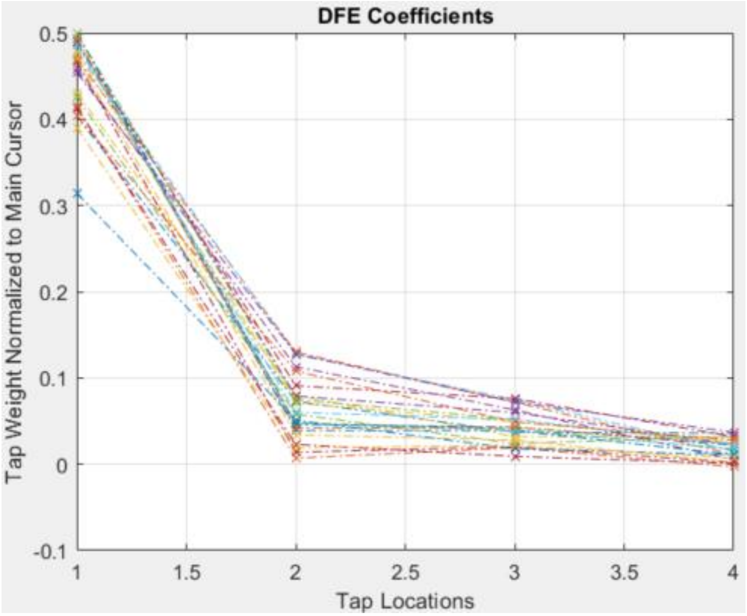


- Two longer FFE receivers are simulated for performance study. (without considering power and implementation challenge.)
- DFE4 and FFE12post can support similar amount of channels, and FFE2pre6post is not sufficient for most of the channels.
- C2M insertion loss is close to 50GE C2C interface. DFE post tap 1 is very effective in this case. Without sufficient DFE tap1, very long linear equalizer will be needed.

DFE Tap Weights and FEC Performance

Receiver A DFE Tap Constraints for Whole Link Simulation	
b1	[0, 0.5]
b2	[-0.05, 0.2]
b3	[-0.05, 0.1]
b4	[-0.05 0.05]

Receiver A DFE Tap Weight Constraints



Receiver A DFE Tap Weights from Whole Link Simulation

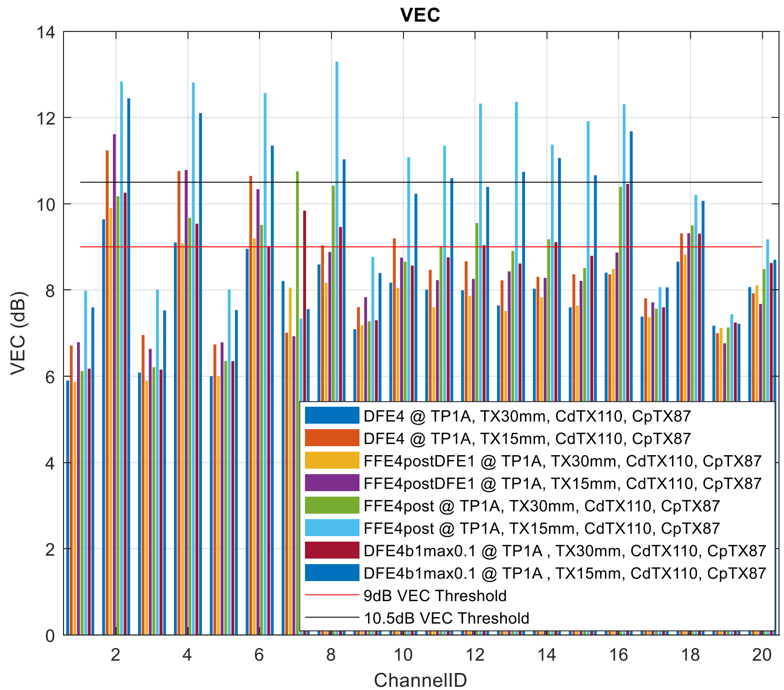
- **Anslow_3ck_01_0119 shows DFE can be used for C2M interface given tap weights are properly managed.**
- Precoding is not effective on some burst errors. Burst errors caused by multiple-tap DFE is one of them.
- Burst errors of multi-tap DFE is studied to avoid being too optimistic about precoding performance.

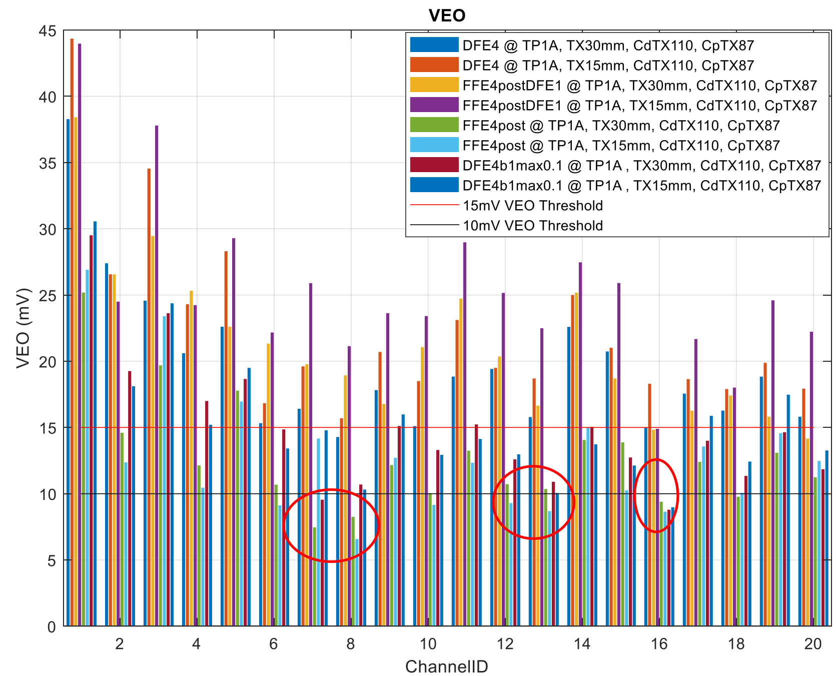
What Channels are Supported

Channel ID	Channel Description	Insertion Loss at 26.5625GHz (dB)	COM (dB) 30mm TX Pkg	COM (dB) 20mm TX Pkg
1	mellitz_3ck_01_0518_C2M\9dB	8.95	4.25	4.48
2	mellitz_3ck_01_0518_C2M\10dB	9.96	1.92	1.66
3	mellitz_3ck_01_0518_C2M\11dB	11.16	4.41	4.56
4	mellitz_3ck_01_0518_C2M\12dB	12.18	2.14	1.89
5	mellitz_3ck_01_0518_C2M\13dB	13.12	4.38	4.58
6	mellitz_3ck_01_0518_C2M\14dB	13.87	2.39	2.04
7	tracy_100GEL_02_0118\long_barrel_via\TX5	16.48	3.42	3.22
8	tracy_100GEL_02_0118\long_barrel_via\TX6	16.08	2.75	2.81
9	tracy_100GEL_06_0118\Microvia\RX6	14.59	3.64	3.78
10	tracy_100GEL_06_0118\Microvia\RX5	14.57	2.99	3.30
11	lim_3ck_01_0918_QDD_legacy_pairs\12dB	12.75	3.49	3.90
12	lim_3ck_01_0918_QDD_legacy_pairs\14dB	14.02	3.51	3.95
13	lim_3ck_01_0918_QDD_legacy_pairs\16dB	15.83	3.73	3.97
14	llim_3ck_01_0918_QDD_new_pairs\12dB	12.19	3.52	3.90
15	llim_3ck_01_0918_QDD_new_pairs\14dB	13.99	3.77	4.00
16	llim_3ck_01_0918_QDD_new_pairs\16dB	15.96	3.30	3.73
17*	ito_3ck_01\QSFP \bottom normal\	15.10	3.38	3.26
18	ito_3ck_01\QSFP \bottom worst\	15.58	2.59	2.53
19	ito_3ck_01\QSFP \top normal\	14.53	3.63	3.60
20	ito_3ck_01\QSFP \top worst\	14.49	2.99	2.96

- If real receiver is receiver A or B, the channels achieving 3dB COM can be supported.
- COM results are with reference receiver A, 15mm RX package.

TP1A Simulation Results

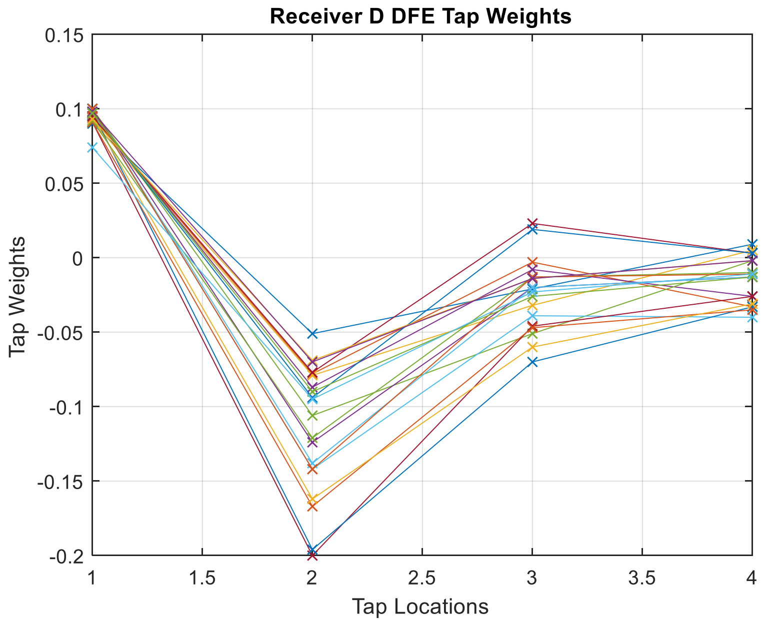




Possible TP1a Criteria	Reference Receiver	VEC Threshold	VEO Threshold	Channels Fail or Marginal
1	A, B	9dB	15mV	2, 4, 6, 8, 18
2	C, D	10.5dB	10mV	2, 4, 6, 7, 8, 10, 11-16, 18

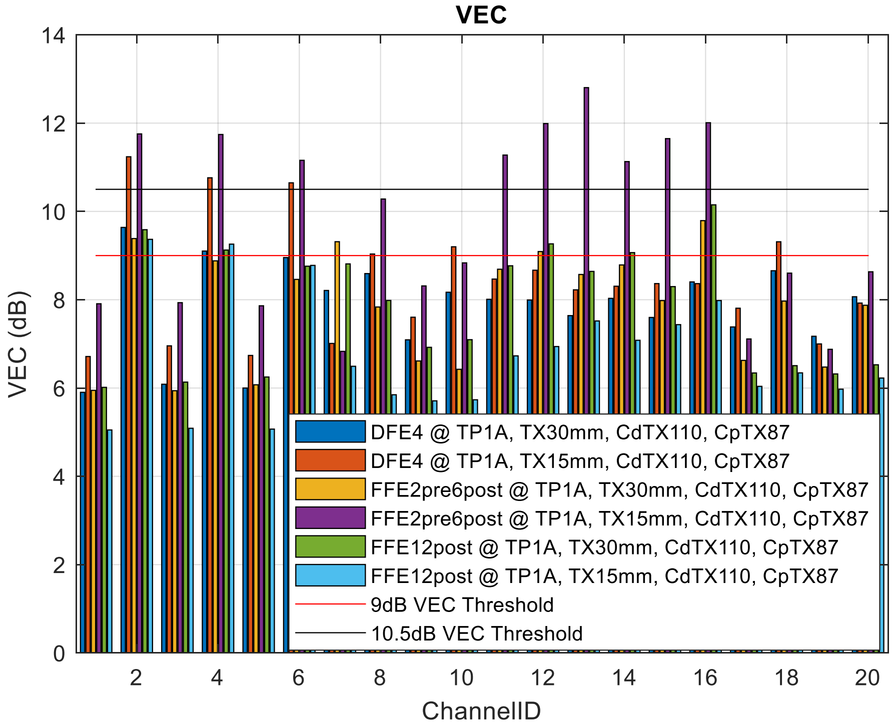
- More channels fail with criteria #2.
- High-loss channels have low VEO with receiver C. DFE b1max=0.5 improves VEO by 70%.
- 10.5dB VEC threshold is corresponding to 3dB COM.

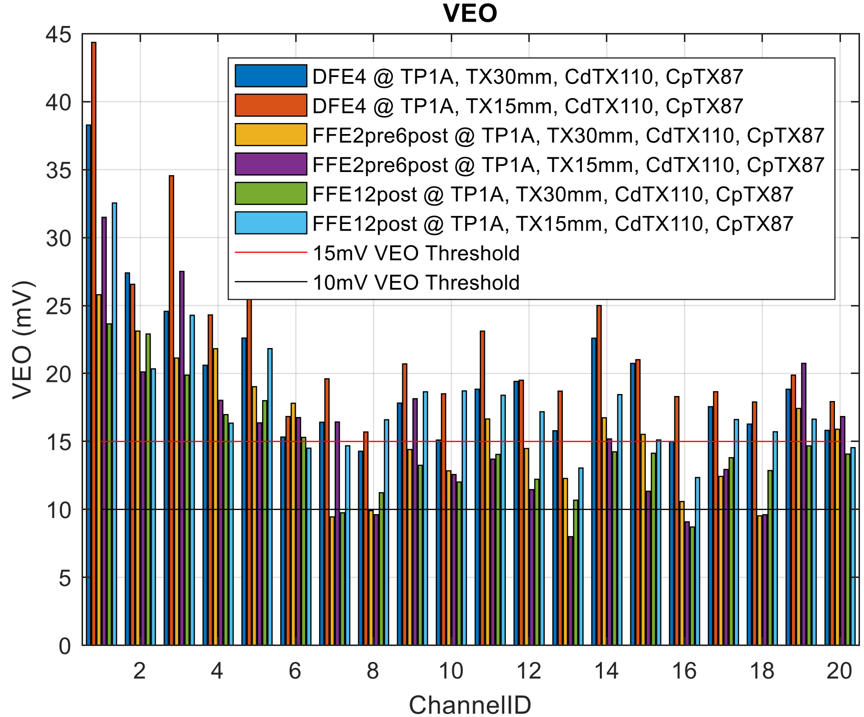
Receiver D Tap Weights



- Receiver D has small DFE tap1.

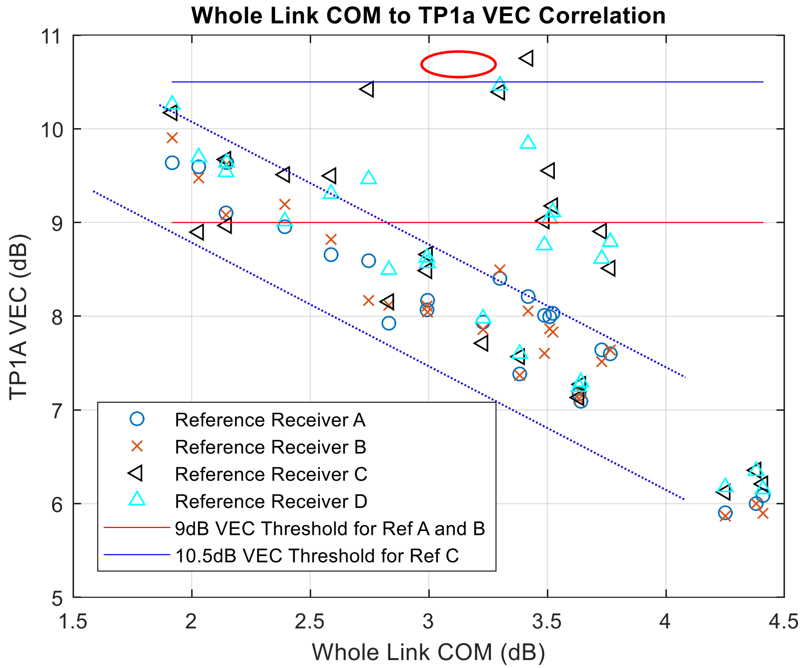
TP1A Simulation With More Receivers





- Two longer receivers are simulated.
- Both FFE2pre6post and FFE12post have difficulty to filter out bad channels.
- **FFE2pre6post and FFE12post will force implementations to have long equalizers.**
- **FFE2pre6post will allow wild TX FIR and result in interop challenge.**

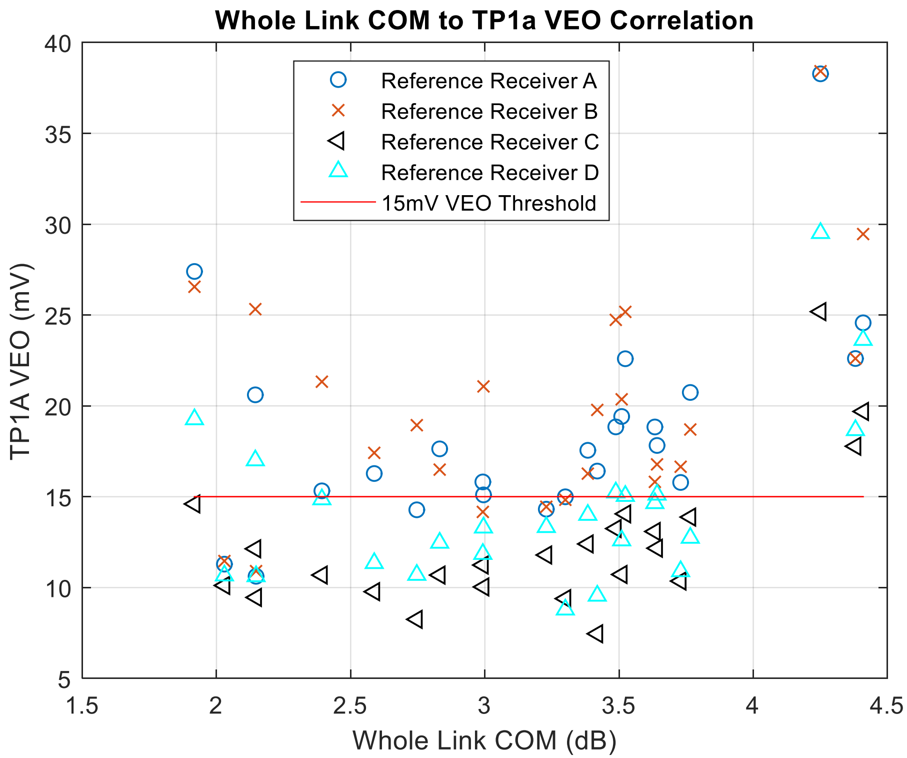
Correlation of TP1A VEC to COM



With whole link receiver DFE4, 30mm pkg

- Correlation is observed between whole link COM and TP1a VEC.
- Correlation appears stronger with receiver A and B. With reference receiver C, channel #7 in red circles need to be improved to avoid being excluded.

Correlation of TP1A VEO to COM



With whole link receiver DFE4

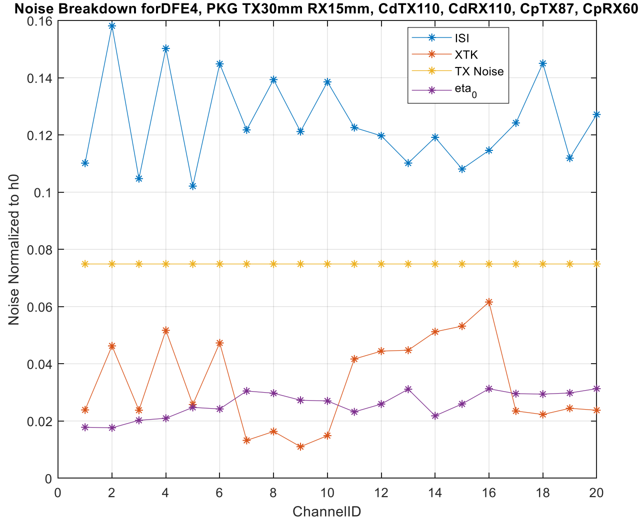
- Whole link COM has no correlation to TP1a VEO.

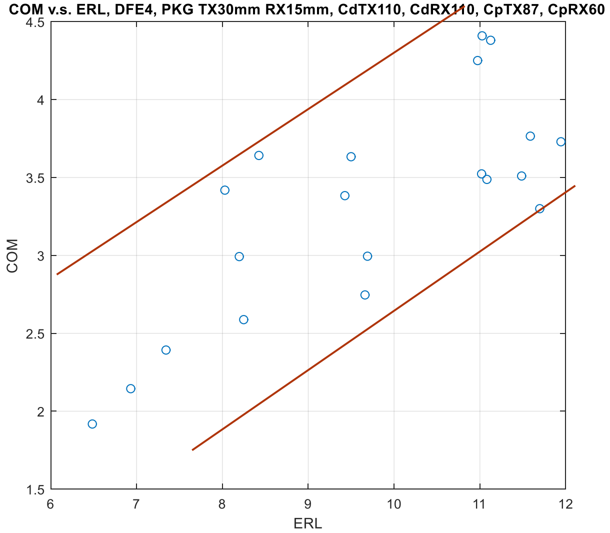
Summary of Reference Receivers

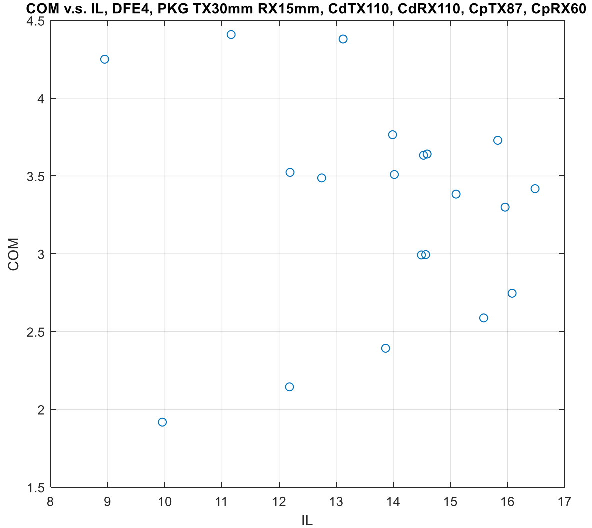
Receiver	Configuration	b1max	Threshold VEC/VEO	Reuse Annex 93A	Sufficient for Whole Link
A	4-tap DFE, b1max=0.5	0.5	9dB/15mV	Yes	Yes
B	5-tap FFE + 1-tap DFE	0.5	9dB/15mV	No	Yes
C	5-tap FFE	0.0*	10.5dB/10mV	No	No
D	4-tap DFE, low b1max	0.1	10.5dB/10mV	Yes	No

* Performance wise, receiver B, C, D are roughly equivalent to receiver A with different b1max.

COM Analysis

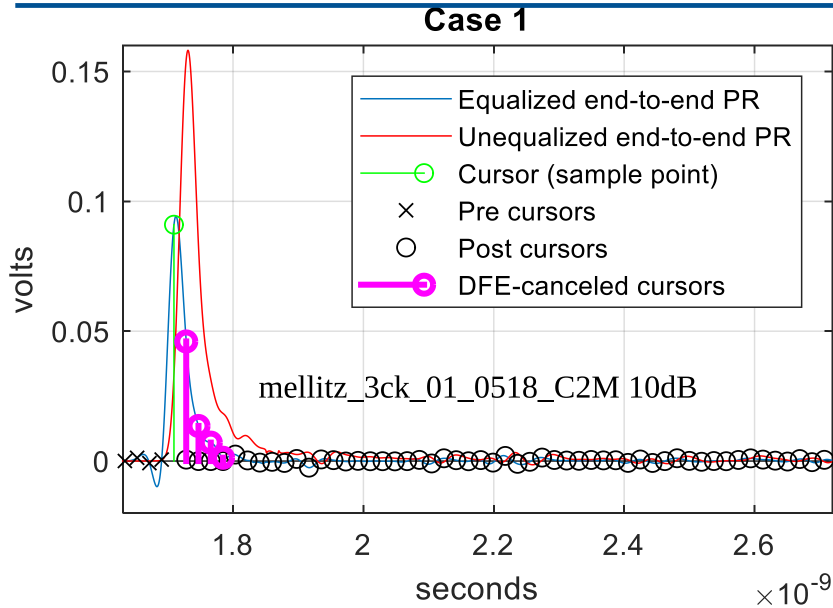


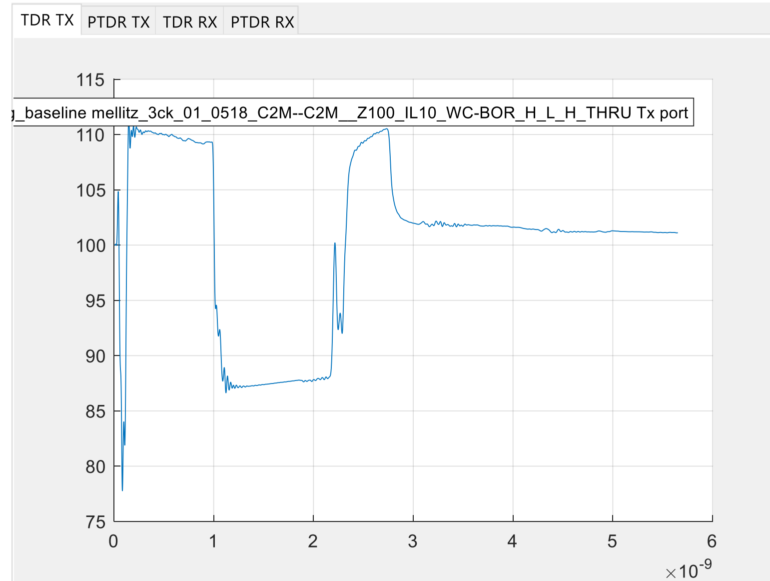


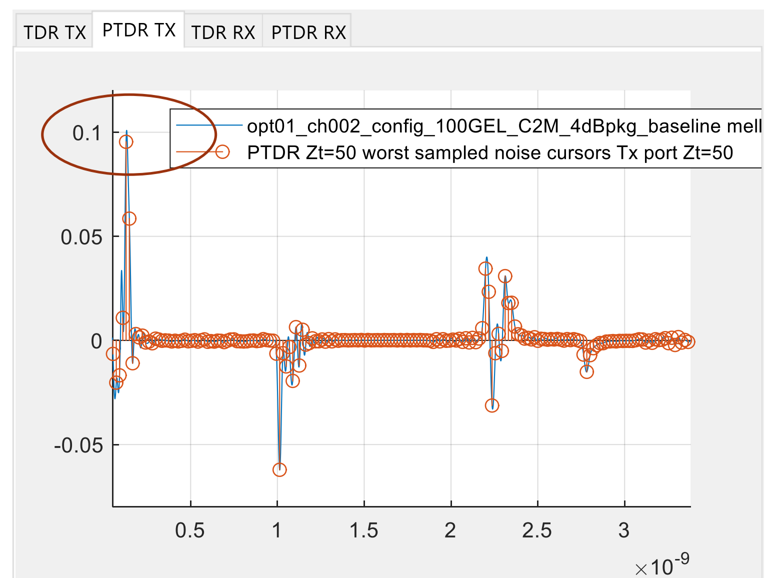


- ISI is the major contributor.
- COM is correlated to ERL.
- Not strong correlation found between COM and IL.
- XTK level of the these channels are very different.

Low COM Channel Analysis – Ch #2

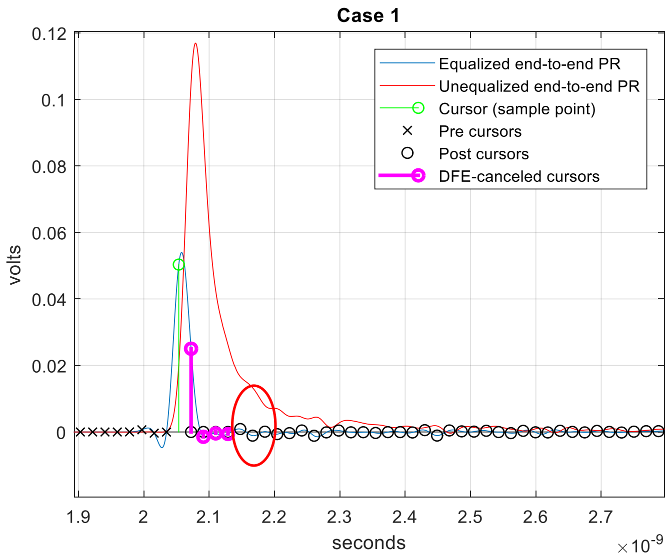


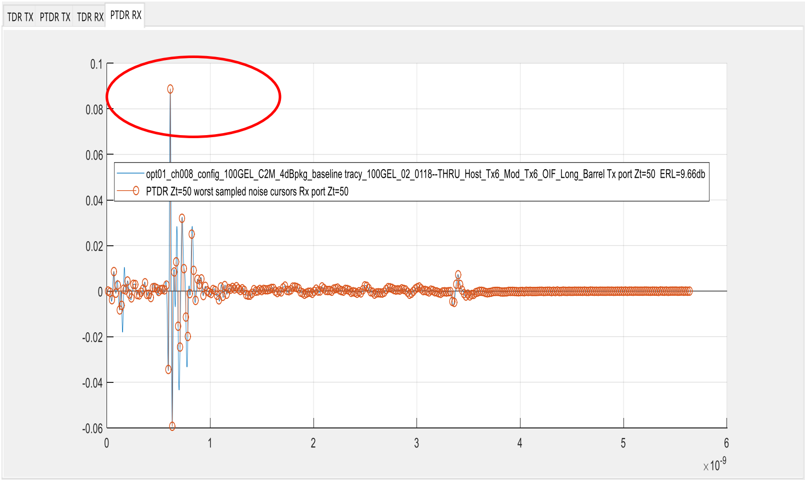




- mellitz_3ck_01_0518_C2M 10dB, 12dB, 14dB (worst case channels) have bad reflections at multiple locations.
- mellitz_3ck_01_0518_C2M 9dB, 11dB, 13dB (best case channels) are OK.

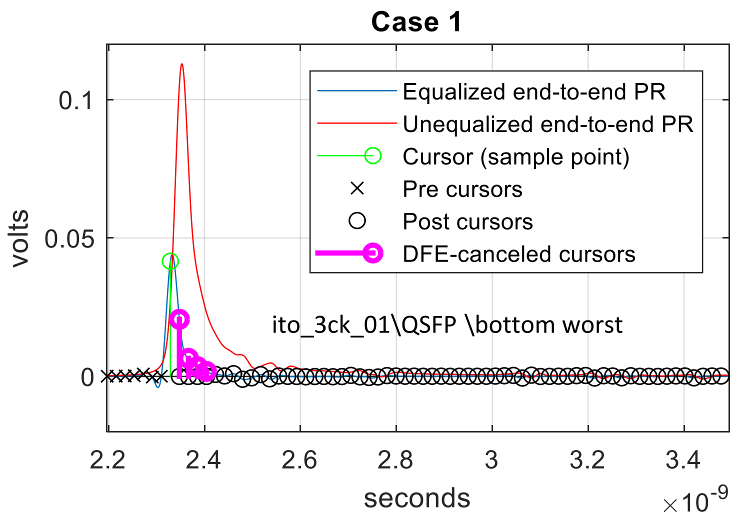
Low COM Channel Analysis – Ch #8

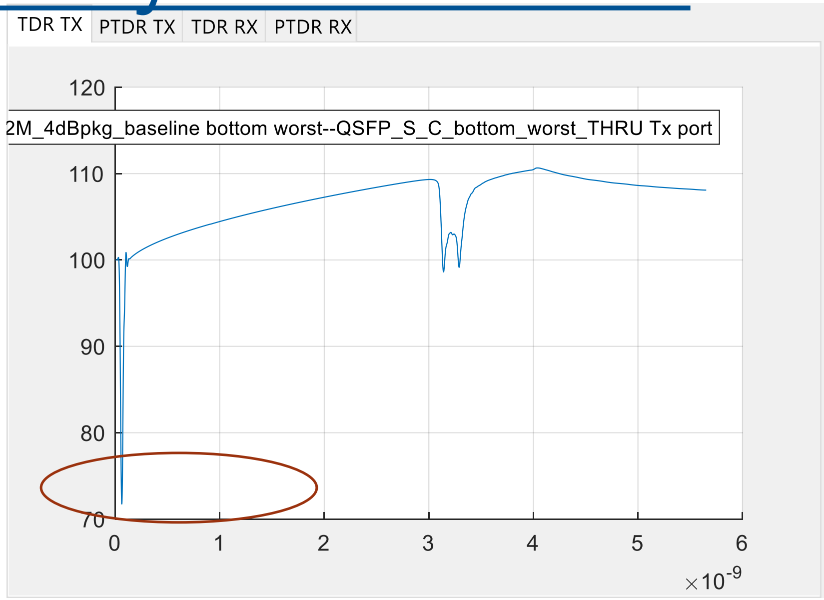




- Channel #8 has bad reflections at tap 5 to 7. Its insertion loss exceeds 16dB.

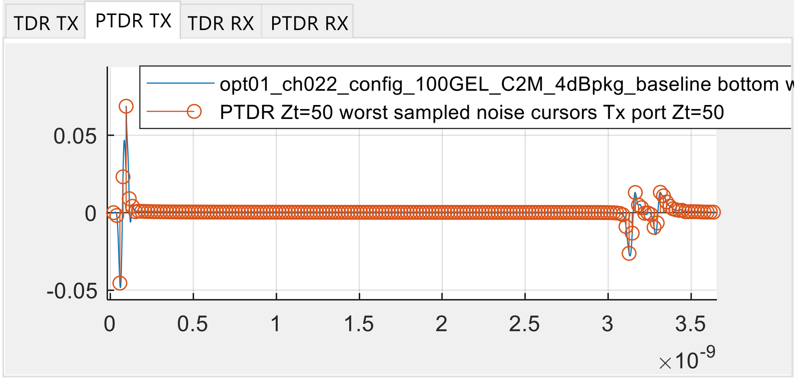
Low COM Channel Analysis – Ch #18



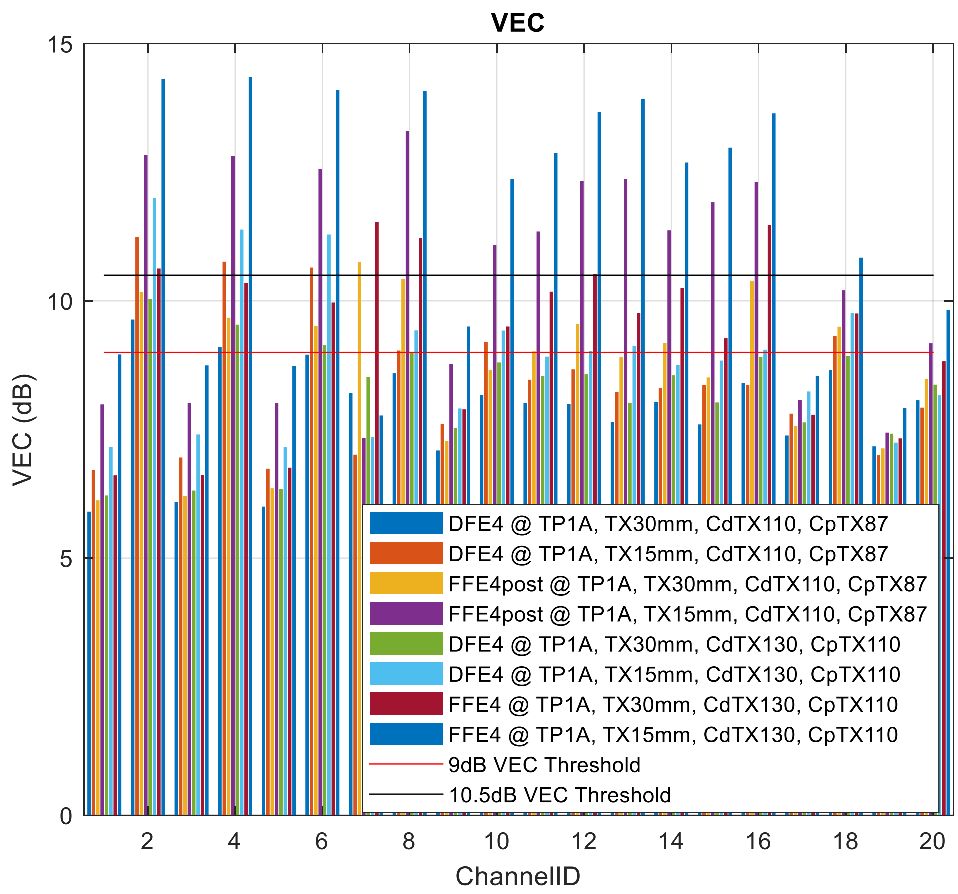


ito_3ck_01 QSFP bottom worst and top worst have bad reflections.

ito_3ck_01 QSFP bottom normal and top normal are OK

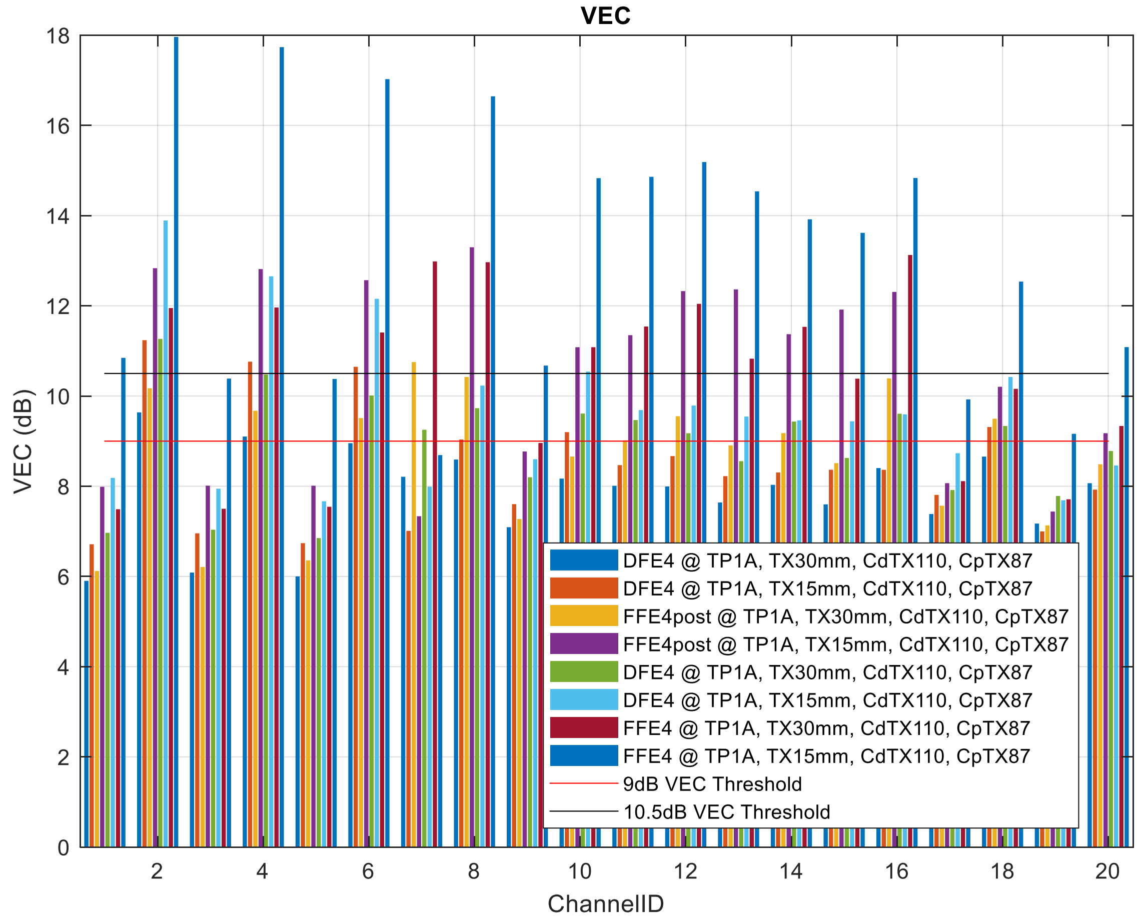


Impact of Cd



- Increasing Cp TX from 110fF to 130fF degrades VEC by about 0.42dB in average for DFE4 receiver, and 0.76dB for FFE4post.

Impact of Legacy Cd and Cp



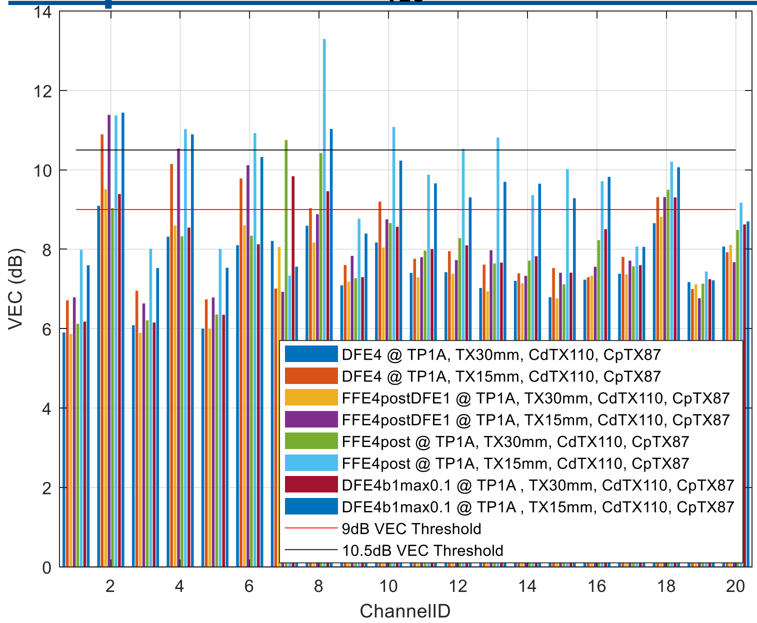
- For Cd and Cp values used for 50G (Cd=130fF, Cp=110fF), VEC is degraded by 1.12dB for DFE4, and 2.11dB for FFE4post.
- **Legacy Cd, Cp cannot be supported.**

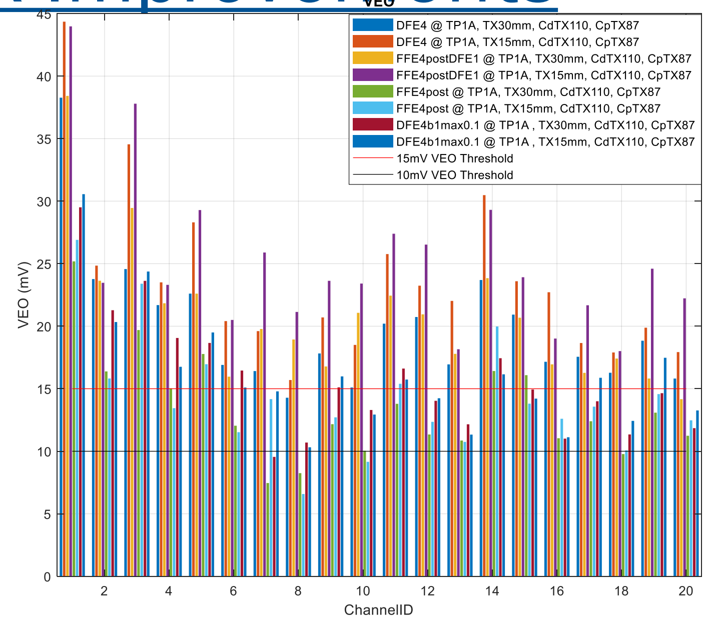
XTK Can be Improved?

Channel ID	Channel Description	ICN before Change (mV)	ICN after Change (mV)
1	mellitz_3ck_01_0518_C2M\9dB	2.28	2.28
2	mellitz_3ck_01_0518_C2M\10dB	4.53	2.26
3	mellitz_3ck_01_0518_C2M\11dB	1.93	1.93
4	mellitz_3ck_01_0518_C2M\12dB	3.99	1.99
5	mellitz_3ck_01_0518_C2M\13dB	1.68	1.68
6	mellitz_3ck_01_0518_C2M\14dB	3.19	1.60
7	tracy_100GEL_02_0118\long_barrel_via\TX5	0.91	0.91
8	tracy_100GEL_02_0118\long_barrel_via\TX6	0.90	0.90
9	tracy_100GEL_06_0118\Microvia\RX6	0.83	0.83
10	tracy_100GEL_06_0118\Microvia\RX5	0.93	0.93
11	lim_3ck_01_0918_QDD_legacy_pairs\12dB	2.70	1.35
12	lim_3ck_01_0918_QDD_legacy_pairs\14dB	2.50	1.25
13	lim_3ck_01_0918_QDD_legacy_pairs\16dB	2.14	1.07
14	llim_3ck_01_0918_QDD_new_pairs\12dB	3.37	1.68
15	llim_3ck_01_0918_QDD_new_pairs\14dB	2.76	1.38
16	llim_3ck_01_0918_QDD_new_pairs\16dB	2.65	1.33
17	ito_3ck_01\QSFP \bottom normal\	1.20	1.20
18	ito_3ck_01\QSFP \bottom worst\	1.14	1.14
19	ito_3ck_01\QSFP \top normal\	1.25	1.25
20	ito_3ck_01\QSFP \top worst\	1.21	1.21

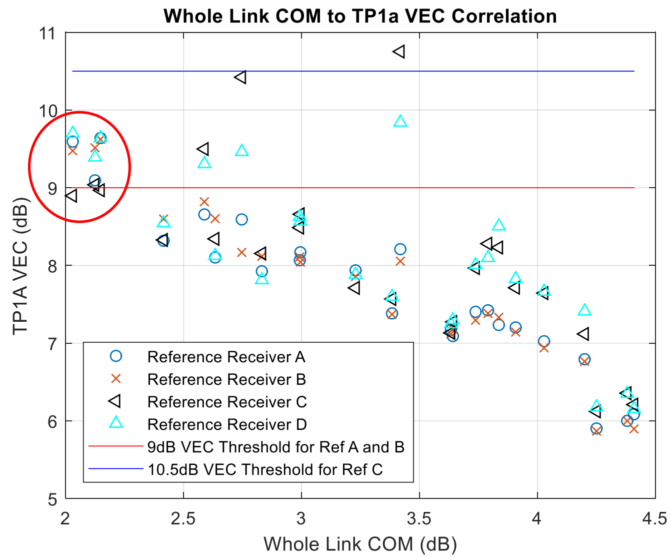
- Highlighted ICN are reduced by 6dB.

Impact of Possible XTK Improvements





- With XTK improvement for high ICN channels, all channels within insertion loss budget pass VEO thresholds (ch10 is marginal with receiver C).
- Channels 11-16 are pass VEC with margin for receiver A, B, and D, marginal for receiver C.
- Ch 2, 4, 6 end-to-end COM with 30mm package is low, but can pass VEC/VEO thresholds with receiver C and D. Other channel qualification constraints may be needed to work with receiver C and D.



Receiver A for Whole Link, 30mm package

Conclusions

- Four TP1A reference receiver candidates are analyzed. Receivers A and B have similar performance, C and D have similar performance.
  - Receiver A and D are better choices for reusing Annex 93A specifications.

- Channels that achieved 3dB COM in whole-link simulation can pass reference receiver A and B without further improvements. Some channels need to be improved to pass receiver C and D.

- Whole link C2M channels can be more than 20dB and have high XTK. Therefore DFE tap1 is effective on performance. Without sufficient DFE b1max long linear equalizer is needed.
  - Real receiver is expected to be stronger than reference receiver C and D regardless which reference receiver is picked.

- Suggest channels to improve reflection and XTK. More study is needed for more detailed thresholds.