KR/CR Simulation Results with COM Tool 2.57

IEEE P802.3ck Task Force

Phil Sun, Yasuo Hidaka

Credo Semiconductor

Introduction

- There are discussions regarding performance of different KR/CR reference receivers.

- This contribution simulated all **115** KR/CR channels submitted to 802.3ck project (including 100GEL) with the three reference receivers under discussion.
  - A: Existing long DFE receiver.
  - B: Long FFE + 1-tap DFE receiver.
  - C: 3-tap FFE precursor + long DFE post cursor receiver.

- Extensive studies have been performed to support 100G KR/CR channels, e.g., package models and equalization parameters. Some important improvements made to support 100G KR/CR channels are analyzed.

- This simulation is based on COM tool 2.57 as requested in minutes_121918_3ck_adhoc.

COM Spread Sheet

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[12 30; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 30; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 30; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 30; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=.694
A_fe	0.413	V	vp/vf=.694
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02:0]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	24	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.25	
fixture delay time	0	enter sec
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	119	mm
z_bp (NEXT)	119	mm
z_bp (FEXT)	119	mm
z_bp (RX)	119	mm

Simulation Conditions

Model Name		DFE (DFE-based)	PDFE (DFE + 3 pre-taps)	FFE (FFE-based)
# of taps	DFE	24 / 16	24	1
	FFE	0	4 (3-pre + 0-post)	28 (3-pre + 24-post) / 20 (3-pre + 16-post)
	TX FIR	5 (3-pre + 1-post)		
Step	RX DFE, FFE	0%		
	TX FIR pre	1.5% / 2.0% / 2.5%	2.0% / 2.5%	1.5% / 2.0% / 2.5%
	TX FIR post	5%		
DFE b1max		0.7 / 0.85 / 1.0	0.7 / 0.85	0.7 / 0.85

- Label of Simulation Condition: Prefix + Model Name + Suffix (+ Option)
  - Prefix: step of TX FIR pre taps
    - None: 1.5%, C (coarse): 2.5%, M (Medium): 2.0%
  - Suffix: DFE b1max value
  - Option: deviation from default condition
    - ENOB5.2: optional model of ADC effective number of bits as 5.2 (default is no ENOB model)
    - Nb16: 16-tap DFE (default is 24-tap DFE)
    - pst16: 20-tap (3-pre + 16-post) FFE (default is 28-tap (3-pre + 24-post) FFE)
  - Example
    - CDFE0.85: DFE-based with DFE b1max=0.85 and 2.5% step of TX FIR pre taps
    - PDFE0.7: DFE + pre-taps with DFE b1max=0.7 and 1.5% step of TX FIR pre taps

- Modifications Made to COM 2.57:
  - To guarantee full grid search, “break” is changed “continue” on line 2642 per discussion with Rich Melitz.
  - The number of equalizer post taps is changed from 16 to 24, as shorter equalizers have already been covered by earlier studies [1].
  - bmax(2:Nb) is relaxed from 0.2 to 0.3 to tolerate higher b2. This will also alleviate error propagation.

Channel Data for Simulation

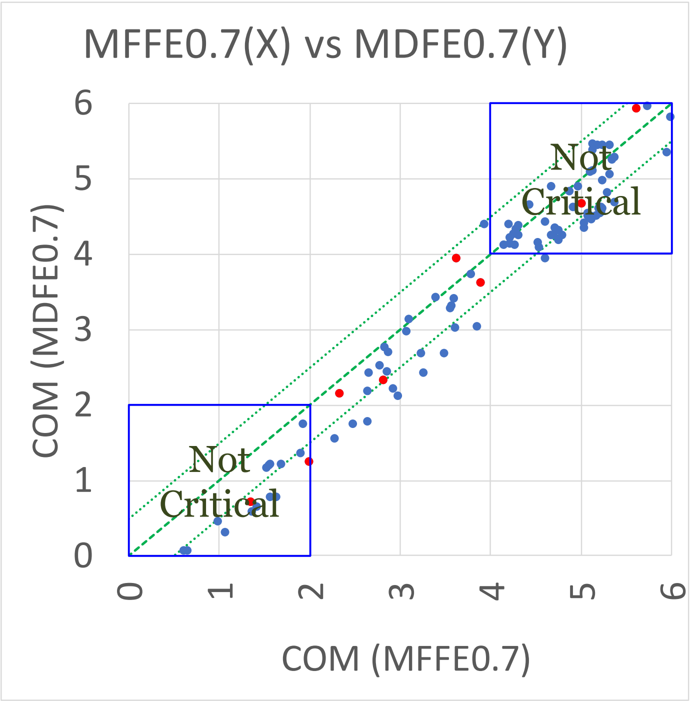
- Simulation was done for the following publicly available 115 LR channels
  - Among them, 8 channels are marked up with red dots in the plots.

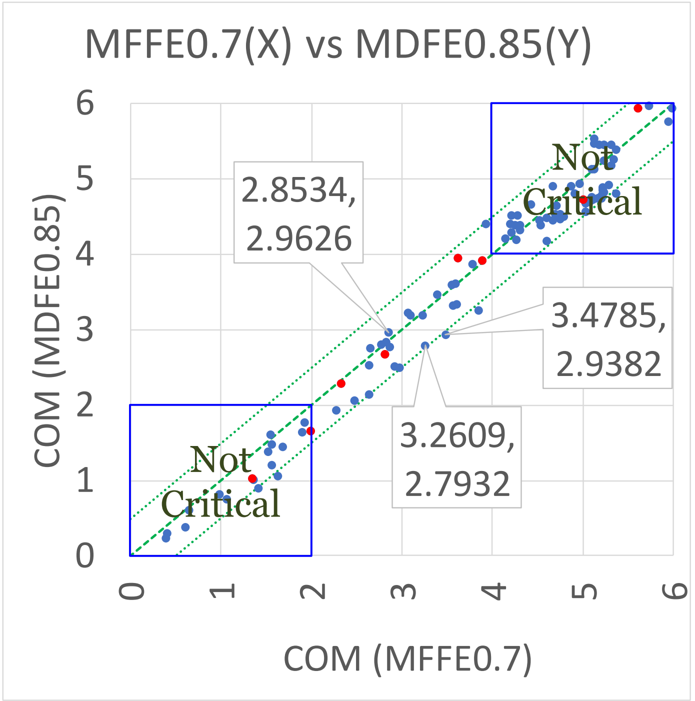
CH #	Channels marked with red dots	Group	Description	Reference Document
1-2		RM1	Two Very Good 28dB Loss Ideal Transmission Lines	mellitz_3ck_adhoc_02_072518.pdf
3-8	CH7 : CaBP_BGAVia_Opt2_28dB	RM2	24/28/32dB Cabled Backplane Channels including Via	mellitz_3ck_adhoc_02_081518.pdf
9-10		RM3	Synthesized CR Channels (2.0m and 2.5m 28AWG Cable)	mellitz_100GEL_adhoc_01_021218.pdf
11-13		RM4	Best Case 3”, 13”, 18” Tachyon Backplane	mellitz_100GEL_adhoc_01_010318.pdf
14-15		NT1	Orthogonal or Cabled Backplane Channels	tracy_100GEL_03_0118.pdf
16		AZ1	Orthogonal Backplane Channel	zambell_100GEL_01a_0318.pdf
17-19		HH1	Initial Host 30dB Backplane Channel Models	heck_100GEL_01_0118.pdf
20-35	CH21 : 16dB 575mm high ISI CH33 : 28dB 575mm high ISI	HH2	16/20/24/28dB Cabled Backplane Channels	heck_3ck_01_1118.pdf
36-54	CH36 : Bch1_3p5 CH46 : Bch2_a7p5_7	UK1	Measured Traditional Backplane Channels	kareti_3ck_01a_1118.pdf
55-73	CH68 : CAch3_b2	UK2	Measured Cabled Backplane Channels	
74-88	CH80 : OAch4 CH81 : Och4	UK3	Measured Orthogonal Backplane Channels	
89-115		AZ2	Measured Orthogonal Backplane with Varied Impedances	zambell_3ck_01_1118.pdf

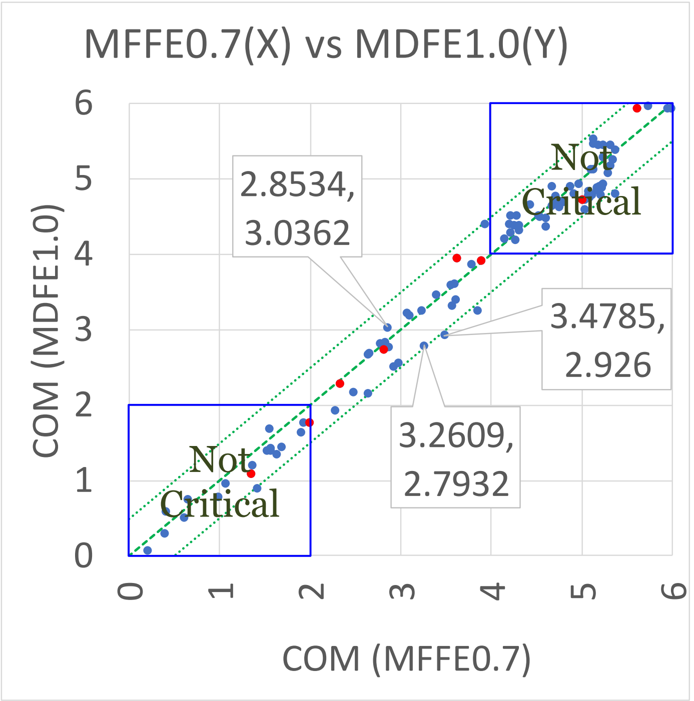
All channel data are taken from IEEE 100GEL Study Group and P802.3ck Task Force – Tools and Channels pages.
i.e. http://www.ieee802.org/3/100GEL/public/tools/index.html and http://www.ieee802.org/3/ck/public/tools/index.html

Performance Comparison of DFE and FFE Receivers

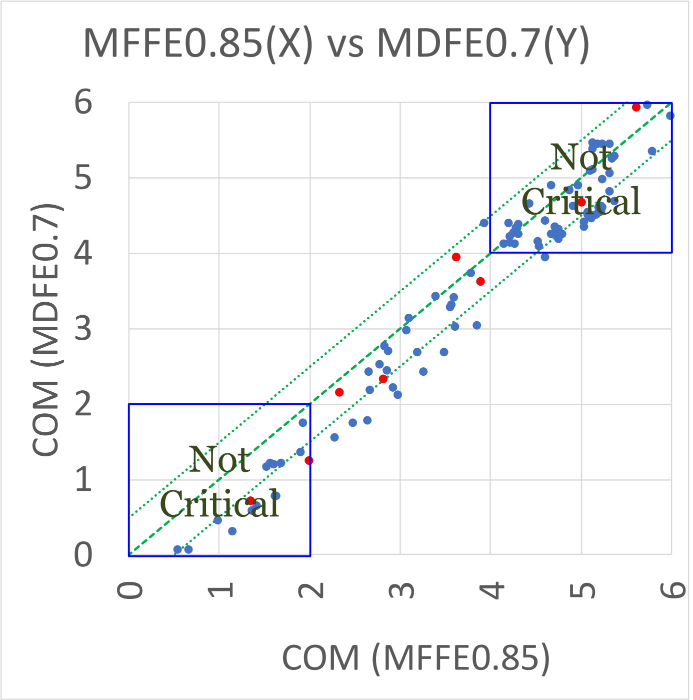
MFFE0.7 (X)
vs
MDFE* (Y)

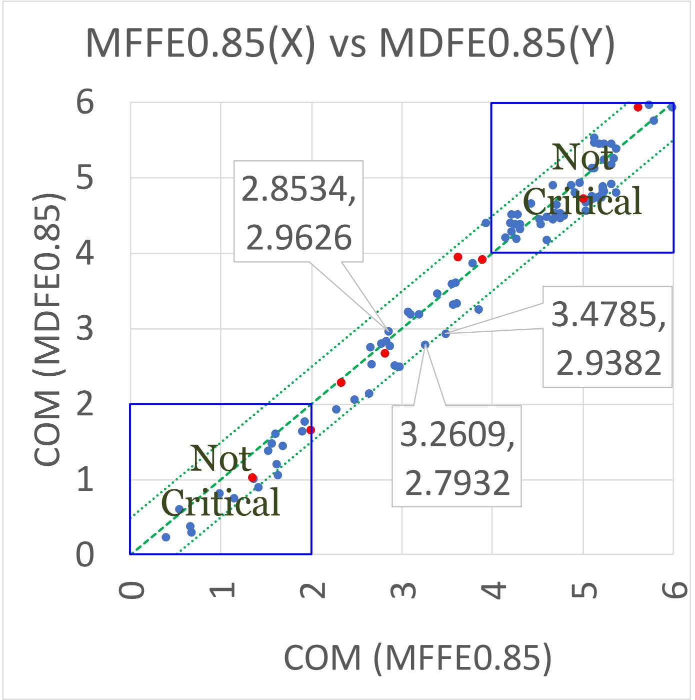


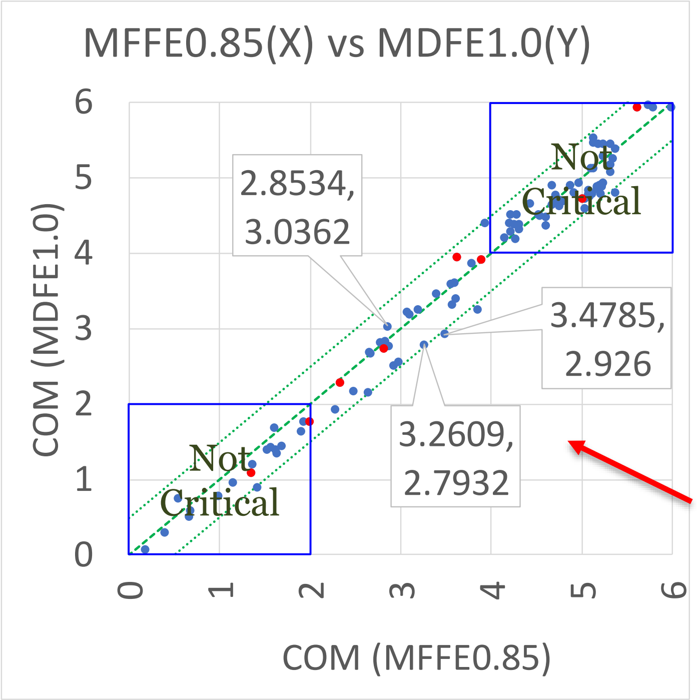




MFFE0.85 (X)
vs
MDFE* (Y)





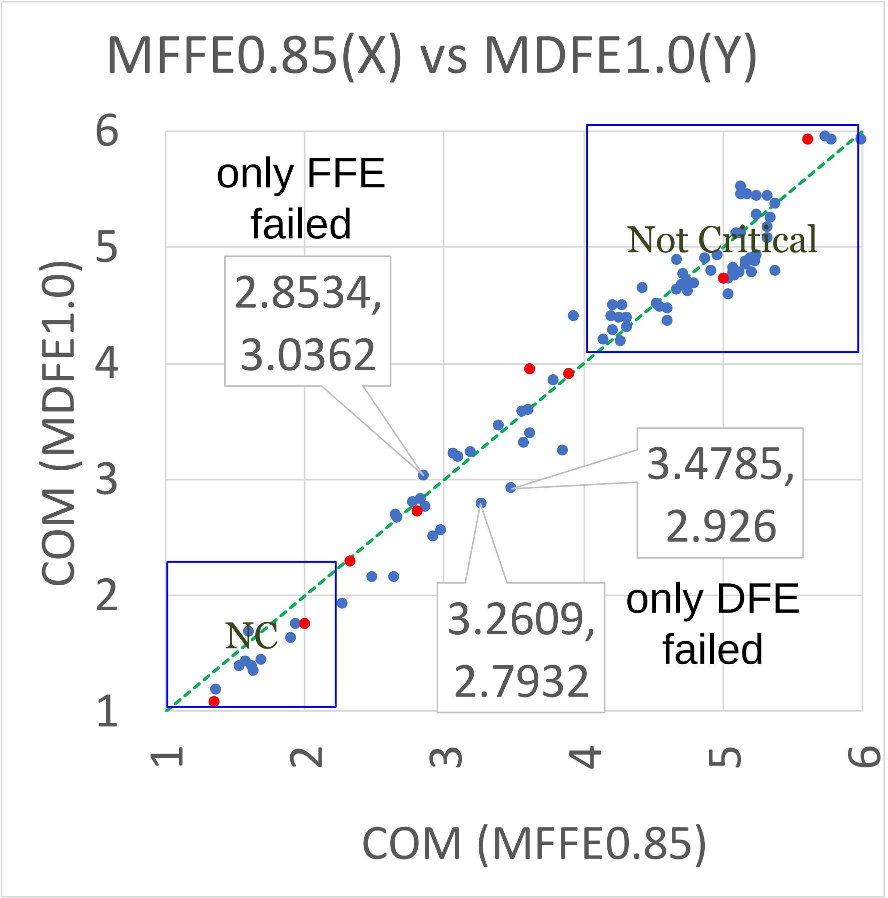


For 3 channels, FFE and DFE give inconsistent pass/fail result.

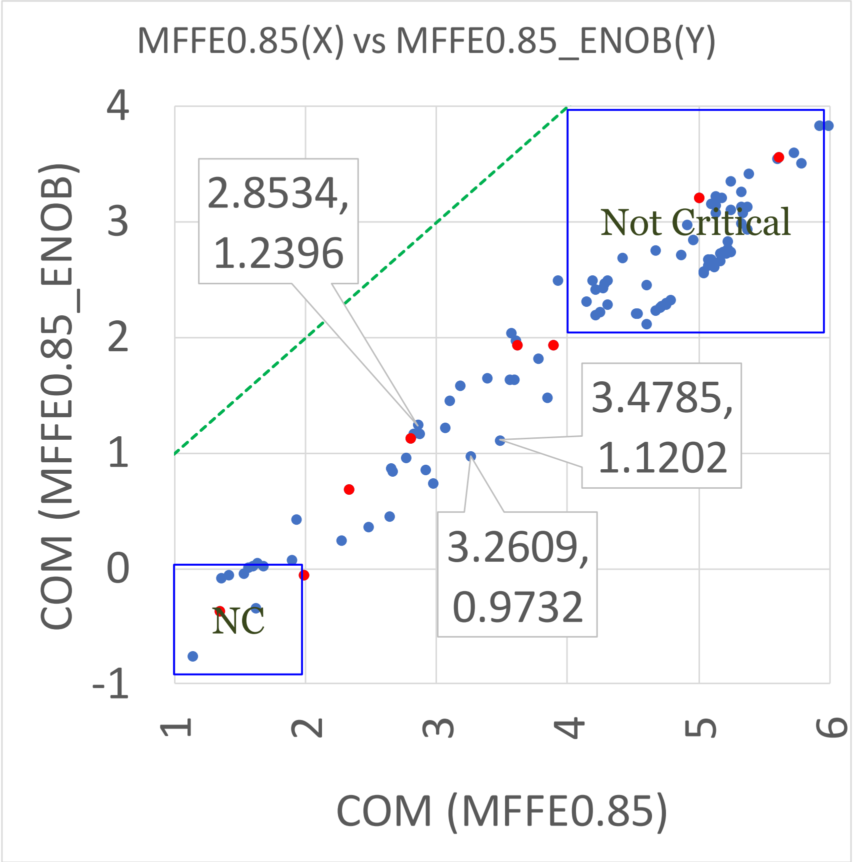
- With b1max=0.85, COM difference is within ~0.5dB for FFE and DFE receivers.
  - The pass/fail inconsistency are three channels passed by either FFE or DFE receiver but failed by the other receiver up to 0.2dB.

Inconsistent Channels Analysis

FFE model (X) v.s. DFE model (Y)



FFE model (X) v.s. Realistic FFE model (Y)



- For DFE-failed channels, degradation from model performance (right figure Y) to more realistic performance (right figure Y) is ~2.3dB that is larger than typical degradation (~2dB).
  - Not only DFE-based receivers, but also *real* FFE-based receivers are likely to fail these channels.
  - These channels should not pass.
- For FFE-failed channel, degradation from model performance to real performance is ~1.6dB that is smaller than typical degradation (~2dB).
  - Although ideal FFE model failed for this channel, this channel is relatively easy for *real* FFE-based receivers.

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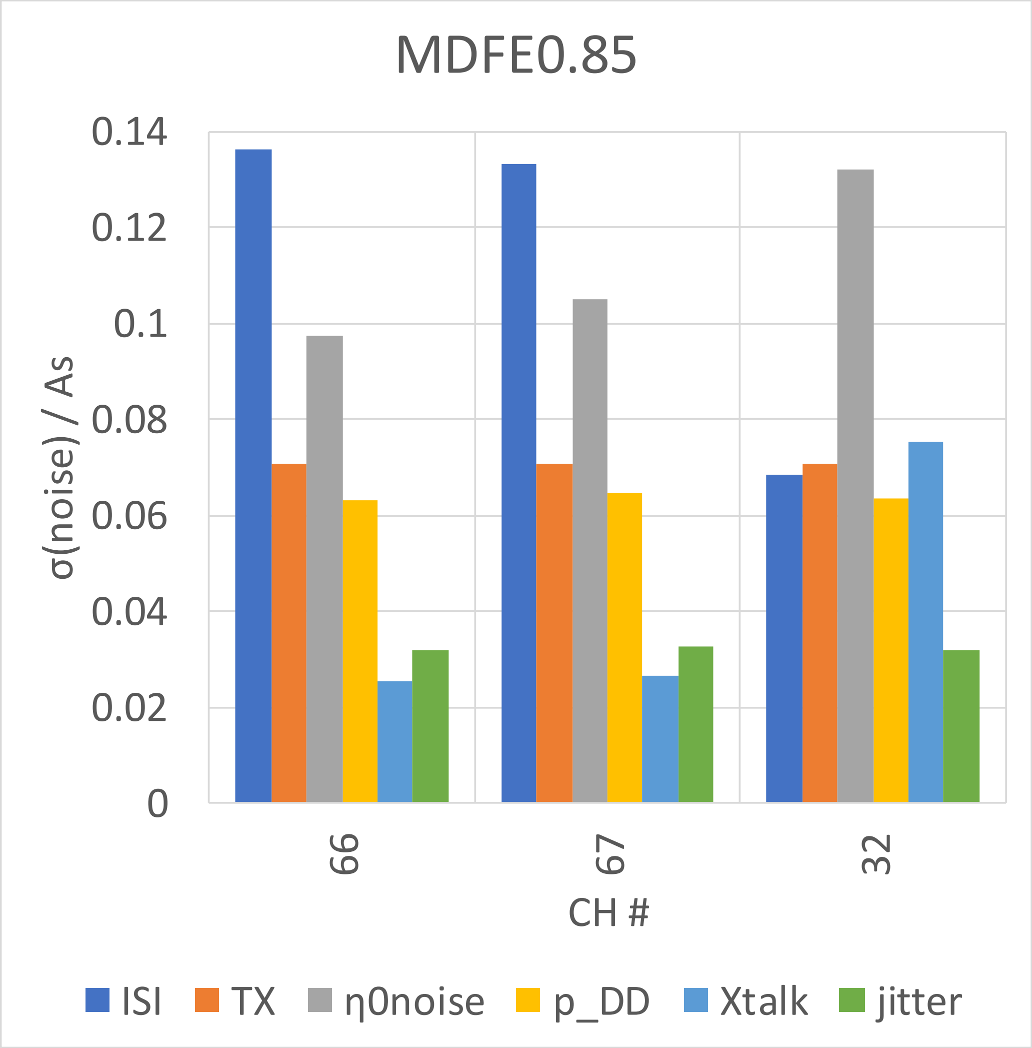
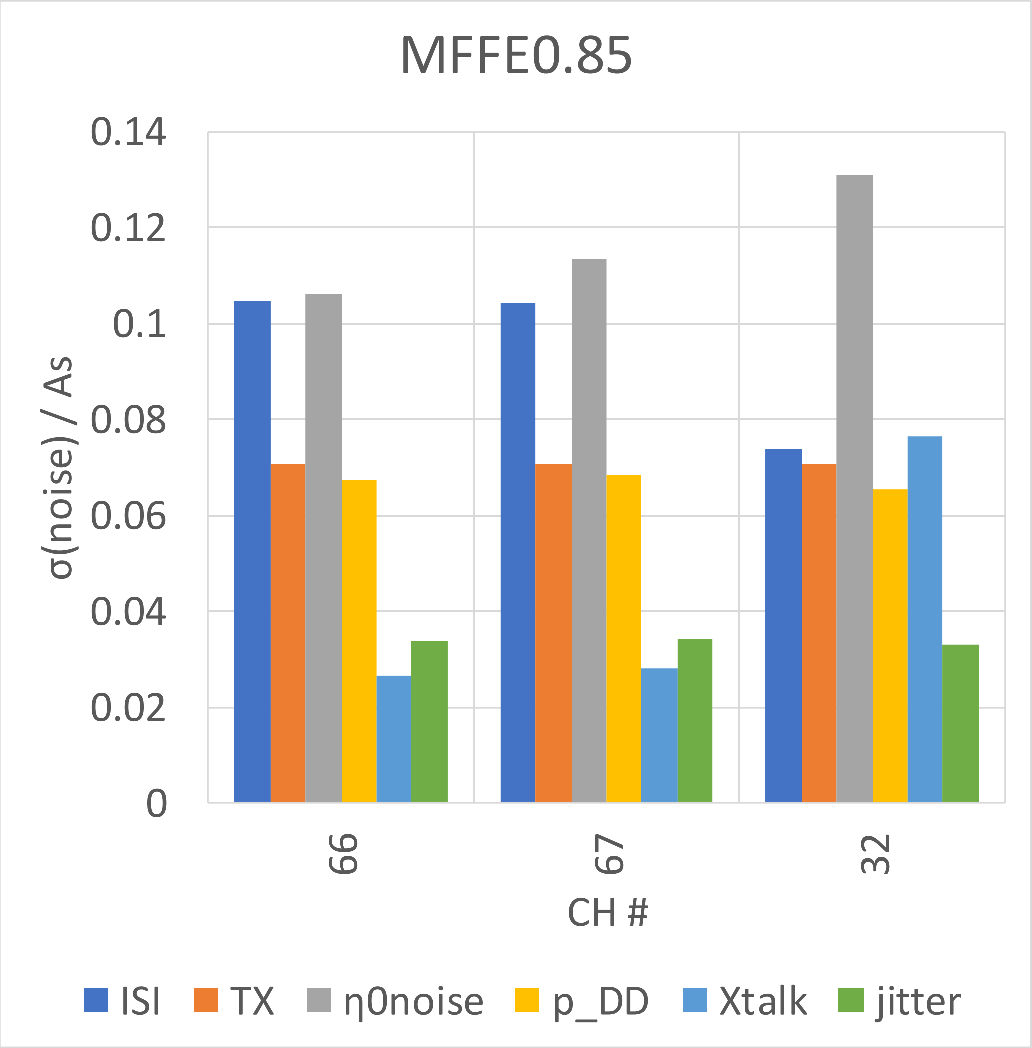
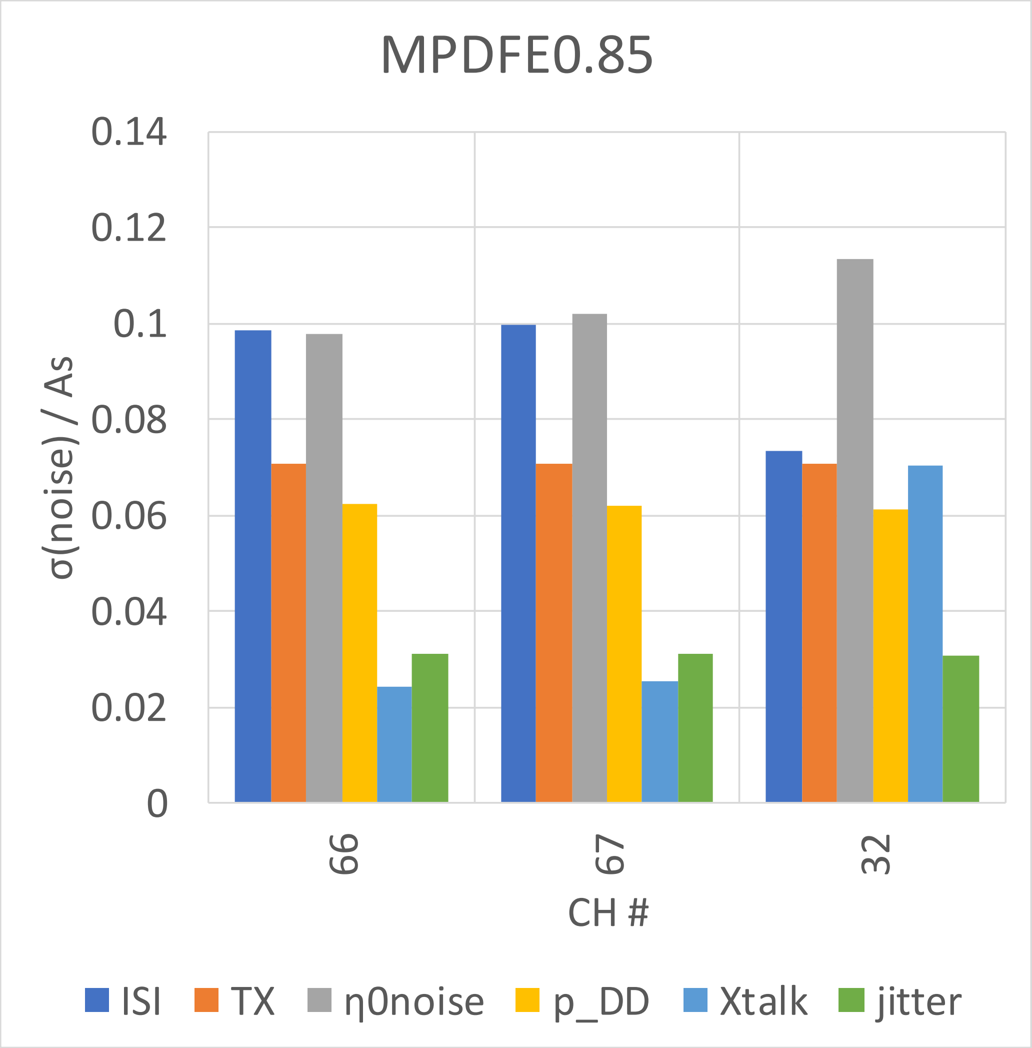
Inconsistent Channels Analysis

Channel	MDFE0.85 COM	MFFE0.85 COM	MPDFE0.85 COM	ERL with 24 taps	ICN	Fitted IL
#66	2.9382	3.4785	3.9994	11.31	0.54	26.19
#67	2.7932	3.2609	3.8493	11.27	0.54	26.88
#32	3.0362	2.8534	3.5566	19.99	1.56	29.66







- For channel #32, FFE and DFE have similar source of impairment. COM difference is small.
- For channel #66 and #67 DFE model sees higher normalized ISI.

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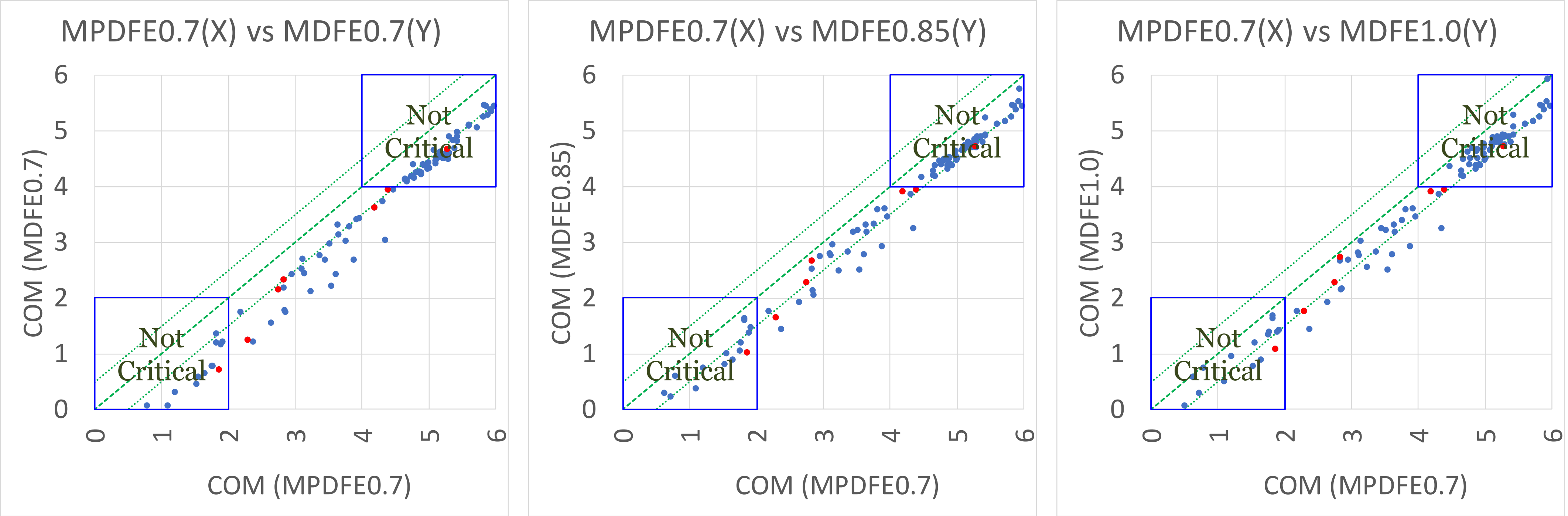
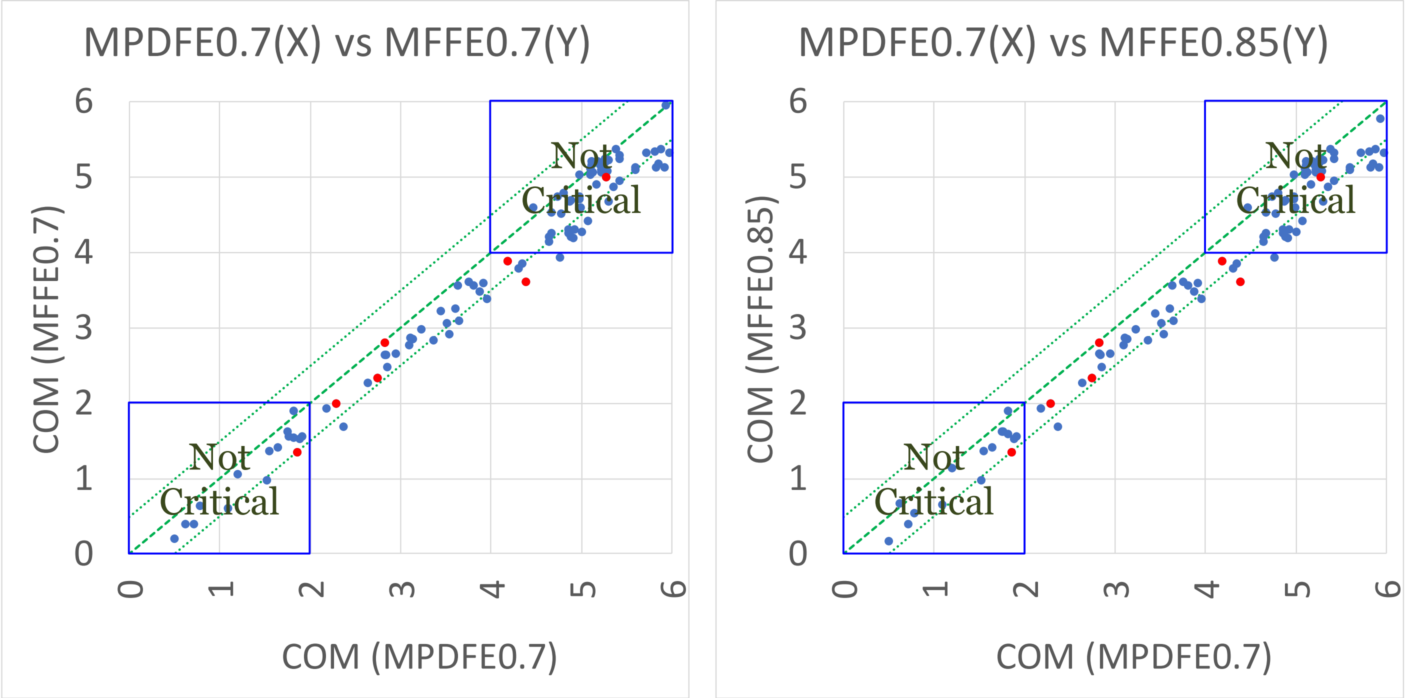
PDFE Receiver Performance



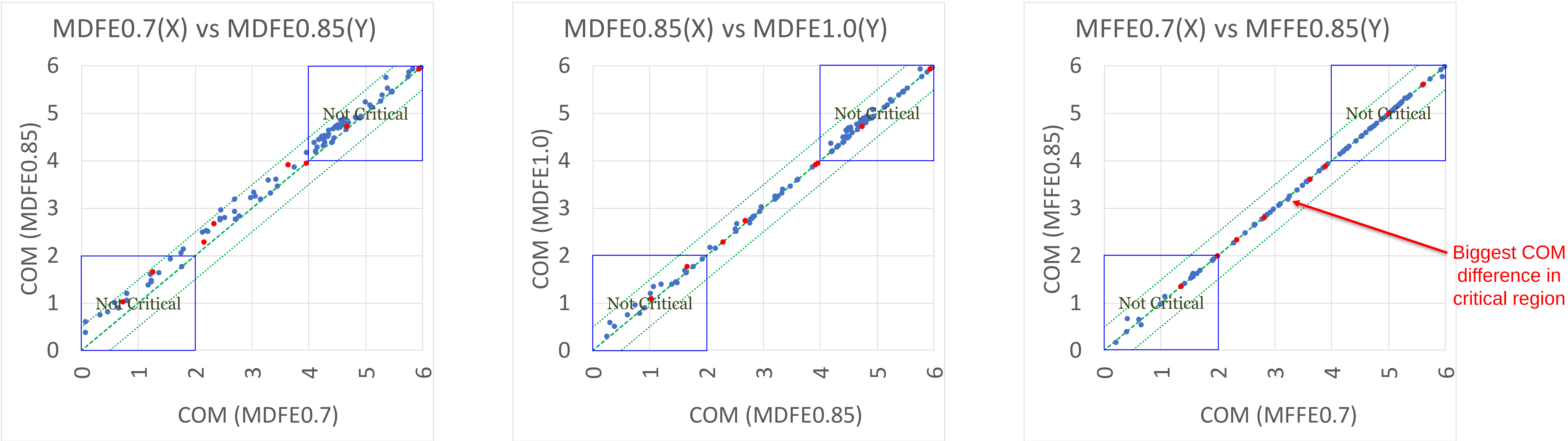
MPDFE0.7 (X) vs MDFE* (Y)



MPDFE0.7 (X) vs MFFE* (Y)

- PDFE is always better than DFE or FFE.
  - Even MPDFE0.7 (b1max=0.7) is mostly better than MDFE* and MFFE*.
    - MPDFE0.85 is always better than MPDFE0.7 (shown in backup)
- PDFE is an ideal analog SERDES architecture.
  - It has implementation penalties which is not captured by this ideal reference model.
- PDFE passes channels that cannot be supported by typical DFE or FFE receivers.

Receiver Performance with Relaxed b1max



- Performance difference close to 3dB threshold is more critical for channel qualification purpose.
- In critical region, DFE receiver performance can be up to ~0.5dB better if b1max is relaxed from 0.7 to 0.85.
- In critical region, DFE receiver performance can be up to ~0.14dB better if b1max is relaxed from 0.85 to 1.00.
- Relaxing b1max does not help FFE as much.
  - The biggest COM difference is FFE0.7 performs about 0.04dB better than FFE0.85.

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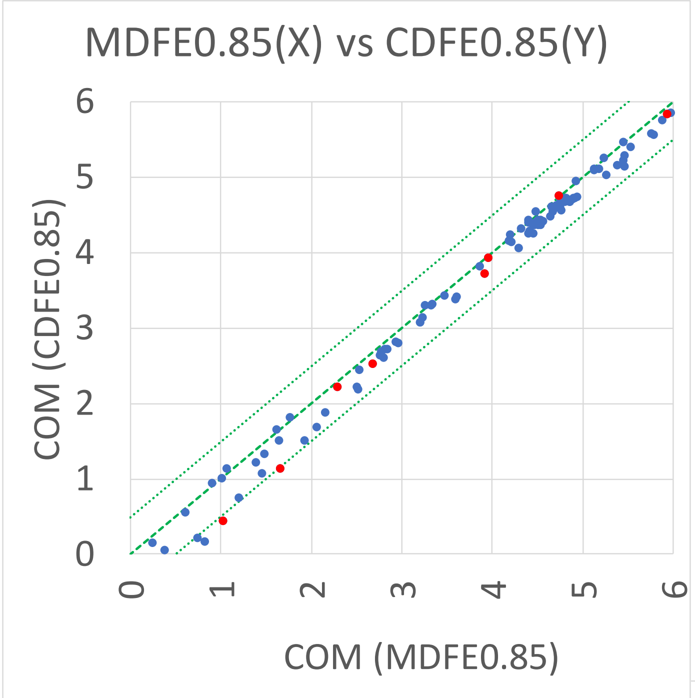
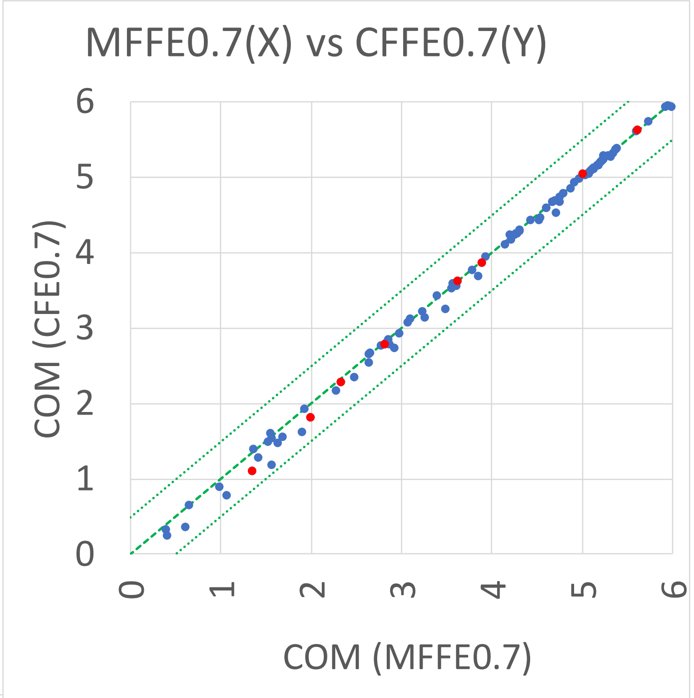
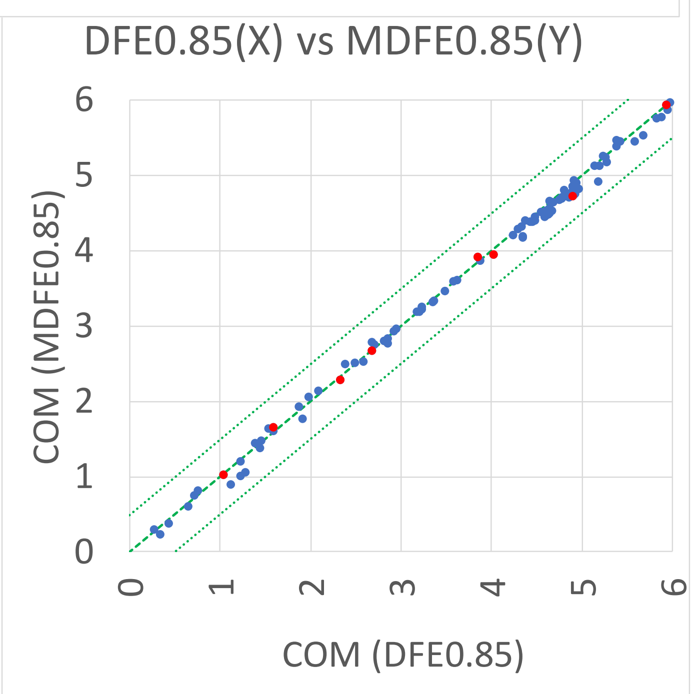
TX Resolution Impact

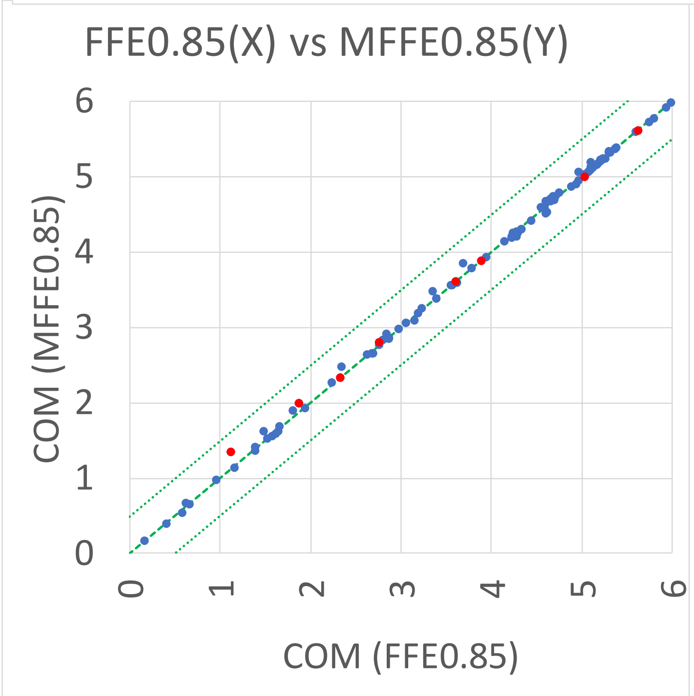
TX Resolution
2.0% (X) vs 2.5% (Y)





TX Resolution
1.5% (X) vs 2.0% (Y)

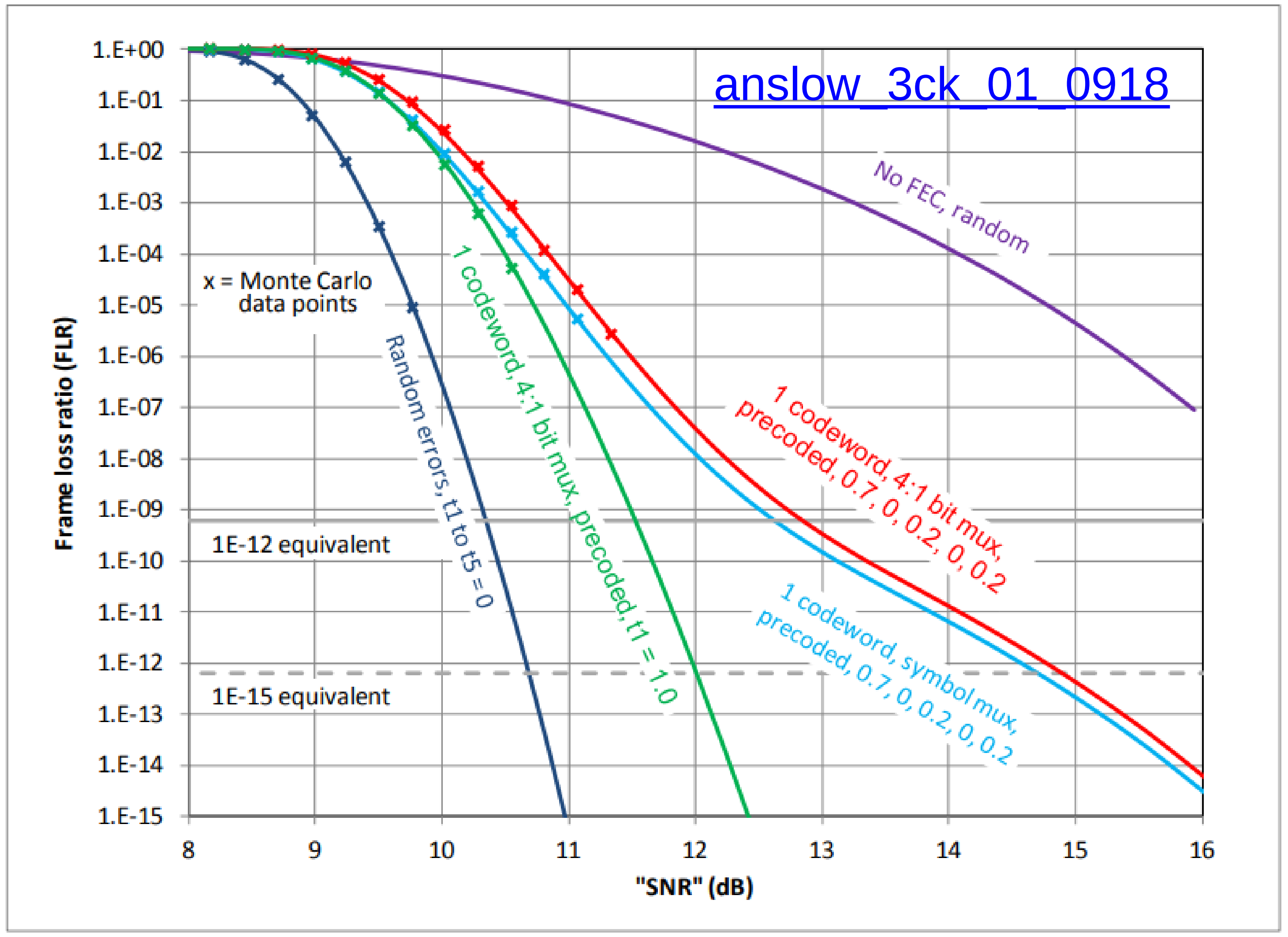




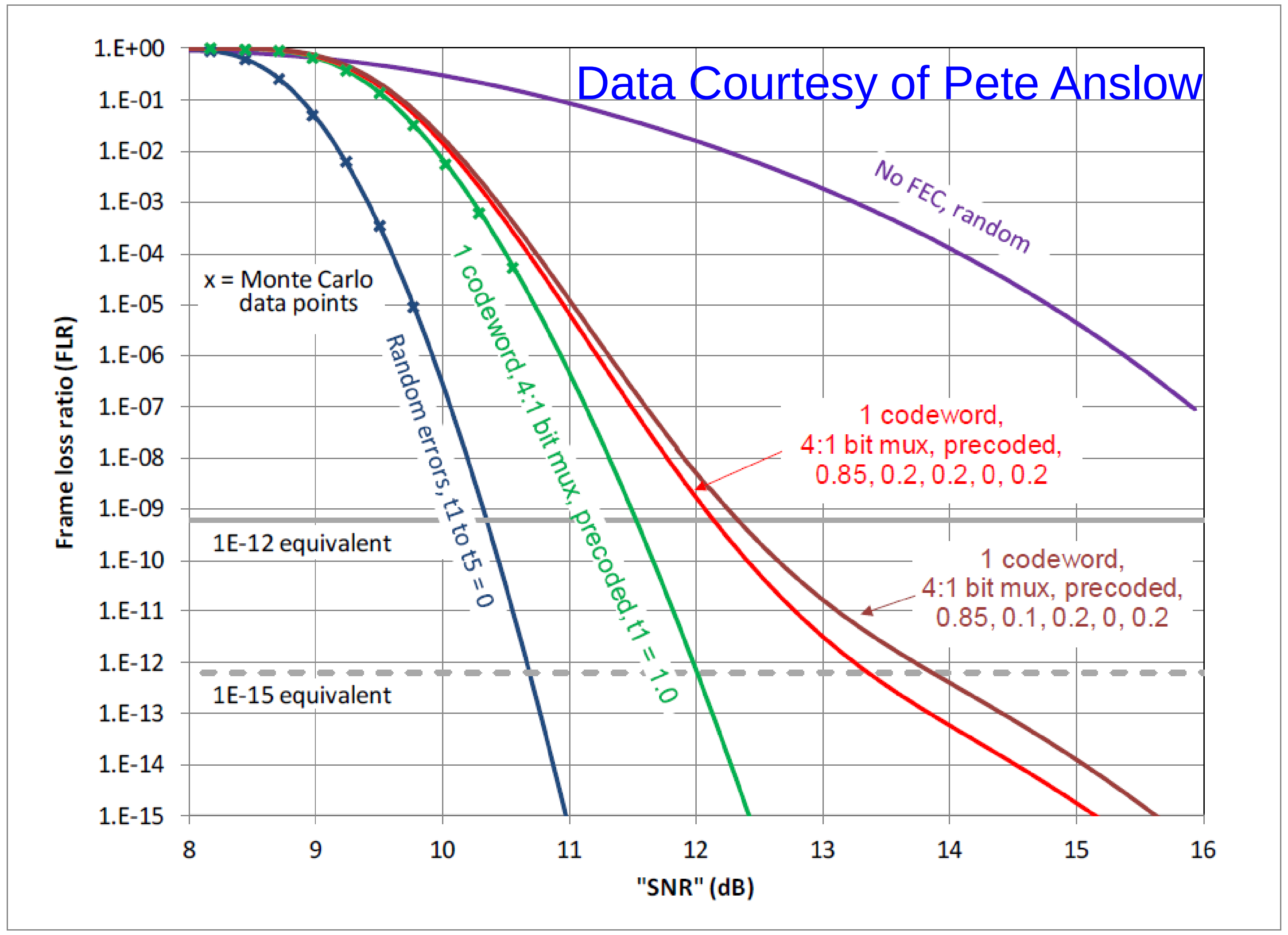
- 2.5% (CDFE and CFFE) are often worse than 2.0% for both DFE and FFE. 2.0% (MDFE and MFFE) are close to 1.5% (DFE and FFE).
- Finer TX resolution are being implemented for 100Gb/s SERDES for better performance and shall be reflected in the standard. For example a 8-bit DAC is implemented for 112G SERDES with less than 1% resolution. [2]
- High resolution can be done by a low power half-size driver [7]. For DAC based architecture, increasing digital tap precision costs very trivial power.
- Finer TX resolution is needed to support C2M.
- Power impact is negligible or very little. This is one of the most efficient ways to help achieve SERDES performance for 100G.

DFE Tap Weight Impact on FEC Performance

100G 5-tap DFE results (0.7, 0, 0.2, 0, 0.2) with precoding



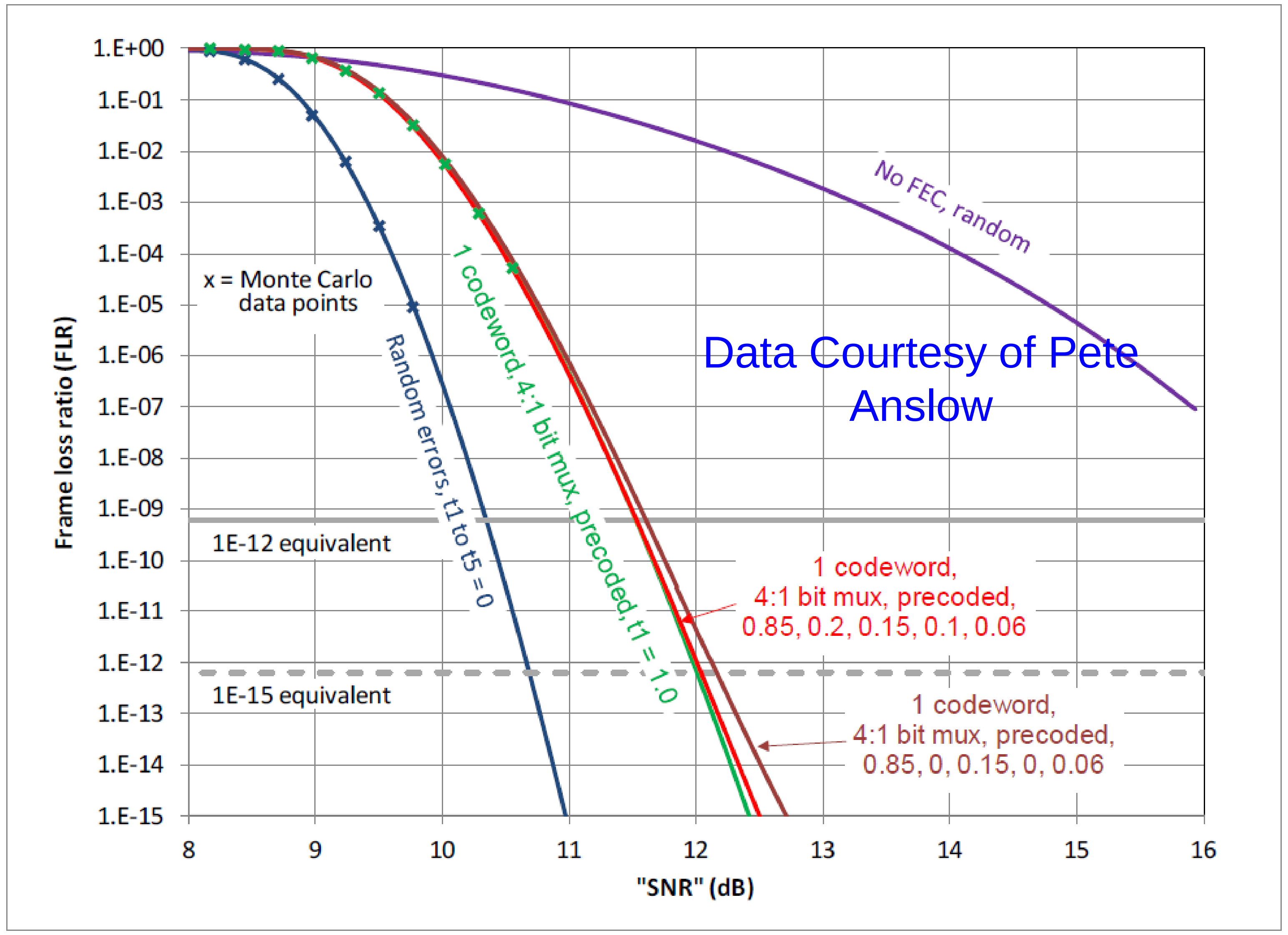
100G with 5-tap DFE (0.85, 0.2 or 0.1, 0.2, 0, 0.2)



- Historically b1max was constrained to limit error propagation [6]. For real implementations, b1, b2, and b3 can be controlled without degrading performance. No need to constrain b1max for a simple reference model.
- With introduction of precoding, simulation shows b1max constraint is not needed.
- [0.85, 0.1/0.2, 0.2, 0, 0.2] has less burst error penalty than [0.7, 0.0, 0.2, 0, 0.2]. Positive b2 alleviates error propagation.

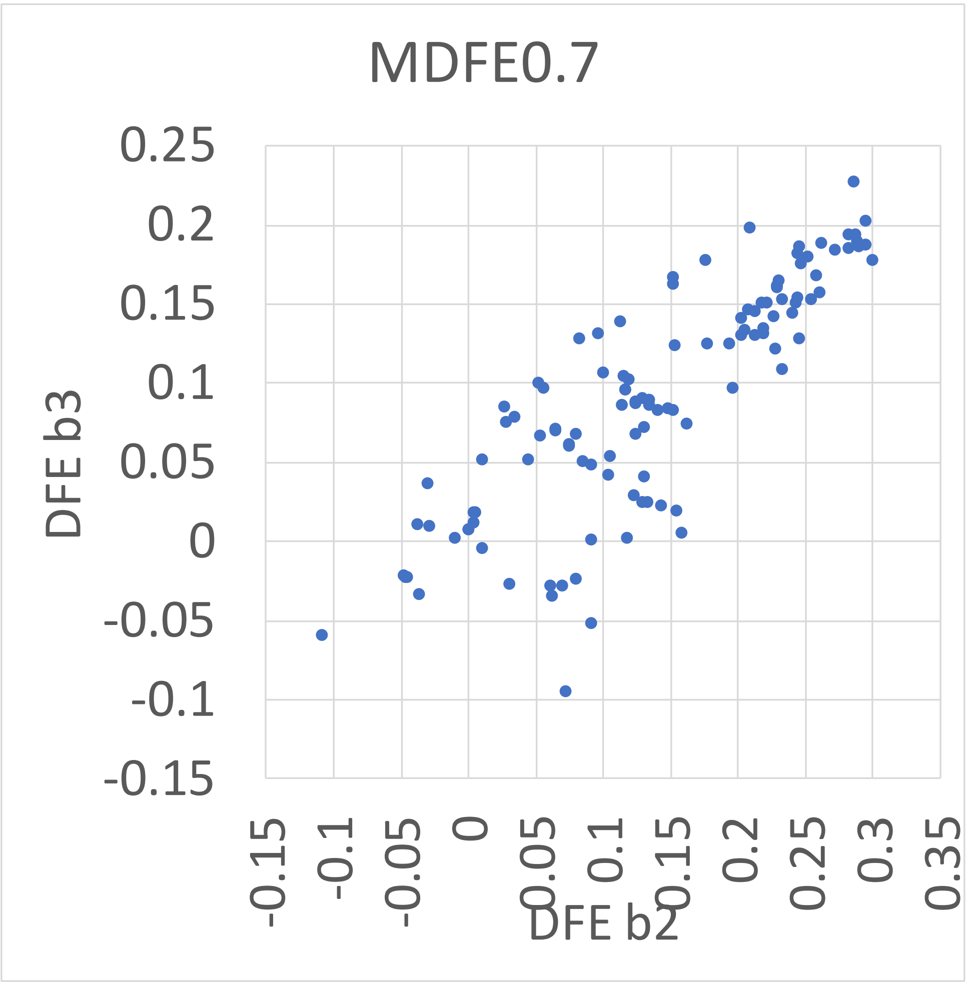
DFE Tap Weight Impact on FEC Performance Cont.

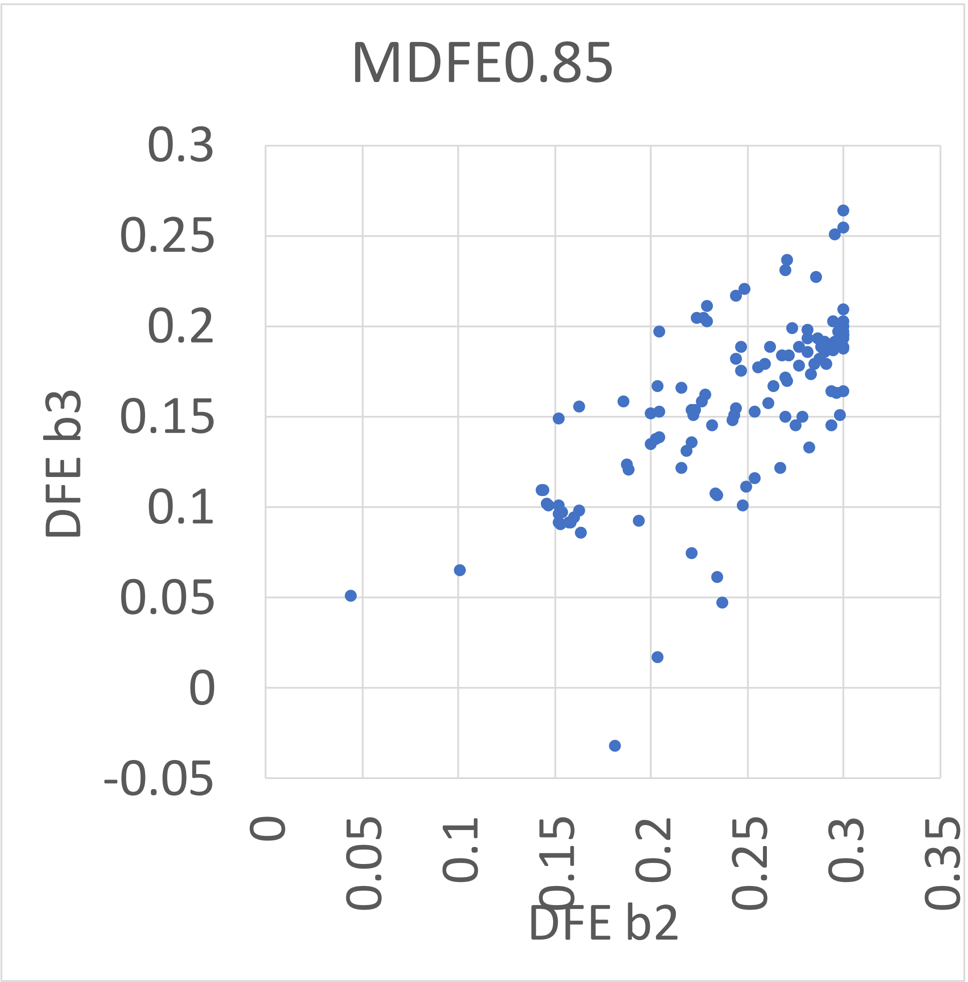
100G with 5-tap DFE (0.85, 0.2 or 0, 0.15, 0.1 or 0, 0.06)

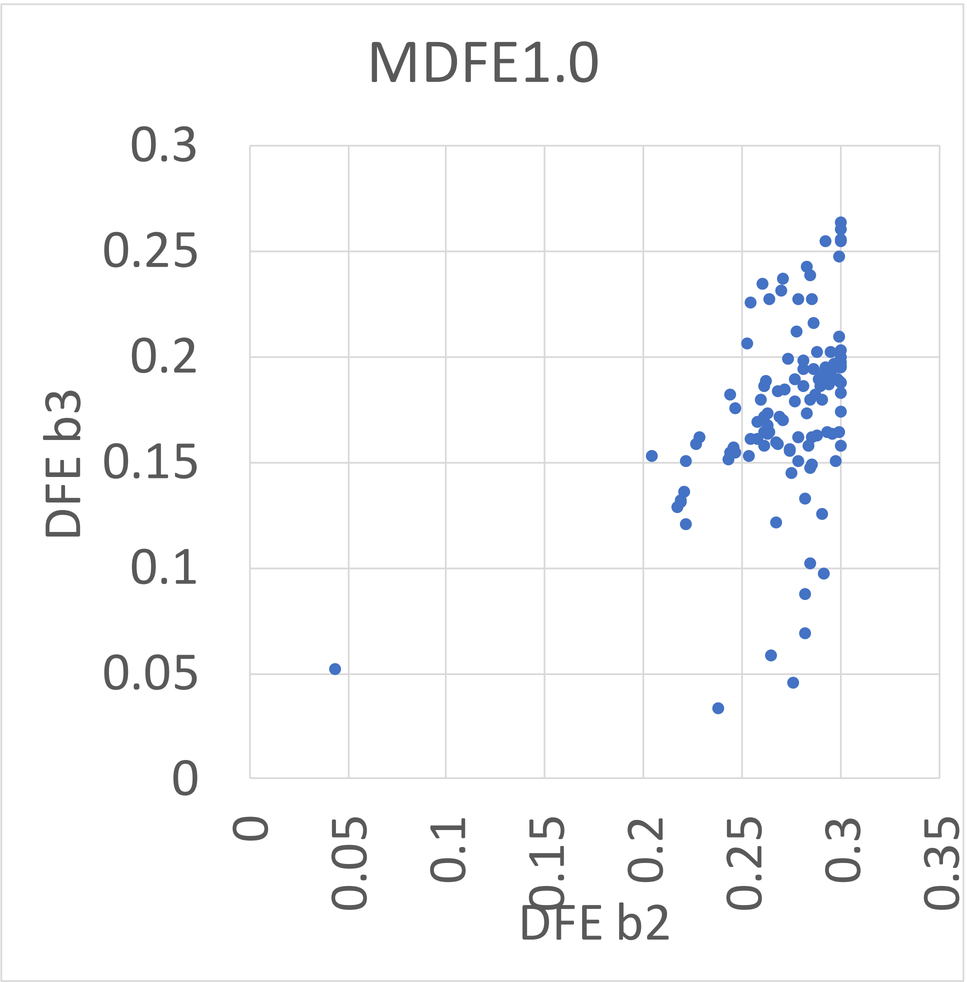


- Precoding is very effective for smaller DFE tail weight or when DFE tail taps cancel each other. DER required by a single-tap or multi-tap DFE becomes similar.
- Precoding is less effective for some burst errors. Burst caused by heavy DFE tail is one of them, while FFE implementations have their own sources.

DFE Tap Weight b2, b3 Statistics







- For b2min is often observed to be more positive with larger b1max.
  - b2 ≥ 0.10 with b1max = 0.85
  - b2 ≥ 0.20 with b1max = 1.0. The low b2 exception is a low loss channel with small b1.

Analysis of Channels Discussed In Ad Hoc Meetings

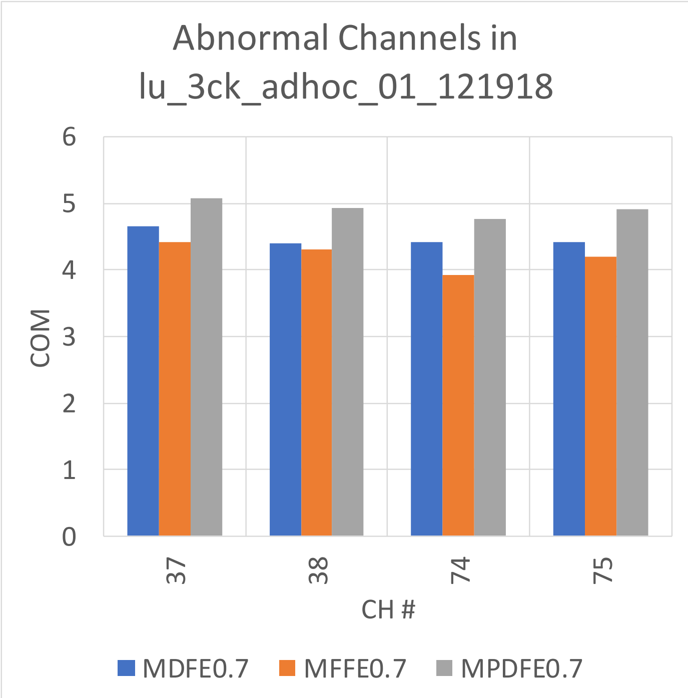
Channel		ID	IL fitted (dB)	ICN (mV)	FOM_ILD (dB)	COM (dB)			
						DFE b_max=0.7 MM-PD	DFE b_max=1.0 MM-PD	FFE-lite b_max=0.7 Modified PD	FFE-heavy b_max=0.7
kareti_3ck_01_1118 backplane	Bch2_7	65	-15.65	1.77	0.47	3.31	2.91	3.50	2.73
	Bch3_14	81	-21.21	1.11	0.45	2.99	3.41	3.40	2.80
kareti_3ck_01_1118 ortho	Och1	109	-15.65	1.12	0.69	3.24	3.27	3.42	1.94
	Och2	110	-19.52	1.12	0.73	3.39	3.39	3.69	2.70

lu_3ck_adhoc_01_121918

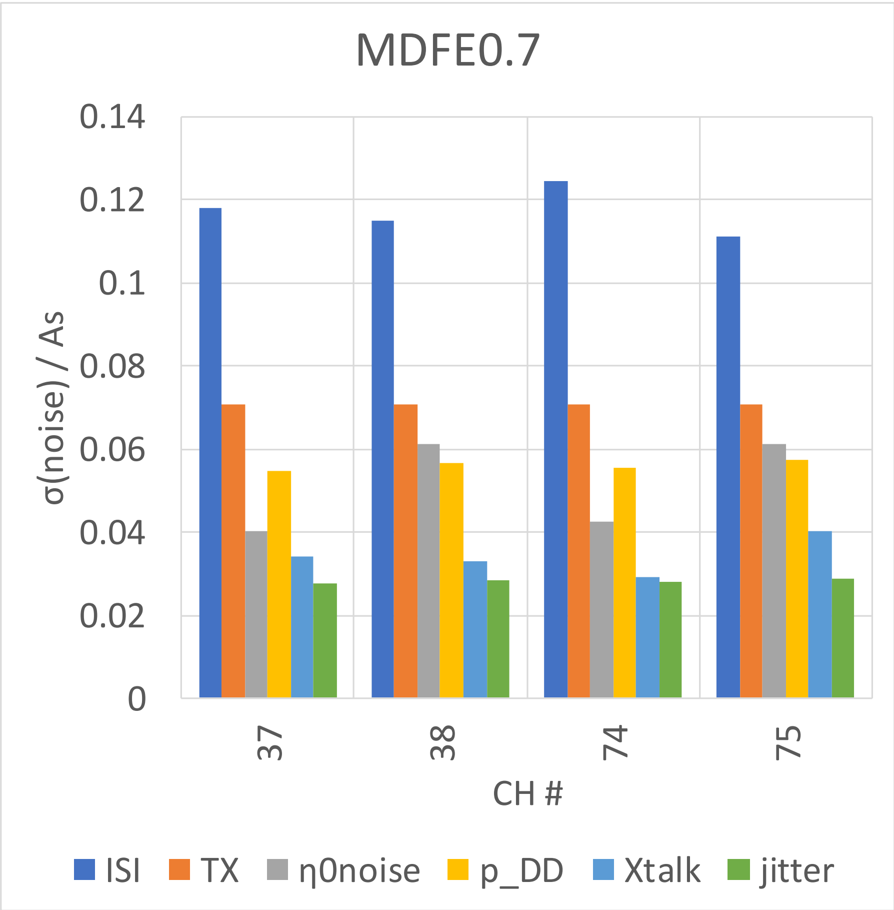
Ch 110 and 81 are not VSR channels, these two channels cannot rule out by other metrics such as ILD.

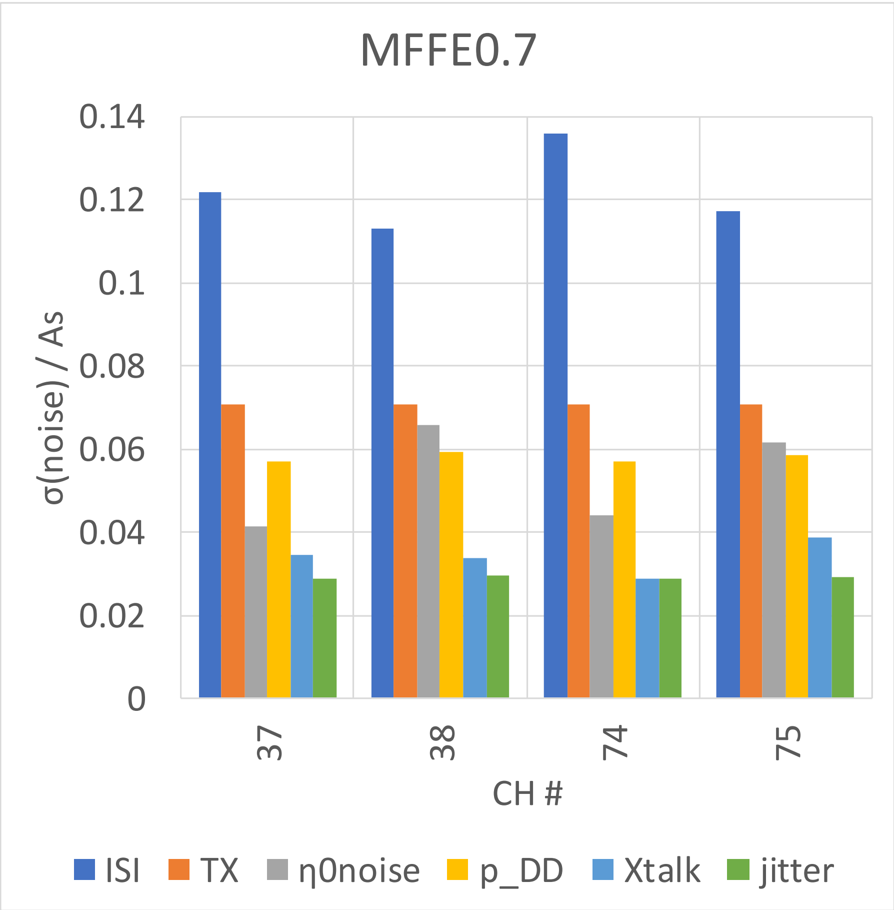
- The above 4 channels were discussed in ad hoc (lu_3ck_adhoc_01_121918) and marked as "abnormal" channels. "Noise amplification was explained as the cause of abnormal". These channels are revisited here for better understanding.
- This simulation based on COM 2.57 shows all these channels have very good COM. COM Difference by DFE and FFE models are less than 0.48dB.

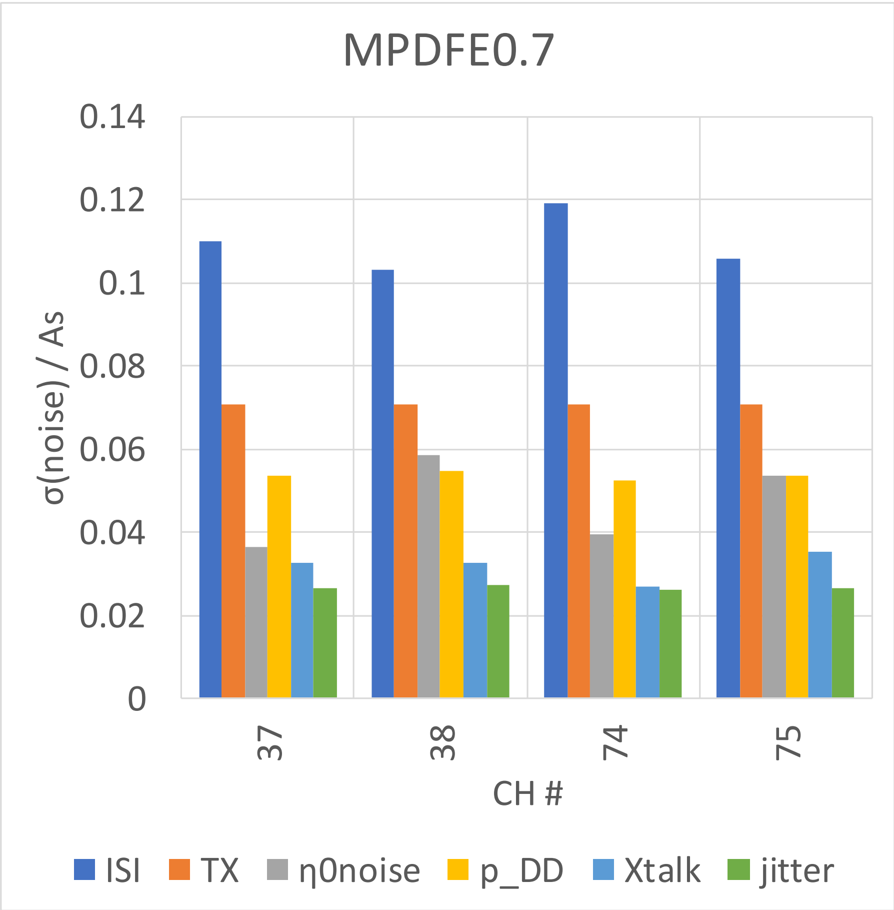
Channel	COM(dB) with MDFE0.7	COM(dB) with MFFE0.7	COM(dB) with MPDFE0.7
Channel #37, Bch2_7	4.66	4.42	5.08
Channel #38, Bch3_14	4.39	4.31	4.93
Channel #74, Och1	4.41	3.93	4.76
Channel #75, Och2	4.41	4.19	4.91

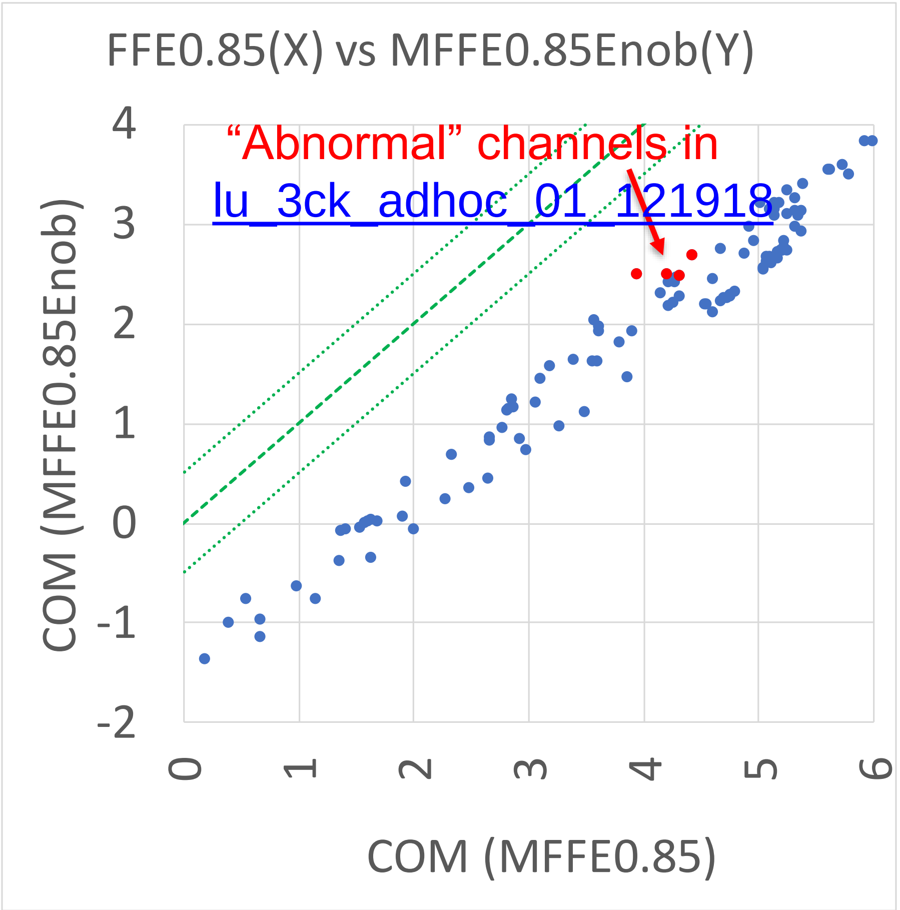


Impairment Breakdown









- These are ISI dominant channels. SNR_noise are very similar for FFE and DFE receivers.
- These channels are relatively easy for a FFE with ENOB considered. These channels should be supported.

Channel #	37	38	74	75
File name	Bch2_7	Bch3_14	Och1	Och2
Lu's Channel ID	65	81	109	110
Fitted IL	15.65dB	21.21dB	15.65dB	19.52dB
FOM_ILD	0.47dB	0.45dB	0.69dB	0.73dB
ERL (Nb=24)	11.34dB	11.84dB	13.28dB	13.97dB
ERL (Nb=1)	10.75dB	11.16dB	11.77dB	13.72dB
ICN	1.78mV	1.12mV	1.14mV	1.14mV

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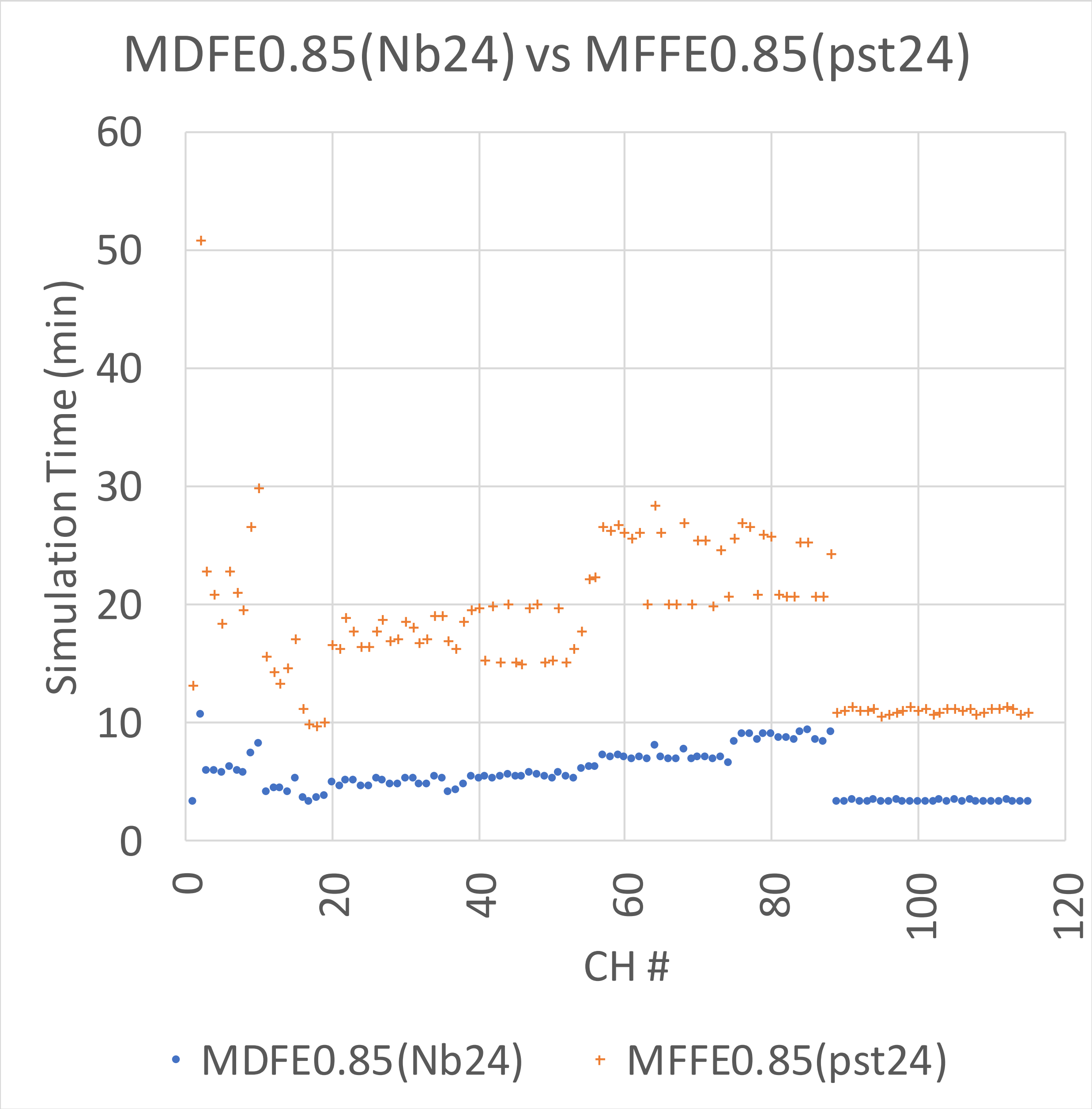
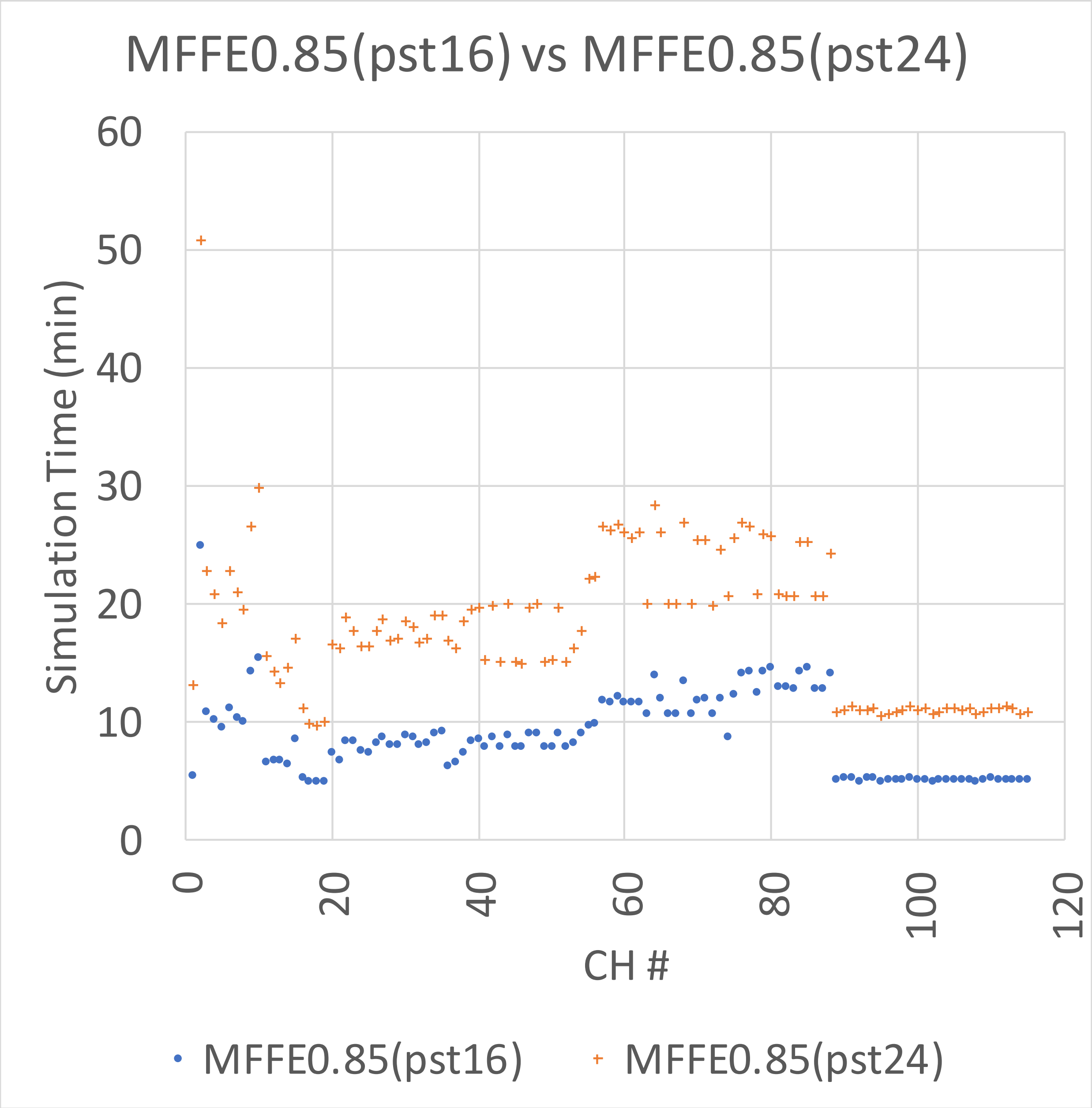
Simulation Time

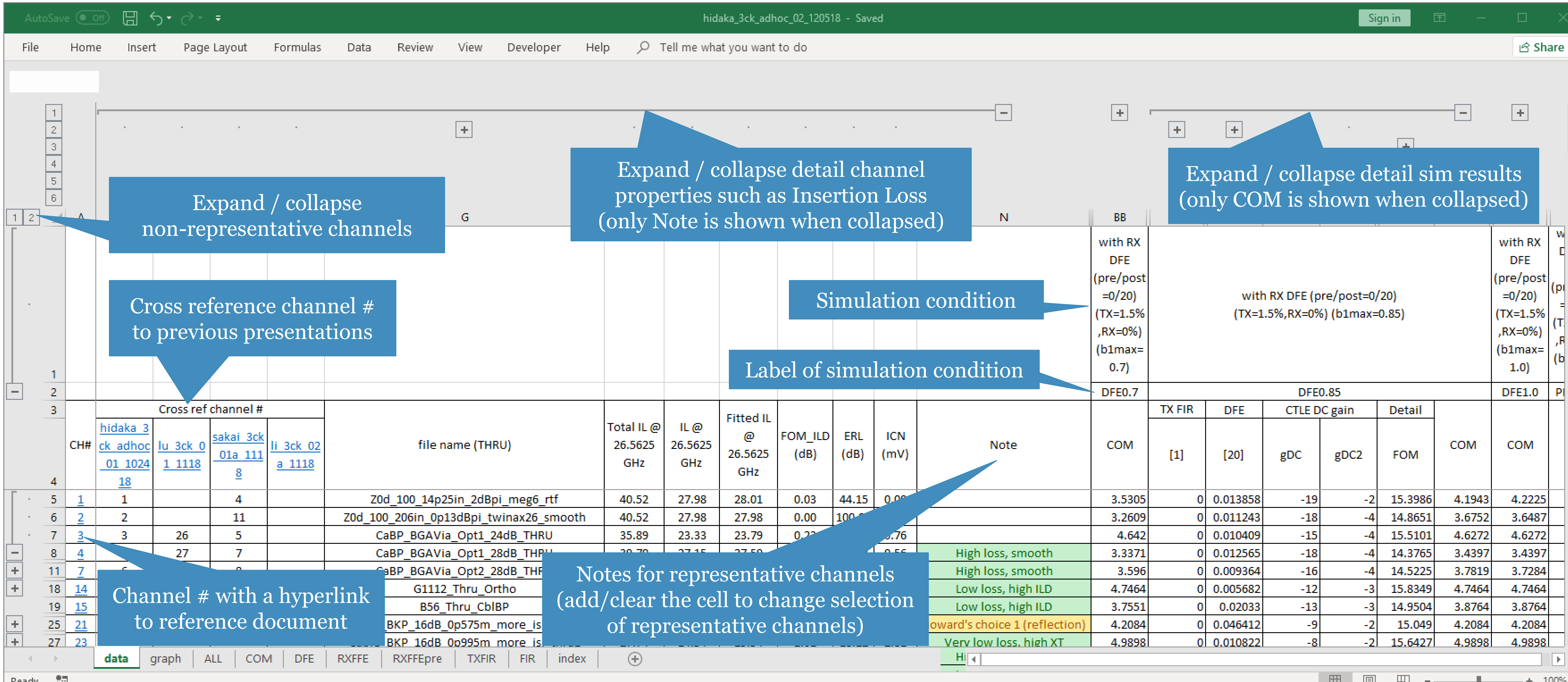




- ➢ FFE execution time is about 4 times of DFE. FFE execution time increases rapidly with the number of taps.
- ➢ One case of FFE with 24 taps took about 50 minutes.

Excel File of Simulation Results

- Excel spread sheet of this contribution is uploaded for future analysis work. It provides information such as TX range, DFE tap weights, COM comparison, etc.



Row	CH#	hidaka_3ck_adhoc_01_1024 18	lu_3ck_01_1118	sakai_3ck_01a_1118	li_3ck_02a_1118	file name (THRU)	Total IL @ 26.5625 GHz	IL @ 26.5625 GHz	Fitted IL @ 26.5625 GHz	FOM_ILD (dB)	ERL (dB)	ICN (mV)	Note	DFE0.7 COM	DFE0.85 TX FIR [1]	DFE0.85 DFE [20]	DFE0.85 CTLE DC gain gDC	DFE0.85 CTLE DC gain gDC2	DFE0.85 Detail FOM	DFE0.85 COM	DFE1.0 COM
5	1	1		4		Z0d_100_14p25in_2dBpi_meg6_rtf	40.52	27.98	28.01	0.03	44.15	[illegible]		3.5305	0	0.013858	-19	-2	15.3986	4.1943	4.2225
6	2	2		11		Z0d_100_206in_0p13dBpi_twinax26_smooth	40.52	27.98	27.98	0.00	[illegible]	[illegible]		3.2609	0	0.011243	-18	-4	14.8651	3.6752	3.6487
7	3	3	26	5		CaBP_BGAVia_Opt1_24dB_THRU	35.89	23.33	23.79	[illegible]	[illegible]	[illegible]		4.642	0	0.010409	-15	-4	15.5101	4.6272	4.6272
8	4		27	7		CaBP_BGAVia_Opt1_28dB_THR[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	High loss, smooth	3.3371	0	0.012565	-18	-4	14.3765	3.4397	3.4397
11	7	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]aBP_BGAVia_Opt2_28dB_THF[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	High loss, smooth	3.596	0	0.009364	-16	-4	14.5225	3.7819	3.7284
18	14	[illegible]	[illegible]	[illegible]	[illegible]	G1112_Thru_Ortho	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Low loss, high ILD	4.7464	0	0.005682	-12	-3	15.8349	4.7464	4.7464
19	15	[illegible]	[illegible]	[illegible]	[illegible]	B56_Thru_CblBP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Low loss, high ILD	3.7551	0	0.02033	-13	-3	14.9504	3.8764	3.8764
25	21	[illegible]	[illegible]	[illegible]	[illegible]	BKP_16dB_0p575m_more_is[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]oward's choice 1 (reflection)	4.2084	0	0.046412	-9	-2	15.049	4.2084	4.2084
27	23	[illegible]	[illegible]	[illegible]	[illegible]	BKP_16dB_0p995m_more_is[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Very low loss, high XT	4.9898	0	0.010822	-8	-2	15.6427	4.9898	4.9898

Conclusions

- 2% or finer TX FIR resolution is recommended to reflect real designs and achieve better performance at very low cost.

- DFE model is about 4x faster than FFE model. FFE model execution time increases rapidly with the number of FFE taps.

- COM simulation shows DFE and FFE model tracks each other's performance. A receiver with DFE + FFE precursor (PDFE) is an ideal analog SERDES architecture. But as a reference model it passes channels that cannot be supported by typical DFE and FFE based implementations.
  - With 5.2 bit ENOB, FFE model performance is significantly degraded.
  - Without proper noise assumption, FFE model behavior is not realistic.

- For DFE model, b1max and COM threshold can be easily tuned to match performance of DFE and FFE based implementations. For example, b1max=0.85 and COM threshold is about 3dB, or b1max=0.7, and COM threshold is about 2.5dB.

References

[1] P. Sun, Y. Hidaka, “Comparison of KR/CR Reference Receivers,” IEEE 802.3ck Task Force Ad Hoc, December 5, 2018.

[2] C. Menolfi, et al., “A 112Gb/s 2.6pJ/b 8-Tap FFE PAM-4 SST TX in 14nm CMOS”, ISSCC, pp. 103-104, Feb. 2018.

[3] Y. Hidaka, P. Sun, “COM Simulation for 100G KR/CR Channels, update ,” IEEE 802.3ck Task Force Ad Hoc, December 12, 2018.

[4] P. Sun, Y. Hidaka, “What is important for a Reference Receiver,” IEEE 802.3ck Task Force Meeting, January 2019.

[5] P. Sun, “100G SERDES Power Study,” IEEE 802.3ck Task Force Meeting, September 2018.

[6] P. Sun, et al., “Achieving BER/FLR targets with clause 74 FEC,” IEEE 802.3by Task Force Ad Hoc, February 2015.

[7] L. Wang, et al., “A 64Gb/s PAM-4 Transceiver Utilizing an Adaptive Threshold ADC in 16nm FinFET”, ISSCC, pp. 110-111, Feb. 2018.

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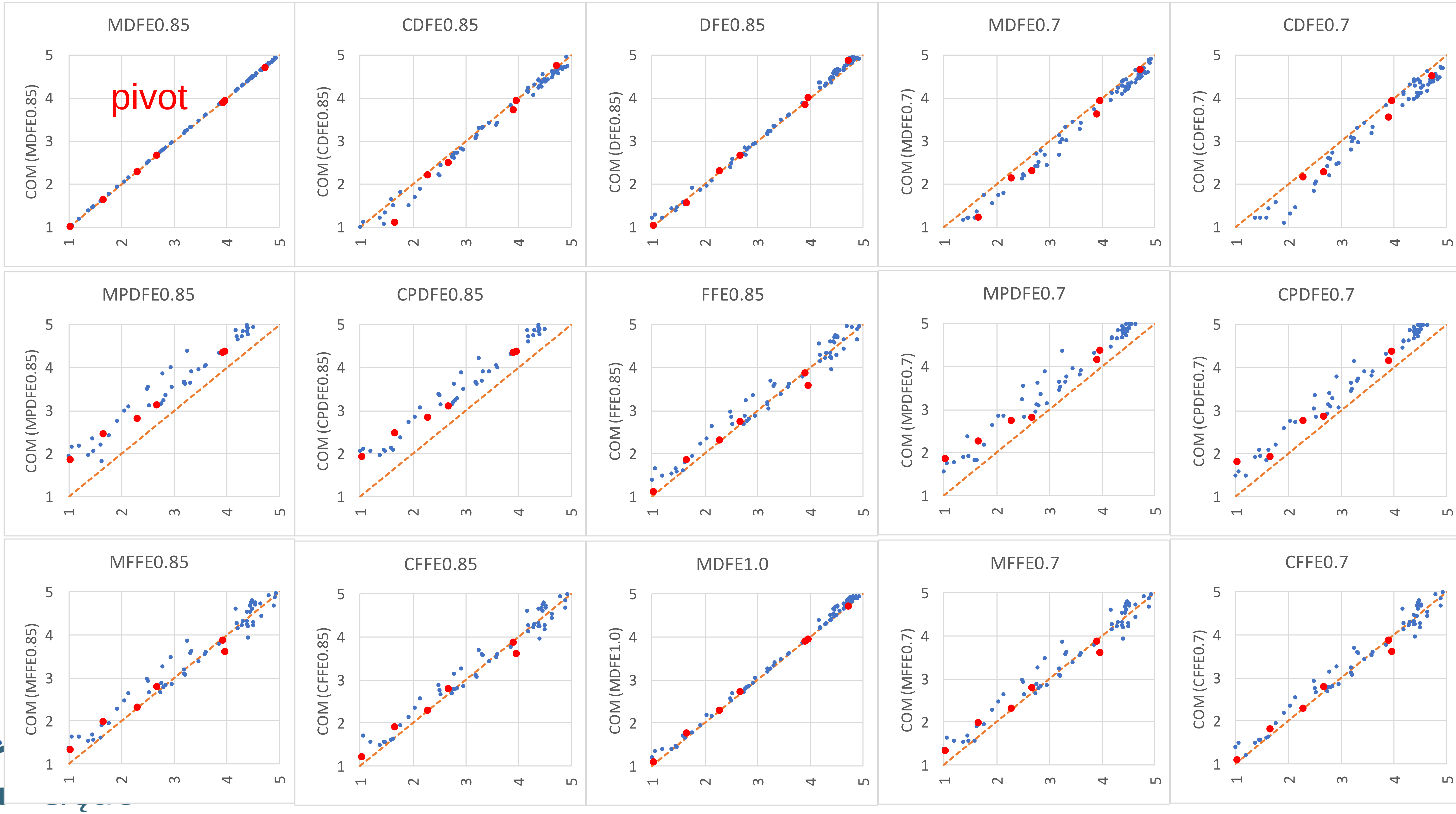
Backup Slides

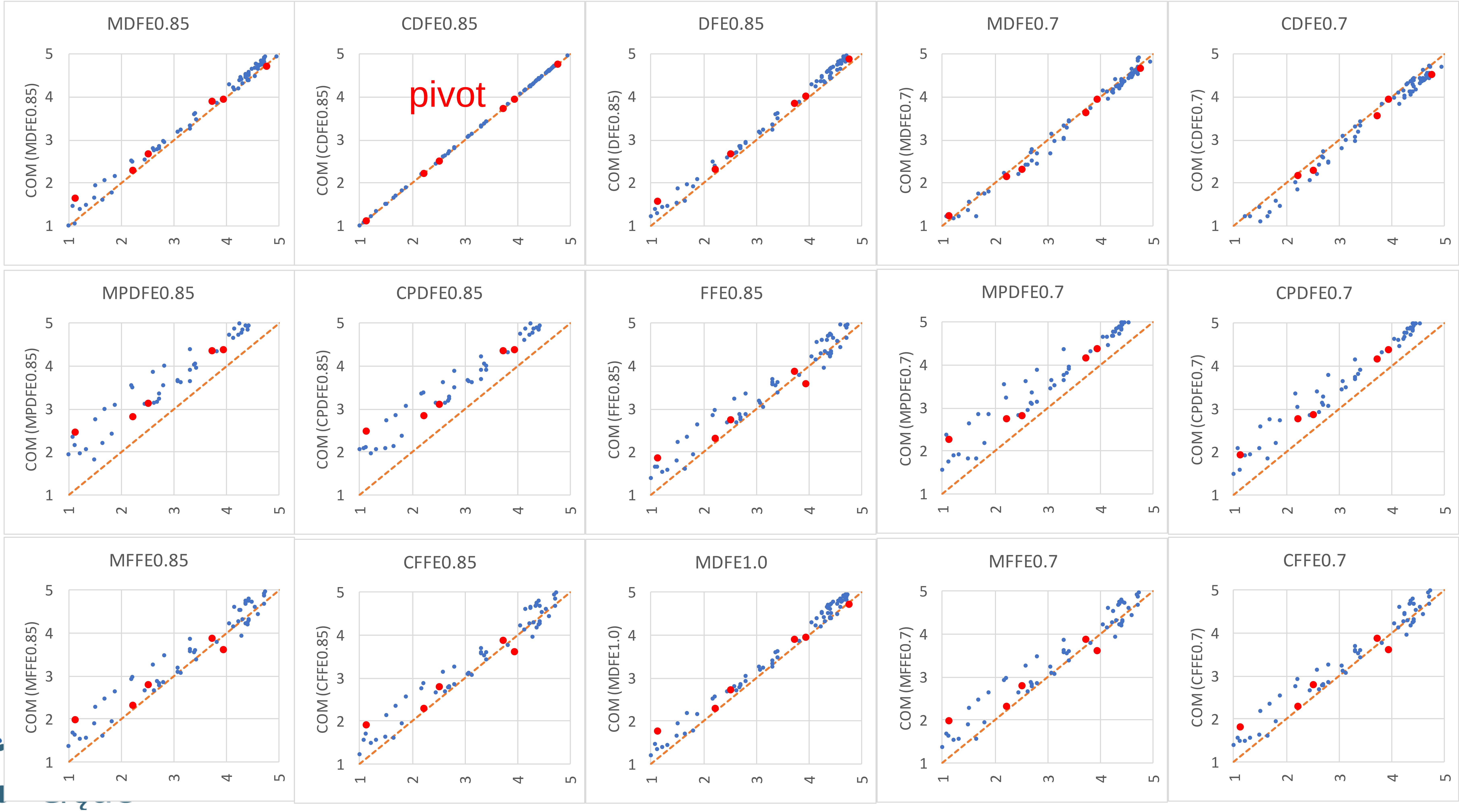
COM Values for Marked Channels

Group : CH#	RM2 : CH7	HH2 : CH21	HH2 : CH33	UK1 : CH36	UK1 : CH46	UK2 : CH68	UK3 : CH80	UK3 : CH81
Description	CaBP_BGAVia _Opt2_28dB	16dB 575mm high ISI	28dB 575mm high ISI	Bch1_3p5	Bch2_a7p5_7	CAch3_b2	OAch4	Och4
MDFE1.0	4.7314	5.9342	2.7335	3.9565	1.7662	3.9172	2.2928	1.0906
MDFE0.85	4.7314	5.9342	2.6743	3.9565	1.6604	3.9172	2.2928	1.0220
CDFE0.85	4.7614	5.8486	2.5220	3.9424	1.1301	3.7284	2.2252	0.43639
MDFE0.7	4.6717	5.9342	2.3268	3.9565	1.2496	3.6355	2.1581	0.72424
CDFE0.7	4.5389	5.8486	2.2928	3.9424	0.72424	3.5697	2.1693	0.41814
MFFE0.85	5.0053	5.6134	2.8052	3.6139	1.9927	3.8900	2.3268	1.3505
CFFE0.85	5.0518	5.6300	2.7932	3.6223	1.9057	3.8764	2.2928	1.2196
MFFE0.7	5.0053	5.6134	2.8052	3.6139	1.9927	3.8900	2.3268	1.3505
CFFE0.7	5.0518	5.6300	2.7932	3.6223	1.8196	3.8764	2.2928	1.1103
MPDFE0.85	5.3521	6.4321	3.1478	4.3885	2.4641	4.3505	2.8293	1.8625
CPDFE0.85	5.3844	6.3761	3.1229	4.3771	2.4872	4.3505	2.8413	1.9382
MPDFE0.7	5.2721	6.4321	2.8293	4.3885	2.2815	4.1802	2.7454	1.8625
CPDFE0.7	5.3040	6.3761	2.8654	4.3771	1.9491	4.1802	2.7693	1.8089
MDFE0.85(Nb16)	2.9309	2.3381	1.1797	2.9096	0.62101	2.7693	1.1897	0.21991
CDFE0.85(Nb16)	3.9172	2.4296	1.1202	2.8843	-0.0086815	2.6624	1.1499	-0.14642
MFFE0.85(pst16)	4.3077	2.2477	1.1698	2.5627	0.73369	2.6271	1.1202	0.34553
CFFE0.85(pst16)	4.2792	2.2815	1.1797	2.5649	0.64904	2.6271	1.1301	0.24667

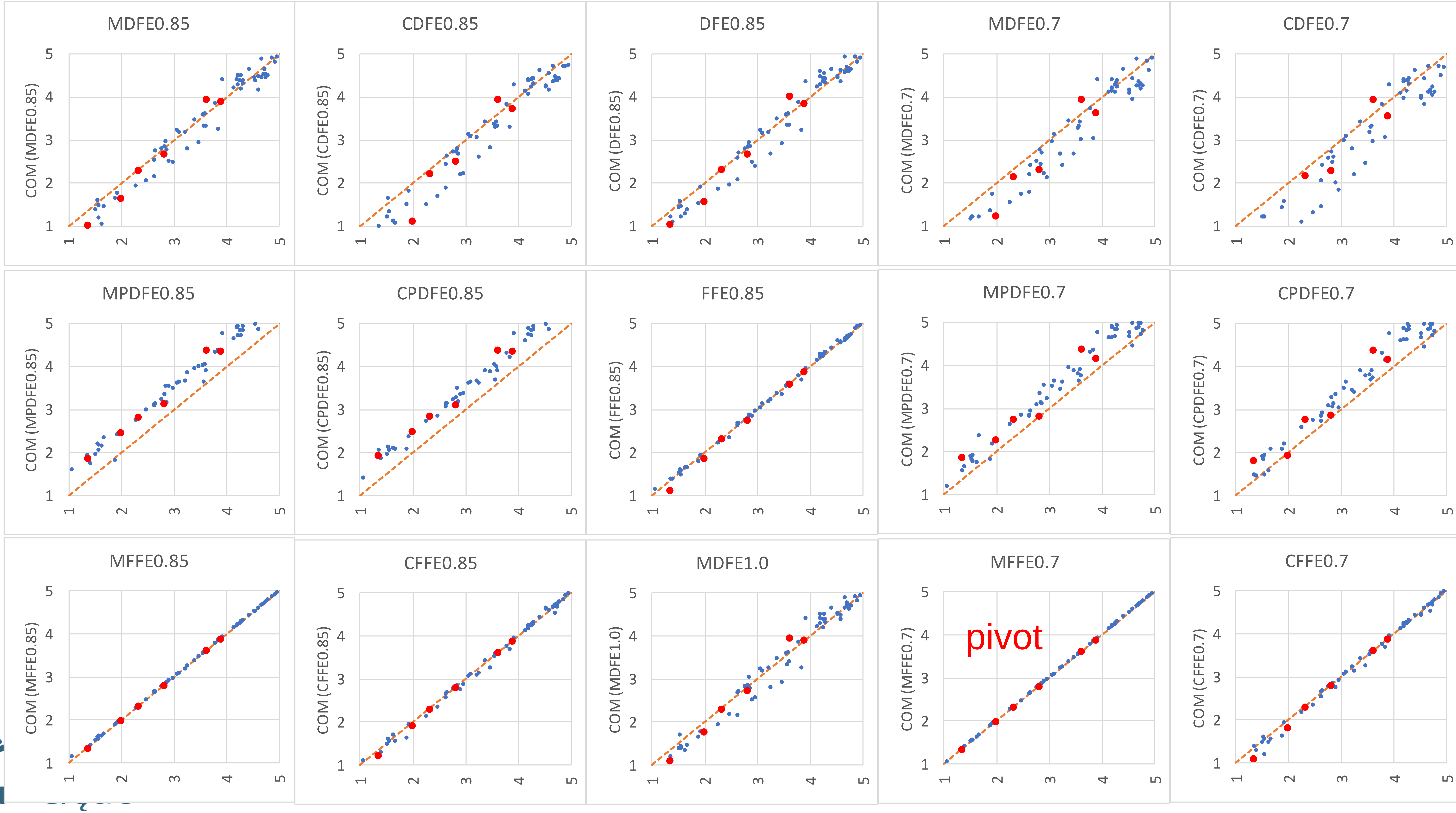
Comparison with COM (MDFE0.85) as X axis



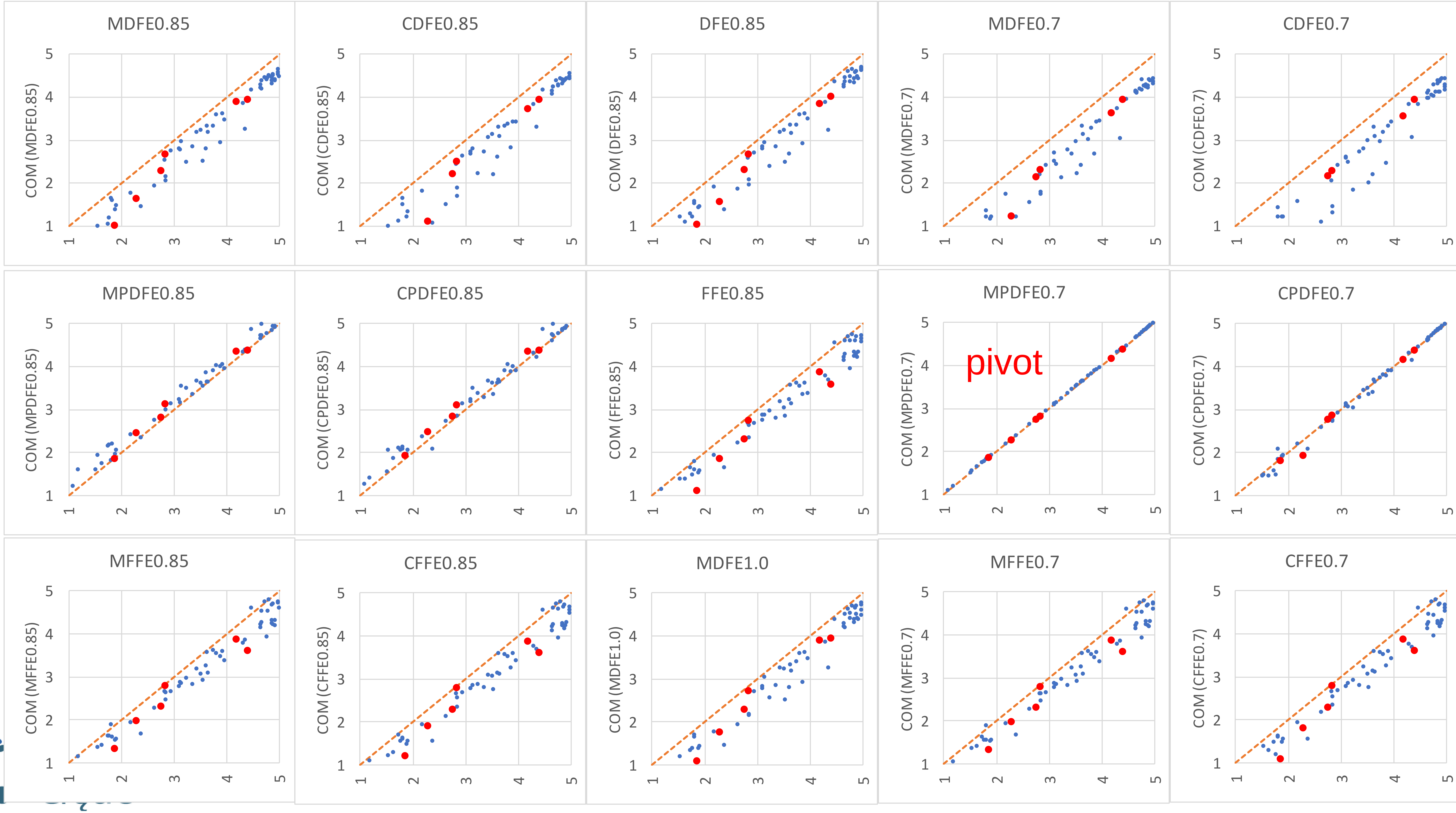
Comparison with COM (CDFE0.85) as X axis



Comparison with COM (MFFE0.7) as X axis



Comparison with COM (MPDFE0.7) as X axis



Comparison with COM (MPDFE0.85) as X axis