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Correlating COM's Excessive Capacitance C_Die Value to Measurements

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Liav Ben Artsi

Conclusions and Summary

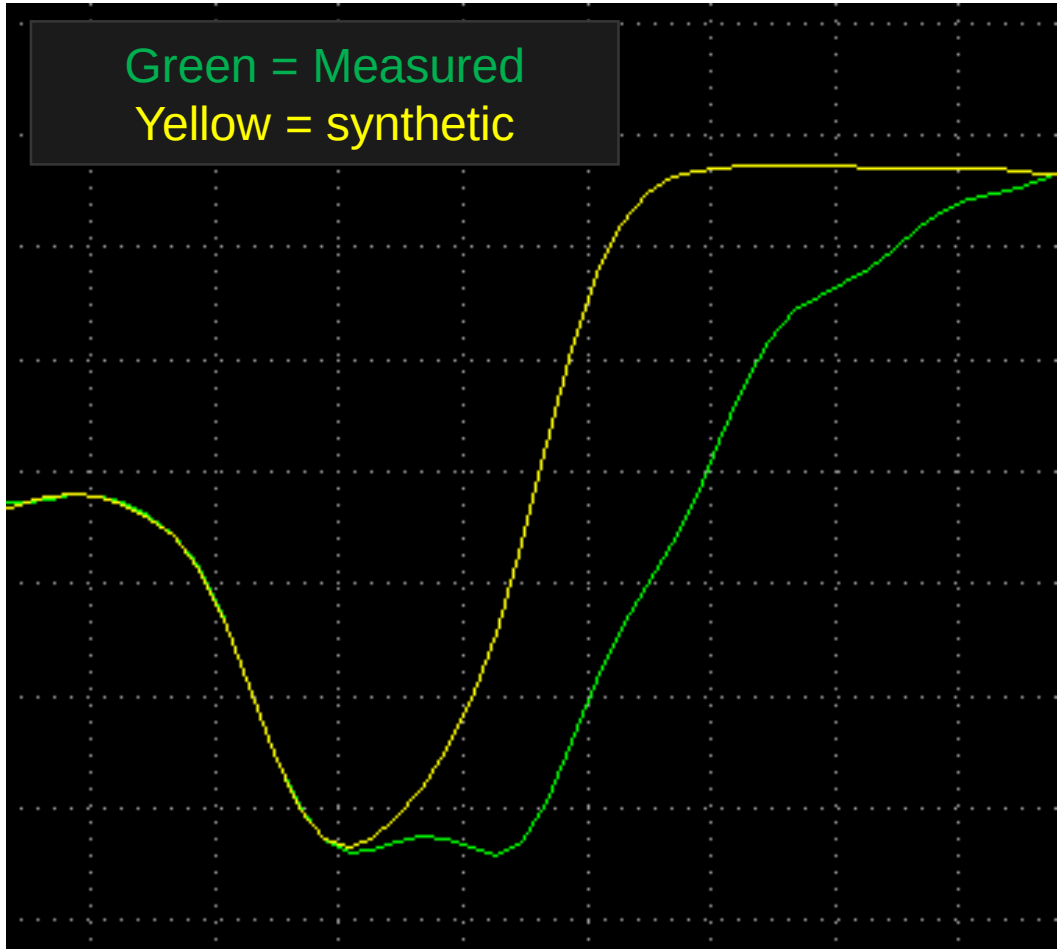
- Die area shows behavior which is not correlated to a pure capacitor, however, the excessive capacitance was correlated in simulation
- Tx shows slightly higher excessive capacitance than Rx
- The excessive capacitance includes both one related to package bump pad (was formerly correlated to ~10fF) as well as to die related circuitry
- Simulation results support high correlation of measured SDD11 die area capacitance to a value of **100fF for Rx and 115fF for Tx ➔ Recommend to use these values in COM**

Measurement and Simulation

- Package was measured for two port (single ended) Sdd11 from both Tx and Rx ball sides
- A TDR simulation was run on return loss results showing a drop in impedance at the die area – Can be correlated to an excessive capacitance
- A synthetic model was used to run TDR and compare the results to TDR on a measured device
- The width of the drop is different than the one correlated to pure capacitance
- The depth and angle follow a value of 115fF for Tx and 100fF for Rx

Simulation Results Compared to Measurements

Tx – 115fF



Rx – 100fF

Thank you!

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Backup – Simulation Method

- Measure both Rx and Tx lanes of the device for two channel Sdd11
- Provide a package model that correlates to the measured device's measured lanes
- Run a TDR Simulation on both measured as well as symthetic models
- Correlate the impedance, loss and delay of the package model to the measured
- Sweep C value until a proper "C_die" value is retrieved