PCS, FEC and PMA Sublayer Baseline Proposal

IEEE P802.3ck

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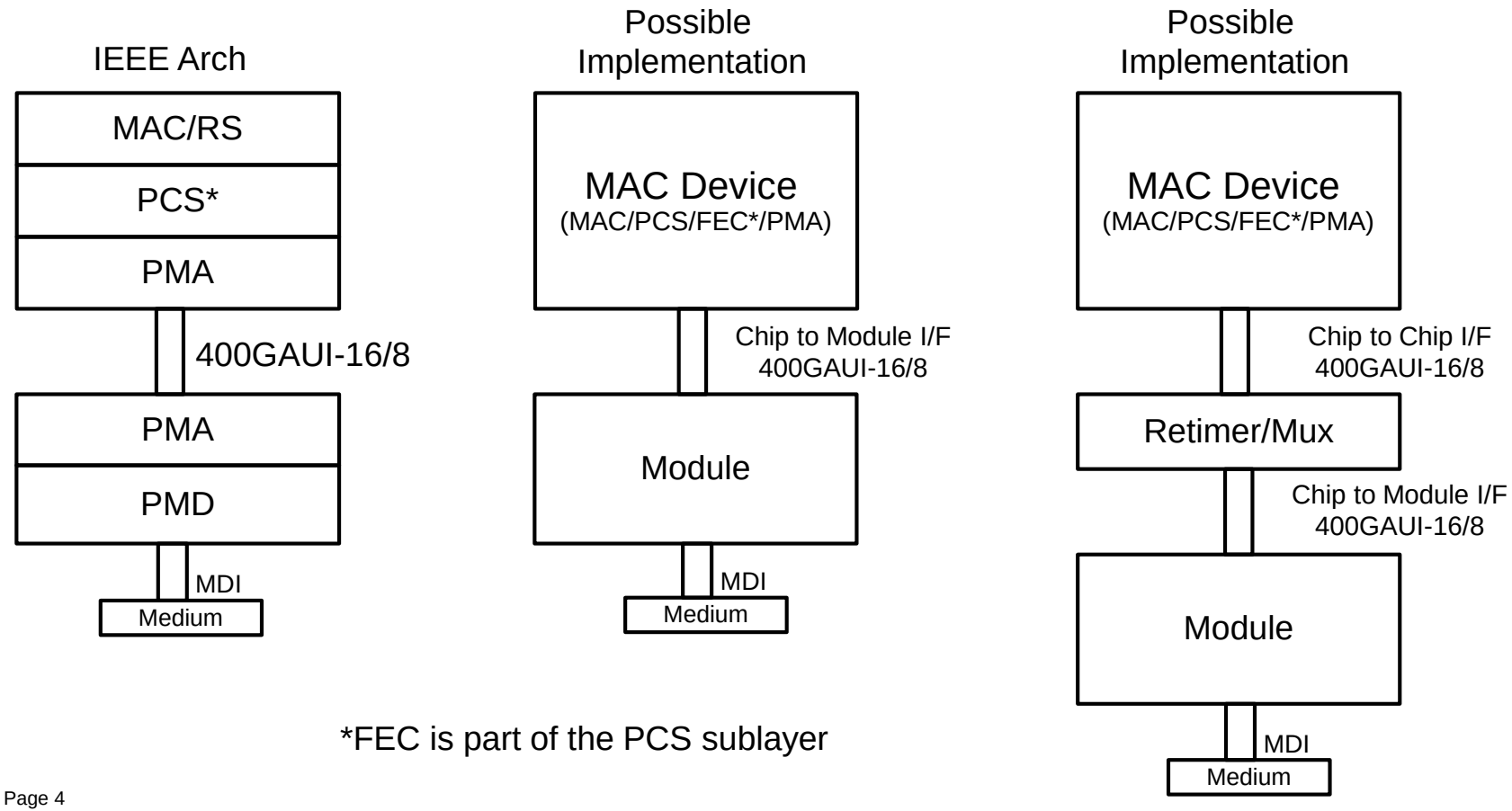
Introduction

- This describes a possible PCS/FEC/PMA baseline proposal for the various Ethernet speeds covered by the 802.3ck task force
- It proposes to reuse existing PCS/FEC/PMA sublayers that have been defined in 802.3bs and 802.3cd
- It leaves the decision for 100GBASE-KR1/CR1 for the future
  - Discussions are ongoing if interleaving is necessary or not for these channels

802.3bs Architecture – 200GbE and 400GbE

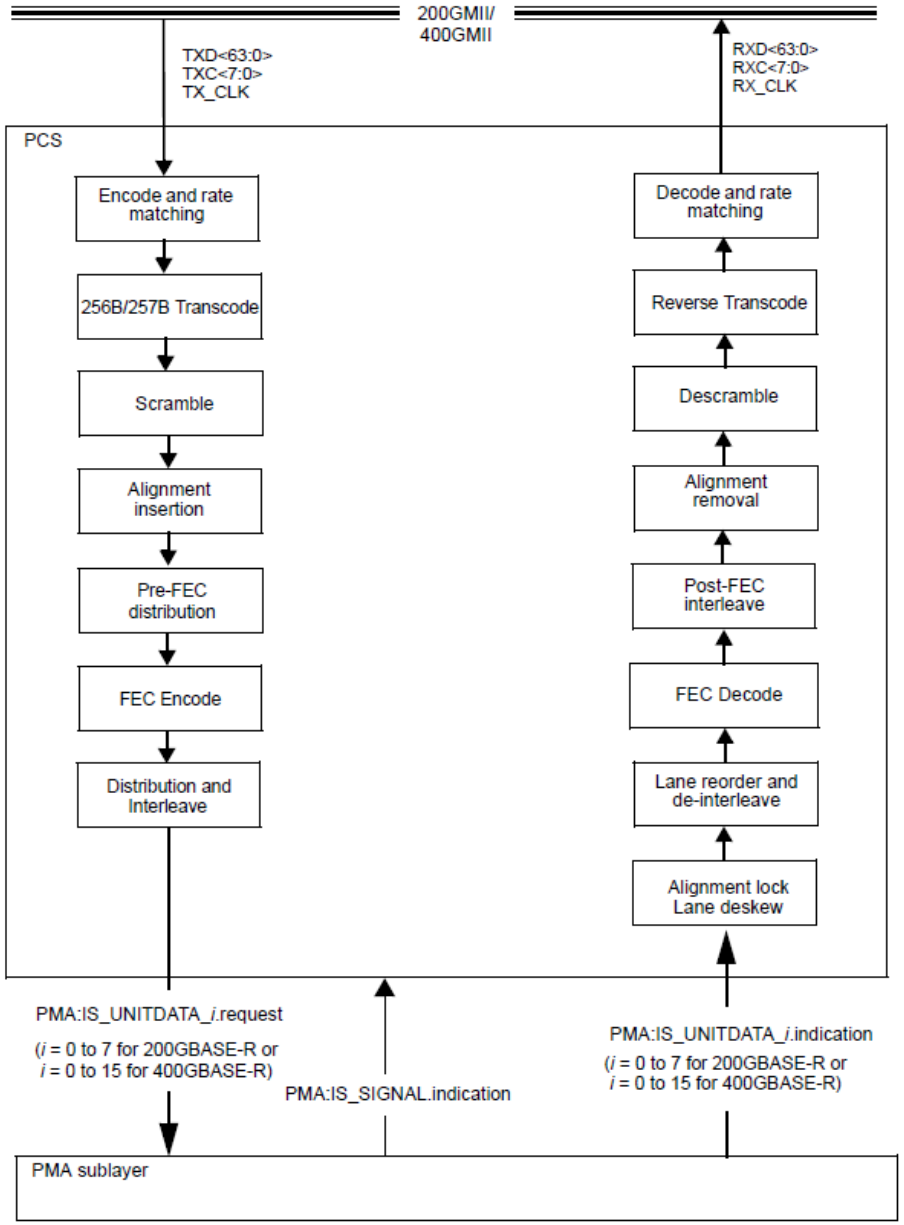
- Adopted architecture and possible implementations are shown below for 400GbE
  - 200GbE is identical except for # lanes and MAC rate
- FEC is part of the PCS sublayer utilizing the RS(544,514) aka “KP4” FEC code.
- An extender sublayer is also defined



*FEC is part of the PCS sublayer

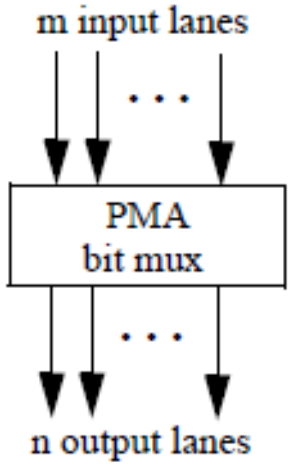
802.3bs PCS

- PCS processing flow is shown in the figure
- The PCS distributes data to 16 PCS lanes for 400GbE and 8 PCS lane for 200GbE
- Pre-FEC distribution plays the data out to two FEC codewords



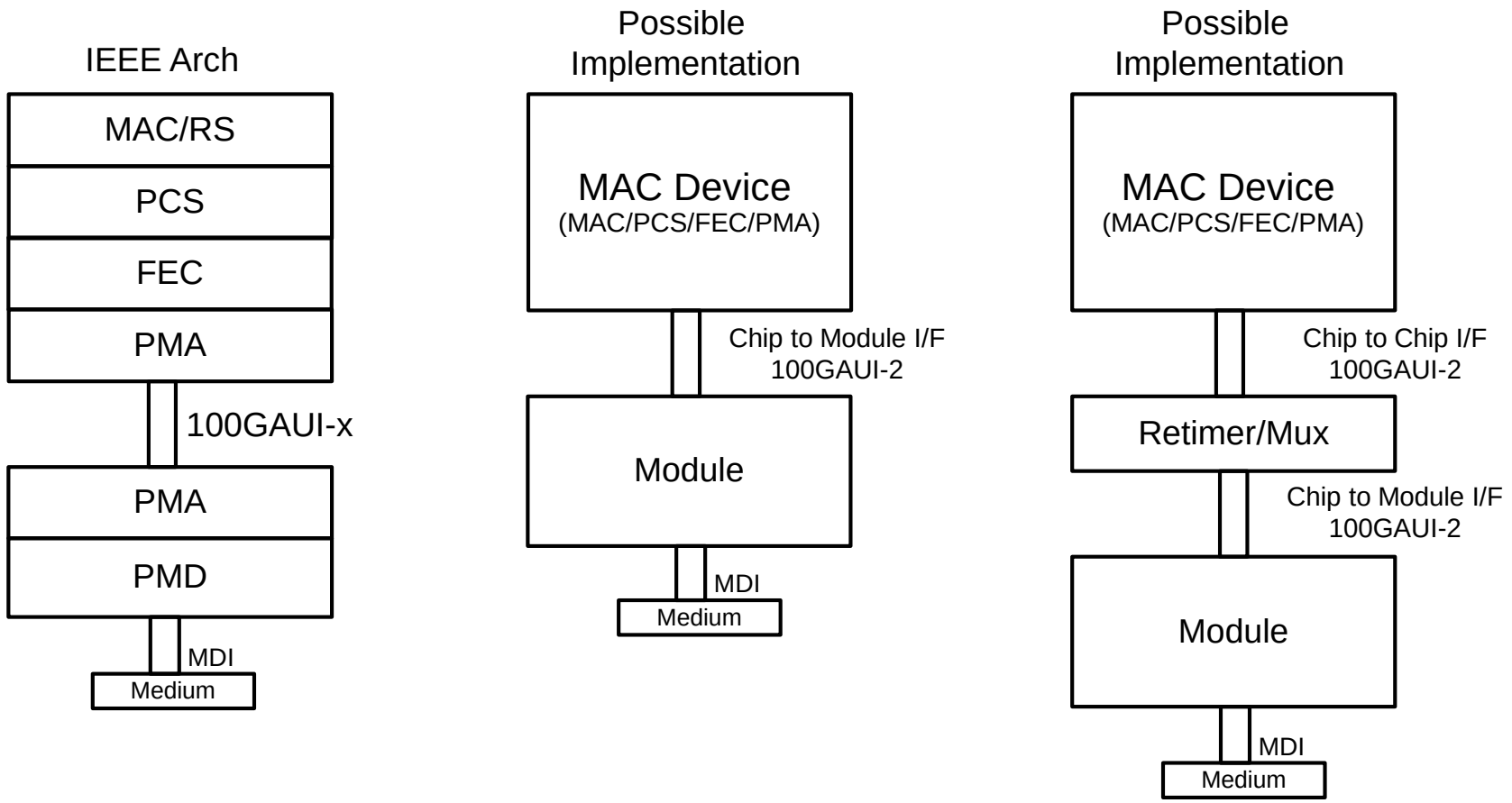
802.3bs PMA

- From a muxing point of view, the PMA is simple, m input lanes are bit muxed to n output lanes
- Bit muxing is blind, lanes can move around, the RX PCS sorts things out
- Clock content and baseline wander simulations have been performed for 1:1, 2:1 and 4:1 muxing scenarios
- Precoding supported on KR/CR PMDs
  - Added by 802.3cd for 200G-KR4/CR4
  - Must implement in TX, optional to implement in RX and the feature is optional to enable



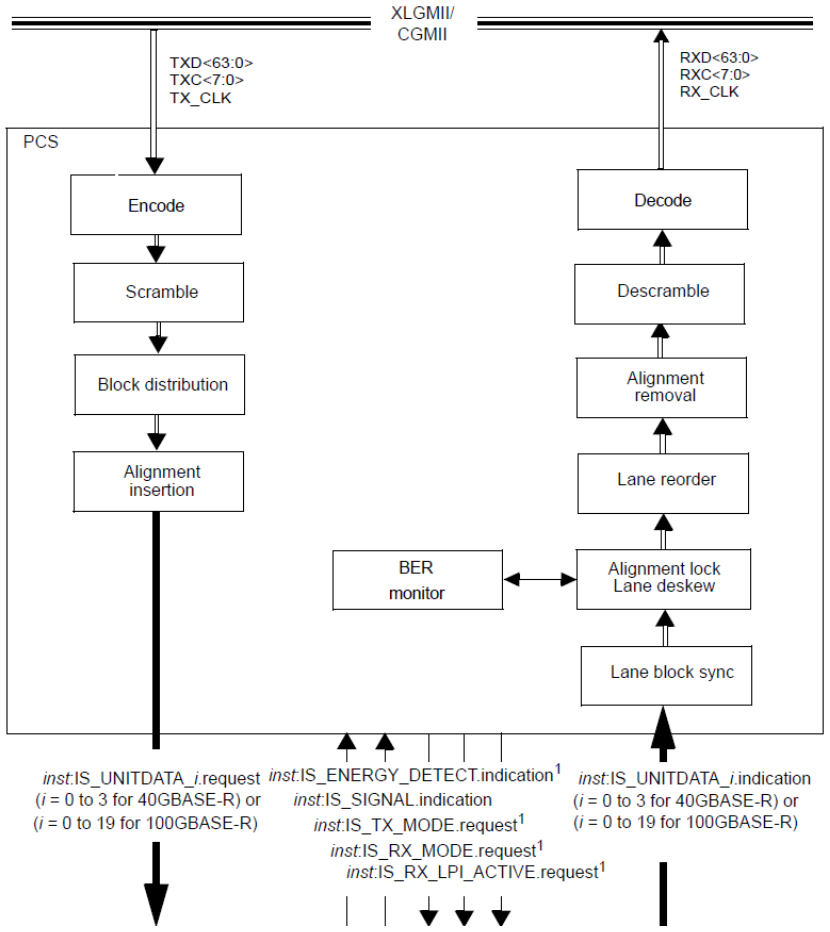
802.3cd Architecture – 100GbE

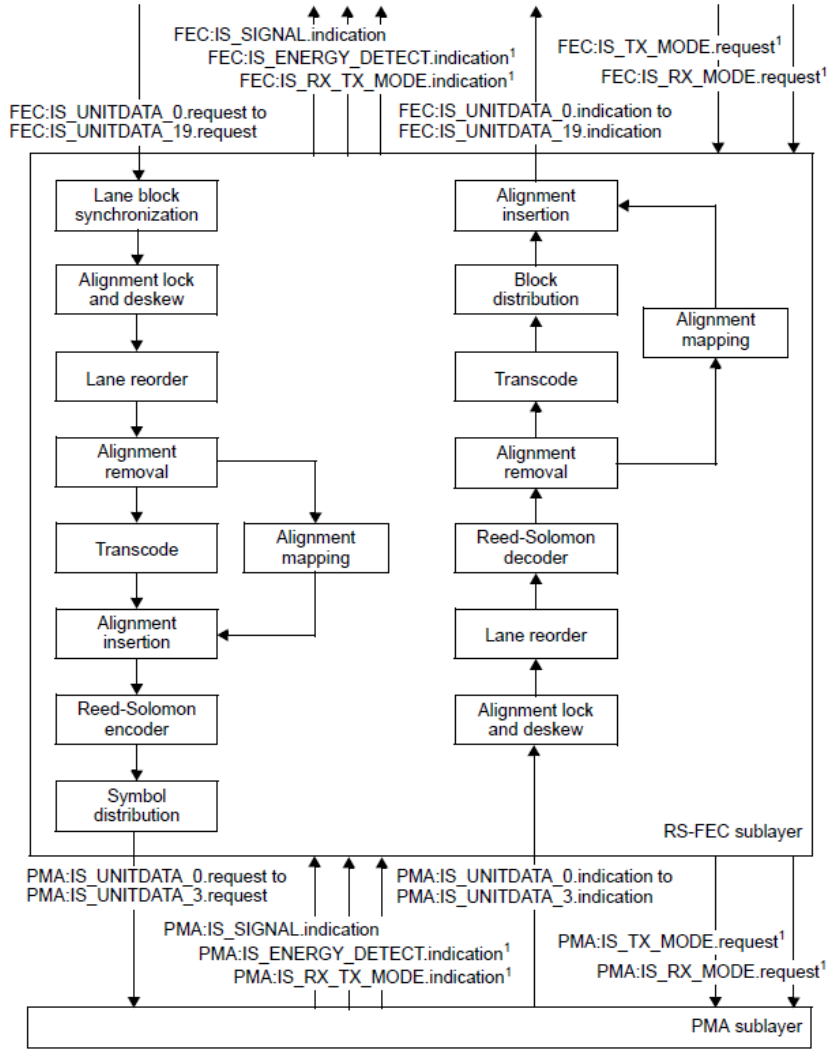
- Adopted architecture and possible implementations are shown below for 100GbE
- FEC is in the FEC sublayer, RS(544,514) aka “KP4” FEC
  - An AUI may exist between the FEC and PCS sublayers



802.3cd PCS/FEC Sublayers

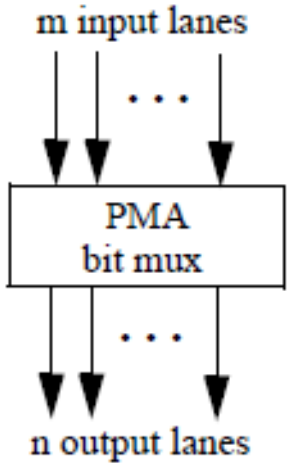
- PCS processing flow is shown in the figure to the left, FEC to the right





802.3cd PMA

- From a muxing point of view, the PMA is simple, m input lanes are bit muxed to n output lanes
- Bit muxing is blind, lanes can move around, the RX PCS sorts things out
- Clock content and baseline wander simulations have been performed for 1:1, 2:1 and 4:1 muxing scenarios
- Precoding supported on C2C and KR/CR PMDs
  - Must implement in TX, optional to implement in RX and the feature is optional to enable



Proposal

- Adopt Clause 119 as the PCS/FEC and Clause 120 as the PMA for all 200 Gb/s and 400Gb/s interfaces for this project (AUIs, backplane and copper cable interfaces).

- Adopt Clause 82 as the PCS, Clause 91 as the FEC (RS544), and Clause 135 as the PMA for 100 Gb/s Attachment Unit interfaces (both Chip-to-module and Chip-to-chip) for this project.
  - Leave the PCS/FEC/PMA decision for 100GBASE-KR1/CR1 open for further discussion
  - C2C here is meant to be the C2C-S that has been discussed, similar loss budget to C2M

Thanks!