Baseline Proposal for 100, 200 and 400 Gb/s Backplane

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IEEE 802.3ck 100 Gb/s, 200 Gb/s and 400 Gb/s Electrical Interfaces Task Force

Acknowledgements

- Thank you to Beth Kochuparambil, Rich Mellitz, Phil Sun and Adam Healey for guidance, feedback and questions.

- This proposal follows the approach used in [li_3cd_01b_0916.pdf](li_3cd_01b_0916.pdf) From Mike Li and Mike Dudek.

Method

- Leverage the 802.3cd specification with modifications for updated COM reference package, reference receiver and SerDes parameters.
  - Clause 137
  - Annex 93A

- Propose to use the same per lane specifications for 100GBASE-KR1, 200GBASE-KR2 and 400GBASE-KR4. The presentation refers to 100GBASE-KR for all of these per lane specifications.

- Some specific values are marked as TBD. Others have proposed values with acknowledgment that they are expected to require further analysis and discussion.

- Presentation is broken into two sections:
  - Clause structure: propose to adopt it
  - COM Rx arch: expect discussion

Contents

- **Clause Structure**
  - PMD
  - Compliance Points
  - Transmitter Characteristics
  - Receiver Characteristics
  - Channel
  - Environmental Specs & PICS

- **COM Specifics**

Clause Structure

PMD

- ## PMD clause structure
  - Follow the structure contained in 137.1-137.8.
  - Several functional specifications in 137.8 (PMD functional specifications) refer to requirements in Clause 136. Need to coordinate this with the corresponding 100GBASE-CR Clause.

- ## MDI
  - The MDI for 50GBASE-KR PHY is an implementation-dependent direct electrical connection between the PMD and the medium.
  - The MDI comprises two differential pairs, one for the transmit function and one for the receive function, marked by TP0 and TP5 in Figure 137–2.
  - Transmitter and receiver characteristics are defined at TP0a and TP5a, which are connected to the MDI through the test fixtures described in 93.8.1.1 and 93.8.2.1.

Compliance Points

- Compliance point definition
  - The electrical characteristics for the 100GBASE-KR interfaces are defined at compliance points for the transmitter (TP0a) and receiver (TP5a), respectively.
  - The location of TP0a and electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93-5 and 93.8.1.1, respectively.
  - The location of TP5a and electrical characteristics of the test fixture used to measure the receiver are defined in Figure 93-10 and 93.8.2.1, respectively.

Transmitter Characteristics

- Transmitter electrical characteristics at TP0a for 100GBASE-KR are the same as those summarized in Table 120D-1 and detailed in 120D.3.1.1 through 120D.3.1.2.2, except
  - Steady state voltage v_f (max): 0.60 V
  - Steady state voltage v_f (min): 0.40 V
  - Linear fit pulse peak (min): $0.75 \times v_f$
  - Signal-to-noise-and-distortion ratio (min): TBD dB Equalization: defined in slide 7

- ERL: pass/fail spec = TBD dB, using same parameters as in Table 137-5, except
  - T_r = 0.01 ns, ρ_x = 0.32, N = 100 UI

Transmitter Equalization
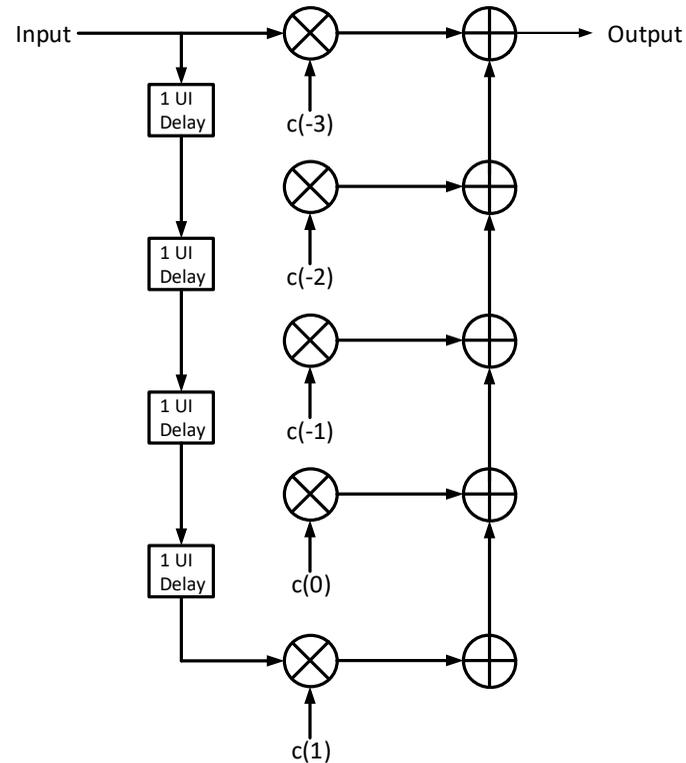
Coefficient	Amplitude		Step Size
	Min	Max	
$c(-3)$	-0.06	0	0.02
$c(-2)$	0	0.12	0.02
$c(-1)$	-0.34	0	0.02
$c(0)$	0.54		
$c(1)$	-0.1	0	0.05

TxEQ values go in the COM Table (refer to Table 137-6 for an example). Refer to "config_com_ieee8023_93a=100GEL-KR_DFE_121918.xls" in

http://www.ieee802.org/3/ck/public/tools/tools/mellitz_3ck_adhoc_01_121918_COM2p57.zip.
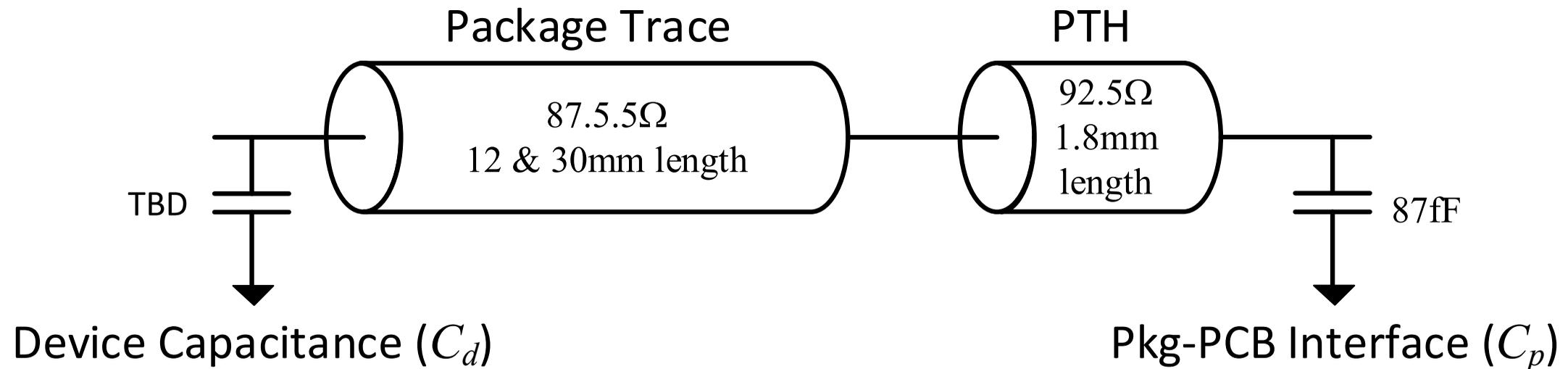
Receiver Spec

- Receiver characteristics at TP5a for 100GBASE-KR are the same as those in 137.9, except:
  - Insertion loss @ 26.5625 GHz values for Test 1 are TBD (min) and TBD (max).
  - Insertion loss @ 26.5625 GHz values for Test 2 are TBD (min) and TBD (max).

- ERL: pass/fail spec = TBD dB, using same parameters as in Table 137-5, except
  - T_r = 0.01 ns
  - ρ_x = 0.32
  - N = 100 UI

Channel Spec

- COM: base upon table 137-6 with modifications per "config_com_ieee8023_93a=100GEL-KR_DFE_121918.xls" in mellitz_3ck_adhoc_01_121918_COM2p57.zip.
  - Transmit equalizer per the values in slide 8.
  - Flexible reference package per slide 13.
  - TBD items: SNR_{Tx} (dB), η_0, C_d, Rx equalizer architecture

- Insertion Loss: Follow Clause 137.10.1, scaling to achieve 28dB @ 26.5625 GHz, and extending to 53.125 GHz.

- ERL: Follow Clause 137.10.2, pass/fail spec = TBD dB, using parameters in Table 137-5, except
  - T_r = 0.01ns, ρ_x = 0.25, N = 2000

Channel Spec – Reference Package

- Adopt the flexible package model proposed in
  http://www.ieee802.org/3/ck/public/19_01/benartsi_3ck_01_0119.pdf.

- Modify 93.A.1.2 to comprehend the flexible package model.

Package Trace

PTH

$87.5.5\Omega$
12 & 30mm length

92.5Ω
1.8mm
length

TBD

87fF

Device Capacitance (C_d)

Pkg-PCB Interface (C_p)

Environmental Specs & PICS

- Environmental Specs: Base on 137-11.
- PICS: Base on 137-12 with updates as needed.

COM Rx Arch

COM Proposal

- Reference Rx: DFE-based as in existing Clause 137 & Annex 93A with modifications:
  - 16 contiguous taps & 4 floating taps with location range up to 40 UI from cursor.
  - Tap selection method described in heck_3ck_01_0319.pdf.
  - $b_{max}(1)$=0.85, $b_{max}(2\ldots N_b)$=0.2
  - Requires modification to Annex 93A.

Summary

- Propose that the P802.3ck task force adopt the Clause Structure contained on slides 6-13.

- Separately propose that the P802.3ck task force adopt the specific COM proposal described on slide 15.

Thank you!