100GEL C2M Channel model Study Update

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IEEE 802.3 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interface Task Force

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- C2M Channel Simulation
  - Simulation Conditions
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- Conclusion

Purpose

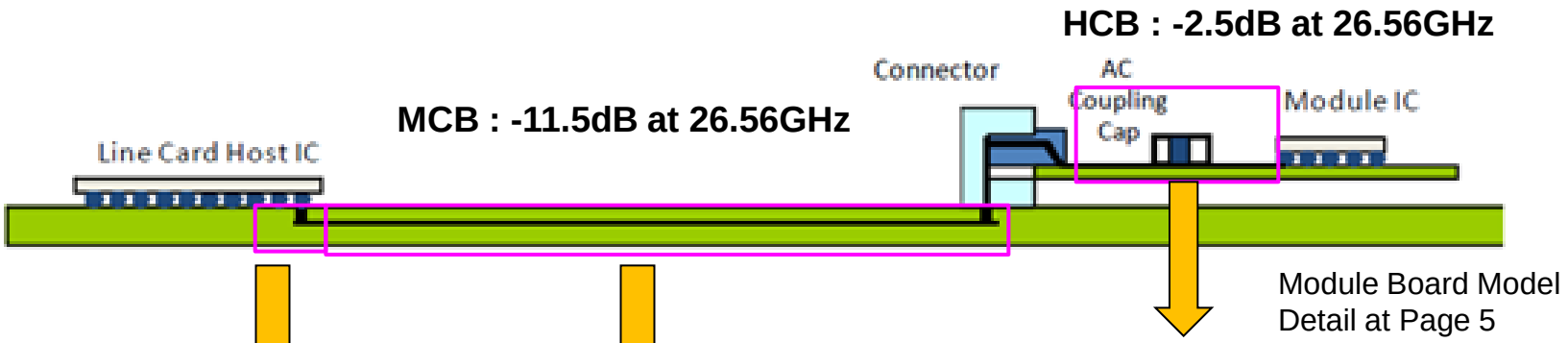
- This update added BGA PAD to a 100G/lane channel model and examined it.
  - Board Model of Chip (Line Card Host IC) mounting Area included in this channel model
  - Simulated by Normal Mating of Connector condition.
    QSFP-DD,OSFP,CFP2,CFP8,QSFP,DSFP.
  - Offer the touch stone files of the total model including MCB and HCB layout and the TH impedance improvement of all channels
  - COM calculated at each case for Reference

- QSFP-DD connector is improved for 112G, other connector models were same as last presentation at Long Beach.

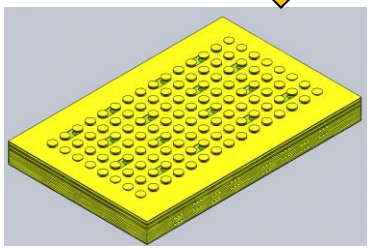
- COM files were used “com_ieee_93a_258.m”.

Simulation Conditions of Channel Model

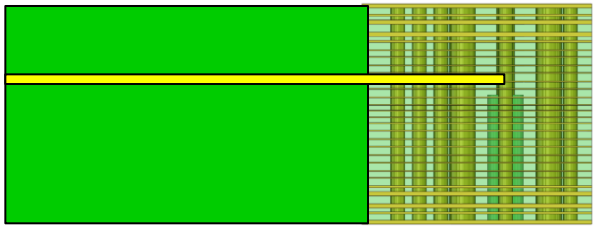
Host and Module board



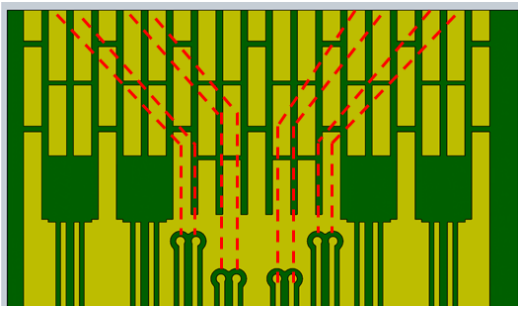
Module Board Model
Detail at Page 5



Chip PAD Model
Detail at Page 8~10



TH and SL Model
Detail at Page 7

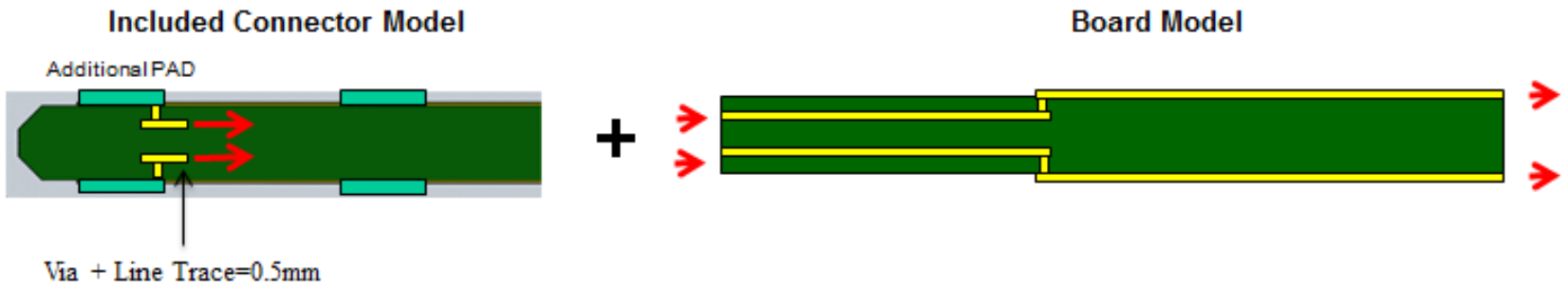


HCB and MCB Insertion loss are shown at Page 11.

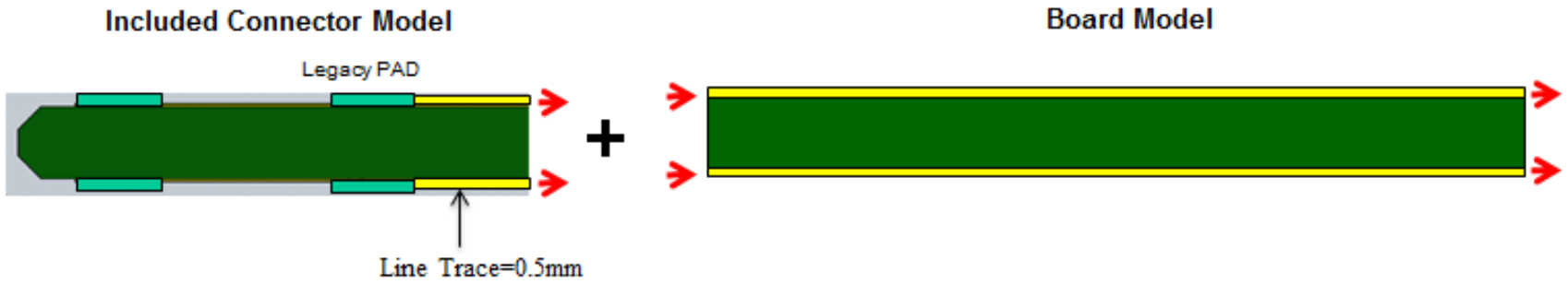
Simulation Conditions of QSFP-DD Module board

1. Connector model included one Via of module board.
2. Board model of additional Pad have one via in the Board. And Legacy Pad is surface trace.
3. Total insertion loss of each channel are -2.5dB at 26.56GHz.

Additional PAD



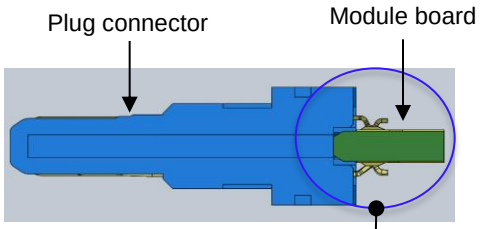
Legacy PAD

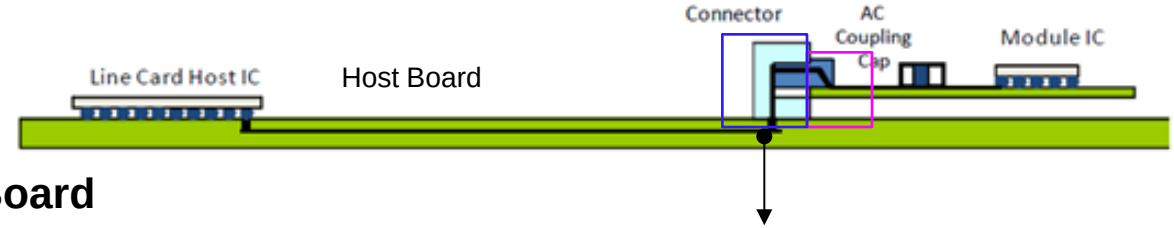


Simulation Conditions of other connector Module board

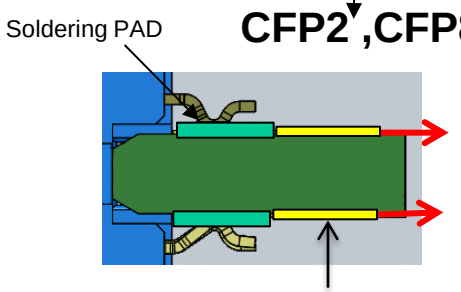
- Simulation Conditions of connector : Host and Module Board

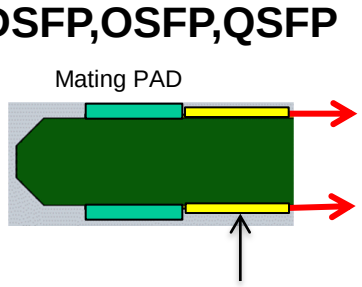
Host board: 1.5mm Line from the soldering PAD of connector. tan δ of Board is zero and Line loss is zero.
Module board: They are shown the figures below. tan δ of Board is zero and Line loss is zero.
Via of board: There are no Via of each boards for simulation model of connectors.

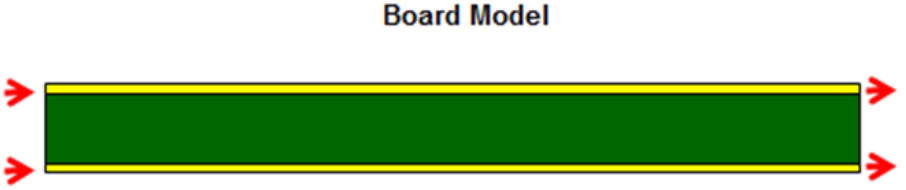




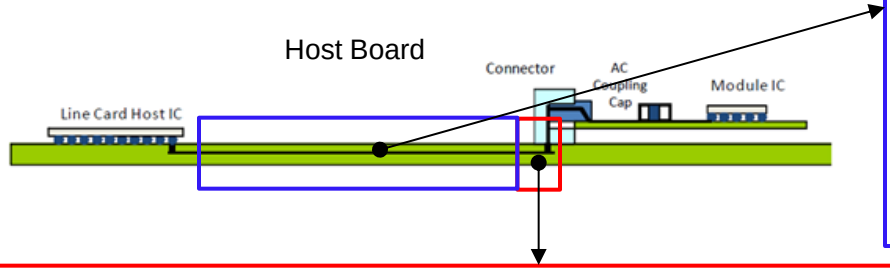
Module Board

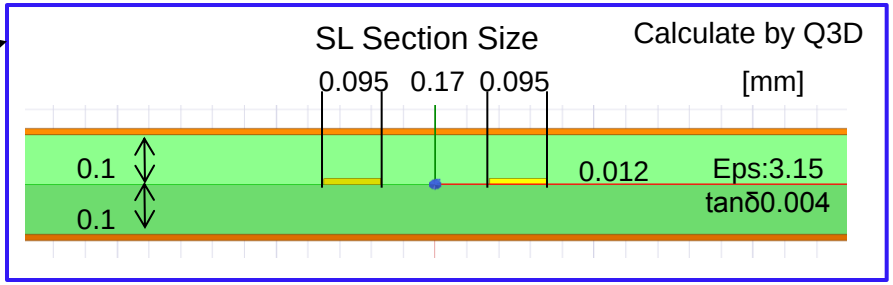




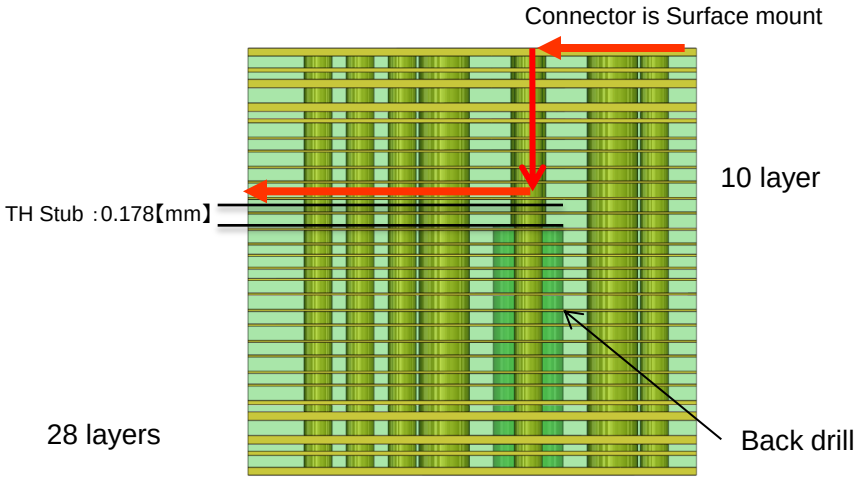


Simulation Conditions of TH and SL Model

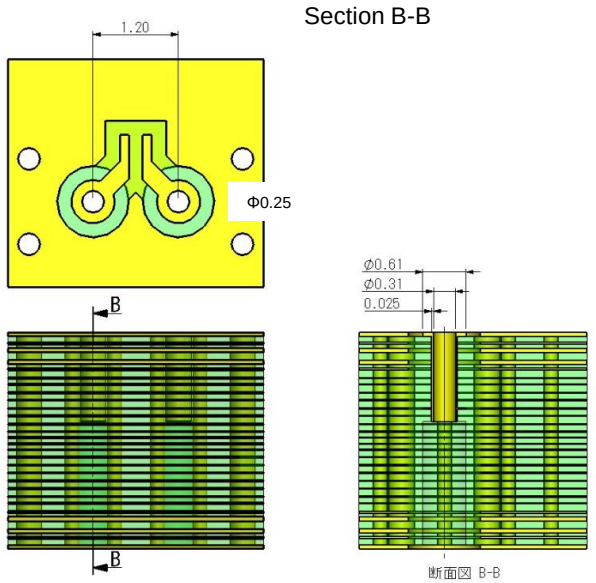




Host Board Layer stack-up and routing

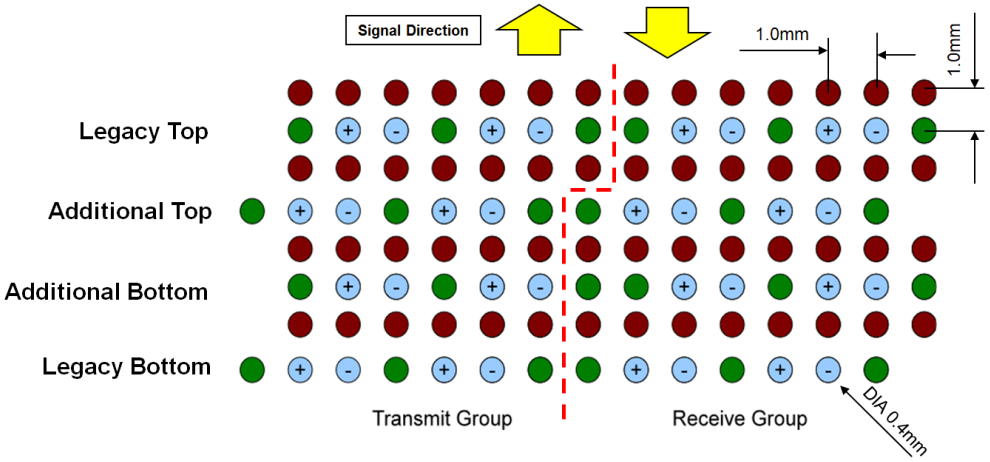


TH Dimension φ0.254

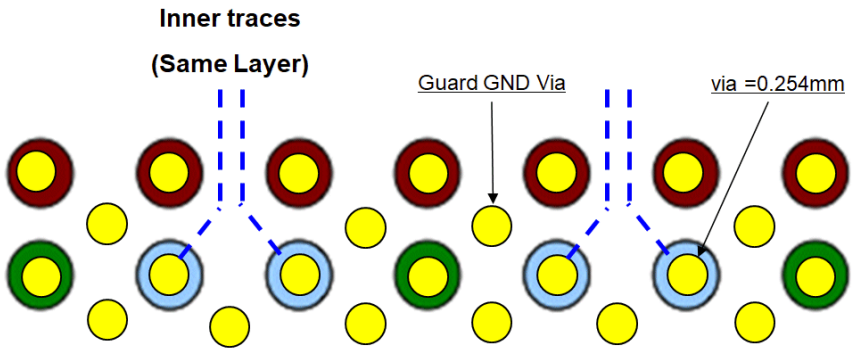


Simulation Conditions of Chip PAD Model

PAD Layout and via condition



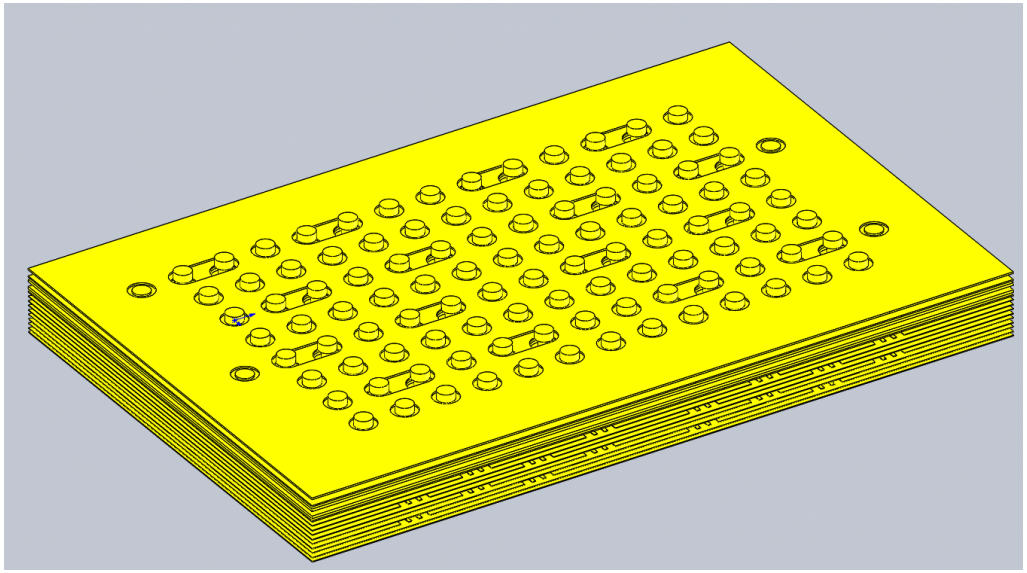
Detail of via and trace



Simulation Conditions of Chip PAD Model

3D model and Stuck up

3D model (BGA side)

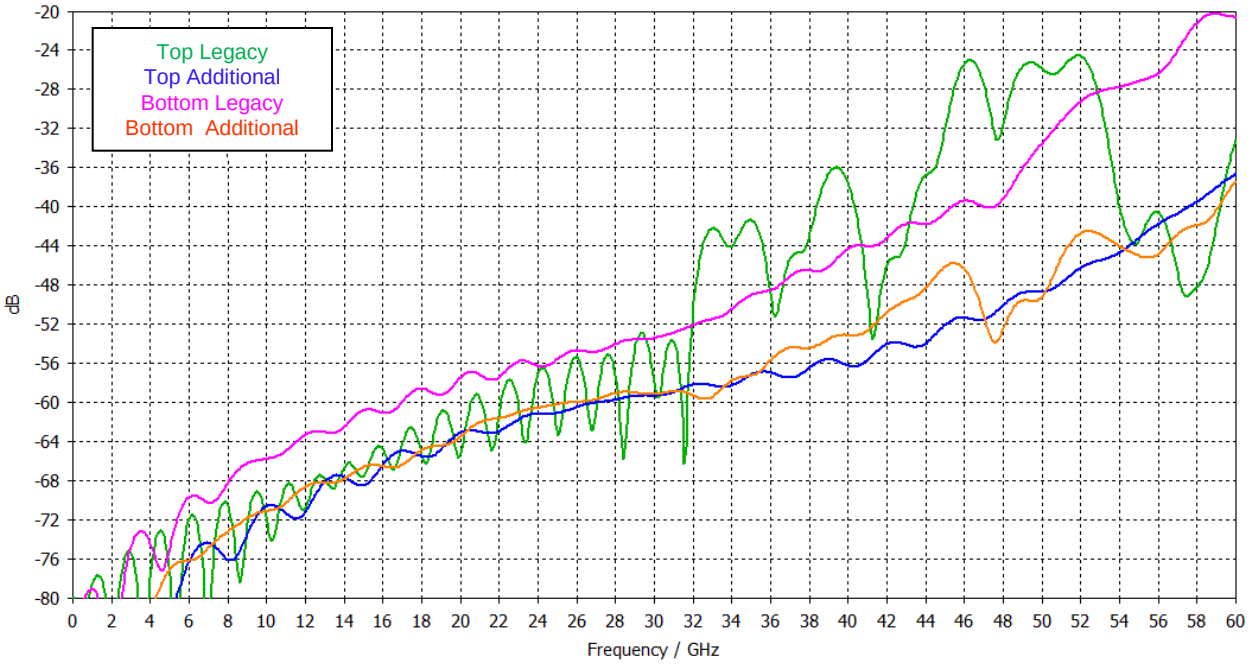


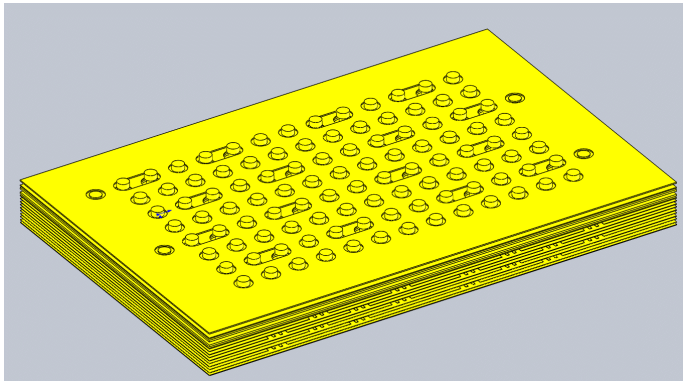
Stuck up

Layer	Thickness[mm]	Total Thickness[mm]	
SR	0.015		
1	0.055		L1
	0.085	0.055	
2	0.030	0.140	GND
	0.060	0.171	
3	0.060	0.231	GND
	0.110	0.291	
4	0.060	0.401	GND
	0.050	0.461	
5	0.030	0.511	GND
	0.090	0.541	
6	0.012	0.631	HS SIG
	0.100	0.643	
7	0.015	0.743	GND
	0.090	0.758	
8	0.090	0.848	HS SIG
	0.100	0.938	
9	0.015	1.038	GND
	0.090	1.054	
10	0.012	1.144	HS SIG
	0.100	1.156	
11	0.015	1.256	GND
	0.090	1.271	
12	0.012	1.361	HS SIG
	0.100	1.373	
13	0.015	1.473	GND
	0.065	1.488	
14	0.015	1.553	GND

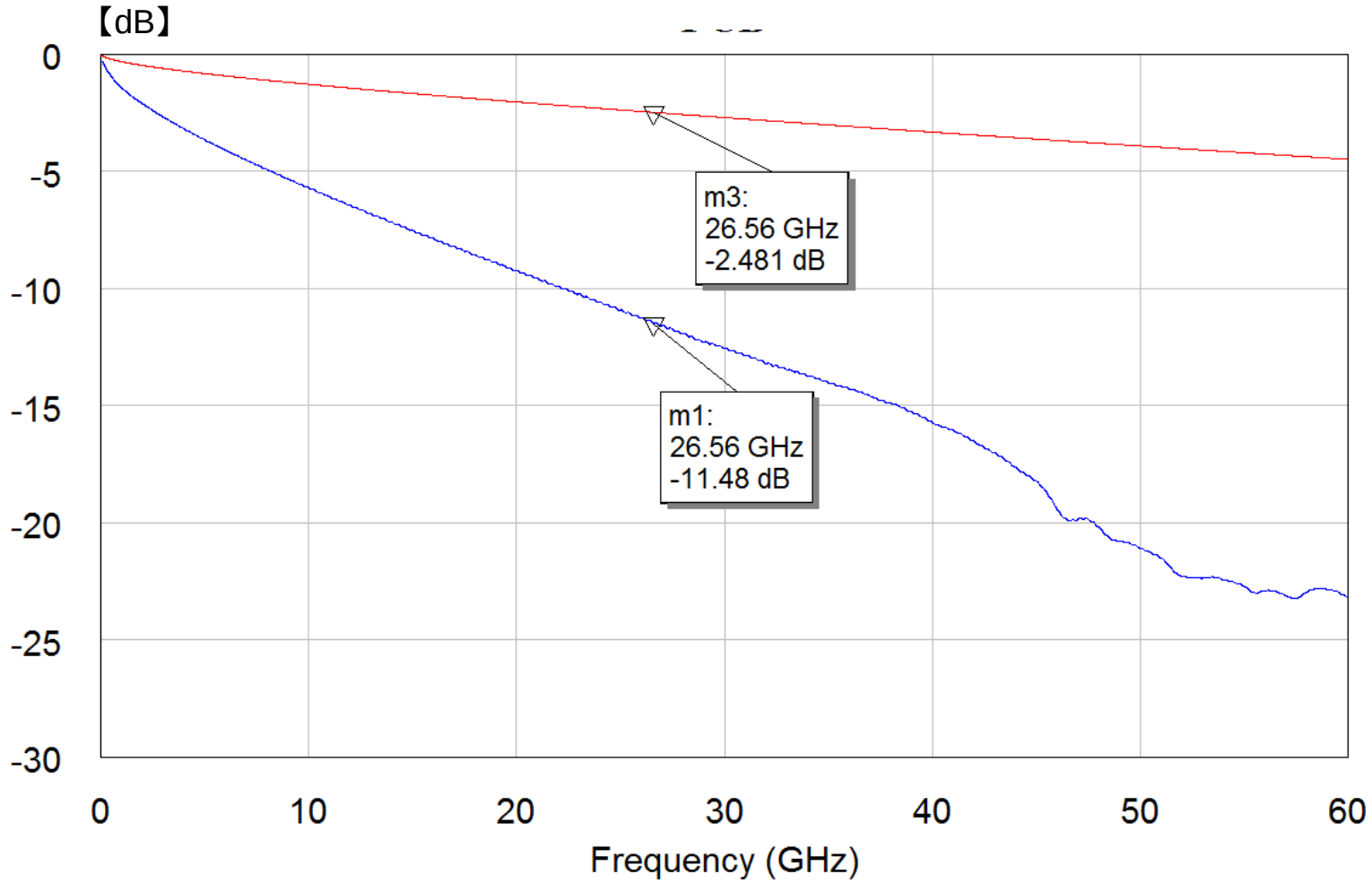
Simulation Result : FEXT of Chip PAD Model

- This Cross-talk are Side by Side of each channels





Insertion Loss of Module and Host Board



COM file : com_ieee_93a_258.m

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.1	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.9e-4 0]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[14 15 30; 1.8 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[14 15 30; 1.8 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[14 15 30; 1.8 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0 0; 0 0 0]	mm	[test cases]
C_p	[0.9e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.63	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.65		min
c(-1)	[-0.2:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:0.5:-4]	dB	[min:step:max]
f_z	18.55345912	GHz	
f_p1	53.1	GHz	
f_p2	28.2	GHz	
g_DC_HP	[-3:0.5:-1]		[min:step:max]
f_HP_PZ	1.2	GHz	
ffe_pre_tap_len	**0**	UI	
ffe_post_tap_len	4	UI	
Include PCB	0	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	1		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical

TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

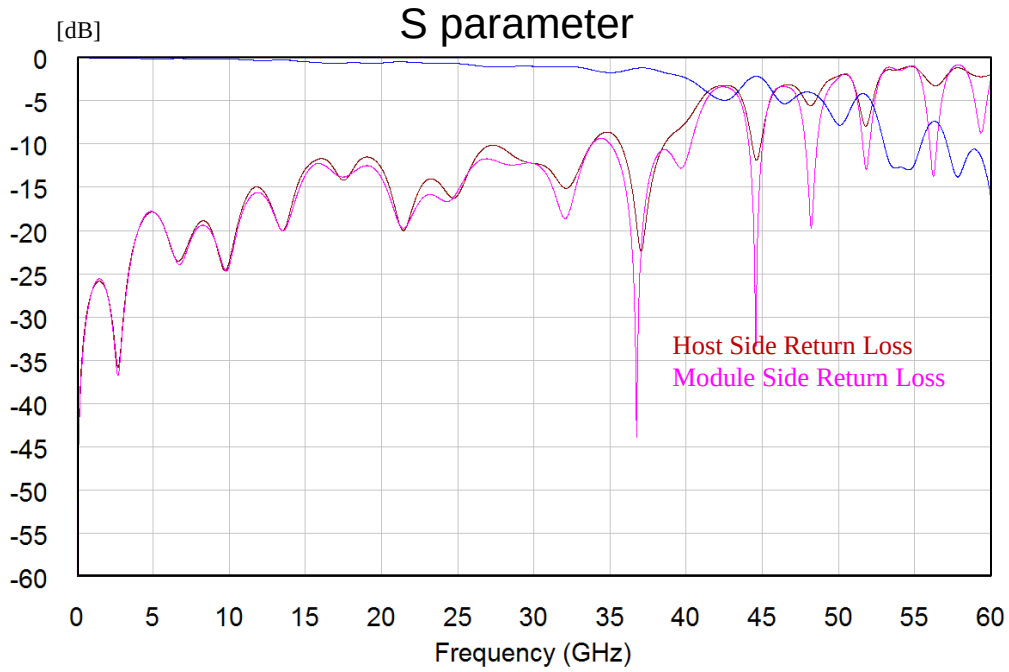
Table 93A≷3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92≷12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*50*	mm
z_bp (NEXT)	*50*	mm
z_bp (FEXT)	*50*	mm
z_bp (RX)	*0*	mm

Parameter is default of Sheet:
N_b = 1
B_max(1) = 0.5
ffe_pre_tap_len = 0
ffe_post_tap_len = 4
(5-tap FFE wih 4 postcursor taps)

Spread sheet : config_100GEL_C2M7CK.xls

Simulation Result : QSFP-DD connector Normal Mating Model



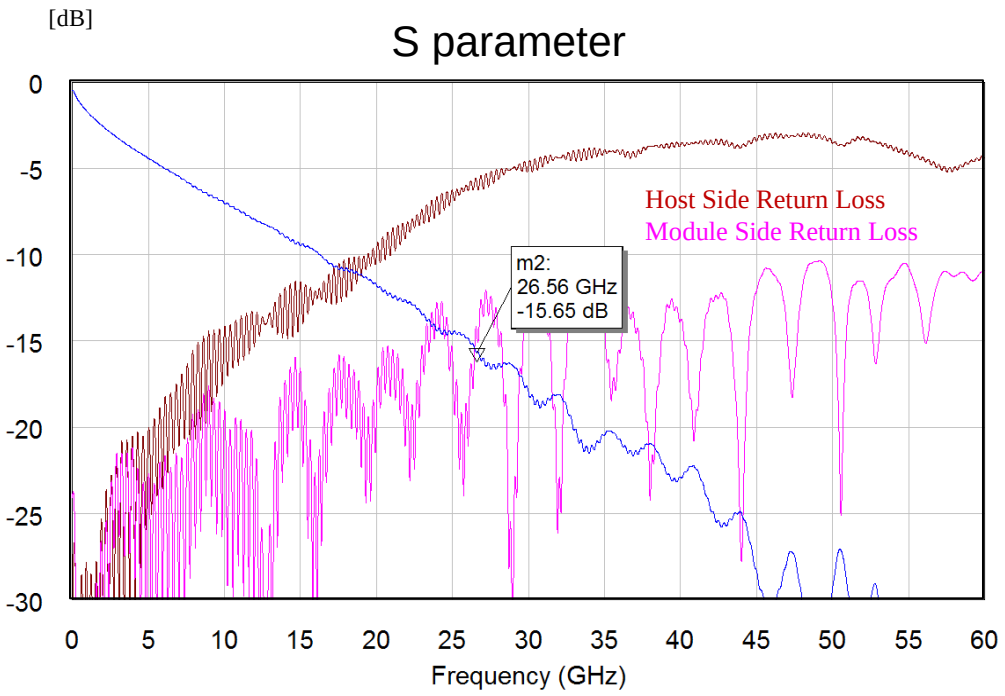
* This S-parameter is shown Legacy Top channel model.
* Channel mapping is refer to following.

	RX Side				TX Side
Legacy Top ch	FEXT1	Victim	DATA	NEXT1	NEXT2
Additional Top ch	FEXT2	FEXT3	DATA	NEXT3	NEXT4
Additional Bottom ch	FEXT4	FEXT5	DATA	NEXT5	NEXT6
Legacy Bottom ch	FEXT6	FEXT7	DATA	NEXT7	NEXT8

Touch stone files

Legacy TOP	Additional TOP	Additional BOTTOM	Legacy BOTTOM
QSFPDD_S_legacytop_normal_THRU.s4p	QSFPDD_S_additionaltop_normal_THRU.s4p	QSFPDD_S_additionalbottom_normal_THRU.s4p	QSFPDD_S_legacybottom_normal_THRU.s4p
QSFPDD_S_legacytop_normal_FEXT1.s4p	QSFPDD_S_additionaltop_normal_FEXT1.s4p	QSFPDD_S_additionalbottom_normal_FEXT1.s4p	QSFPDD_S_legacybottom_normal_FEXT1.s4p
QSFPDD_S_legacytop_normal_FEXT2.s4p	QSFPDD_S_additionaltop_normal_FEXT2.s4p	QSFPDD_S_additionalbottom_normal_FEXT2.s4p	QSFPDD_S_legacybottom_normal_FEXT2.s4p
QSFPDD_S_legacytop_normal_FEXT3.s4p	QSFPDD_S_additionaltop_normal_FEXT3.s4p	QSFPDD_S_additionalbottom_normal_FEXT3.s4p	QSFPDD_S_legacybottom_normal_FEXT3.s4p
QSFPDD_S_legacytop_normal_FEXT4.s4p	QSFPDD_S_additionaltop_normal_FEXT4.s4p	QSFPDD_S_additionalbottom_normal_FEXT4.s4p	QSFPDD_S_legacybottom_normal_FEXT4.s4p
QSFPDD_S_legacytop_normal_FEXT5.s4p	QSFPDD_S_additionaltop_normal_FEXT5.s4p	QSFPDD_S_additionalbottom_normal_FEXT5.s4p	QSFPDD_S_legacybottom_normal_FEXT5.s4p
QSFPDD_S_legacytop_normal_FEXT6.s4p	QSFPDD_S_additionaltop_normal_FEXT6.s4p	QSFPDD_S_additionalbottom_normal_FEXT6.s4p	QSFPDD_S_legacybottom_normal_FEXT6.s4p
QSFPDD_S_legacytop_normal_FEXT7.s4p	QSFPDD_S_additionaltop_normal_FEXT7.s4p	QSFPDD_S_additionalbottom_normal_FEXT7.s4p	QSFPDD_S_legacybottom_normal_FEXT7.s4p
QSFPDD_S_legacytop_normal_NEXT1.s4p	QSFPDD_S_additionaltop_normal_NEXT1.s4p	QSFPDD_S_additionalbottom_normal_NEXT1.s4p	QSFPDD_S_legacybottom_normal_NEXT1.s4p
QSFPDD_S_legacytop_normal_NEXT2.s4p	QSFPDD_S_additionaltop_normal_NEXT2.s4p	QSFPDD_S_additionalbottom_normal_NEXT2.s4p	QSFPDD_S_legacybottom_normal_NEXT2.s4p
QSFPDD_S_legacytop_normal_NEXT3.s4p	QSFPDD_S_additionaltop_normal_NEXT3.s4p	QSFPDD_S_additionalbottom_normal_NEXT3.s4p	QSFPDD_S_legacybottom_normal_NEXT3.s4p
QSFPDD_S_legacytop_normal_NEXT4.s4p	QSFPDD_S_additionaltop_normal_NEXT4.s4p	QSFPDD_S_additionalbottom_normal_NEXT4.s4p	QSFPDD_S_legacybottom_normal_NEXT4.s4p

Simulation Result : QSFP-DD Normal Mating Channel Model



* This S-parameter is shown Legacy Top channel model.
* Channel mapping is refer to following.

	RX Side				TX Side
Legacy Top ch	FEXT1	Victim	DATA	NEXT1	NEXT2
Additional Top ch	FEXT2	FEXT3	DATA	NEXT3	NEXT4
Additional Bottom ch	FEXT4	FEXT5	DATA	NEXT5	NEXT6
Legacy Bottom ch	FEXT6	FEXT7	DATA	NEXT7	NEXT8

Touch stone files

Legacy TOP	Additional TOP	Additional BOTTOM	Legacy BOTTOM
QSFPDD_SC_legacytop_normal_THRU.s4p	QSFPDD_SC_additionaltop_normal_THRU.s4p	QSFPDD_SC_additionalbottom_normal_THRU.s4p	QSFPDD_SC_legacybottom_normal_THRU.s4p
QSFPDD_SC_legacytop_normal_FEXT1.s4p	QSFPDD_SC_additionaltop_normal_FEXT1.s4p	QSFPDD_SC_additionalbottom_normal_FEXT1.s4p	QSFPDD_SC_legacybottom_normal_FEXT1.s4p
QSFPDD_SC_legacytop_normal_FEXT2.s4p	QSFPDD_SC_additionaltop_normal_FEXT2.s4p	QSFPDD_SC_additionalbottom_normal_FEXT2.s4p	QSFPDD_SC_legacybottom_normal_FEXT2.s4p
QSFPDD_SC_legacytop_normal_FEXT3.s4p	QSFPDD_SC_additionaltop_normal_FEXT3.s4p	QSFPDD_SC_additionalbottom_normal_FEXT3.s4p	QSFPDD_SC_legacybottom_normal_FEXT3.s4p
QSFPDD_SC_legacytop_normal_FEXT4.s4p	QSFPDD_SC_additionaltop_normal_FEXT4.s4p	QSFPDD_SC_additionalbottom_normal_FEXT4.s4p	QSFPDD_SC_legacybottom_normal_FEXT4.s4p
QSFPDD_SC_legacytop_normal_FEXT5.s4p	QSFPDD_SC_additionaltop_normal_FEXT5.s4p	QSFPDD_SC_additionalbottom_normal_FEXT5.s4p	QSFPDD_SC_legacybottom_normal_FEXT5.s4p
QSFPDD_SC_legacytop_normal_FEXT6.s4p	QSFPDD_SC_additionaltop_normal_FEXT6.s4p	QSFPDD_SC_additionalbottom_normal_FEXT6.s4p	QSFPDD_SC_legacybottom_normal_FEXT6.s4p
QSFPDD_SC_legacytop_normal_FEXT7.s4p	QSFPDD_SC_additionaltop_normal_FEXT7.s4p	QSFPDD_SC_additionalbottom_normal_FEXT7.s4p	QSFPDD_SC_legacybottom_normal_FEXT7.s4p
QSFPDD_SC_legacytop_normal_NEXT1.s4p	QSFPDD_SC_additionaltop_normal_NEXT1.s4p	QSFPDD_SC_additionalbottom_normal_NEXT1.s4p	QSFPDD_SC_legacybottom_normal_NEXT1.s4p
QSFPDD_SC_legacytop_normal_NEXT2.s4p	QSFPDD_SC_additionaltop_normal_NEXT2.s4p	QSFPDD_SC_additionalbottom_normal_NEXT2.s4p	QSFPDD_SC_legacybottom_normal_NEXT2.s4p
QSFPDD_SC_legacytop_normal_NEXT3.s4p	QSFPDD_SC_additionaltop_normal_NEXT3.s4p	QSFPDD_SC_additionalbottom_normal_NEXT3.s4p	QSFPDD_SC_legacybottom_normal_NEXT3.s4p
QSFPDD_SC_legacytop_normal_NEXT4.s4p	QSFPDD_SC_additionaltop_normal_NEXT4.s4p	QSFPDD_SC_additionalbottom_normal_NEXT4.s4p	QSFPDD_SC_legacybottom_normal_NEXT4.s4p

Conclusion

1) COMs of Yamaichi's calculation is shown as table of below . This is just reference.
2) QSFP-DD connector is improved for 112G, other connector is math production model. ALL model used chip PAD mode.
3) All normal mating connectors which I examined were able to satisfy COM3.0.

Normal Mating COM

Connector Type	Channel	PAD Model
QSFP-DD	Legacy top	5.349
	Additional top	5.130
	Additional bottom	5.984
	Legacy bottom	6.611
OSFP	TOP	6.702
	BOTTOM	6.866
QSFP	TOP	5.909
	BOTTOM	6.487
CFP2 (8ch)	TOP	6.488
CFP8	TOP	5.294
	BOTTOM	5.483
DSFP	TOP	6.799
	BOTTOM	6.230

For more information, please contact,

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