106Gbps C2M Simulation Updates

For IEEE 802.3ck

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Intel

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Objective and Motivation

- New C2M channels and packages became available recently
  - http://www.ieee802.org/3/ck/public/tools/c2m/lim_3ck_01_0319_c2m.zip
- Reference RX architectures
  - CTLE (2 options)
  - DFE/FFE options: FFE-only, FFE+DFE, or DFE-only
- C2M performance comparisons at TP1a
  - COM method: COM, VEC, VOE
  - Waveform simulation: Eye height/width, VEC
- Previous C2M studies was presented in 802.3ck and OIF CEI
  - *"106.25 Gb/s Per Lane VSR Studies: Typical TX FFE + RX CTLE/FFE vs. Longer TX FFE + RX CTLE"* by Mike Li, Hsinho Wu, Masashi Shimanouchi, Adee Ran, October 30, 2018
  - *"Updated C2M COM Simulations"* by Ali Ghiasi (ghiasi_3ck_adhoc_01_021319.pdf)
- Need to adjust C2M spec. RX to accommodate these channels

106.25 Gb/s C2M TP1a Link Simulations

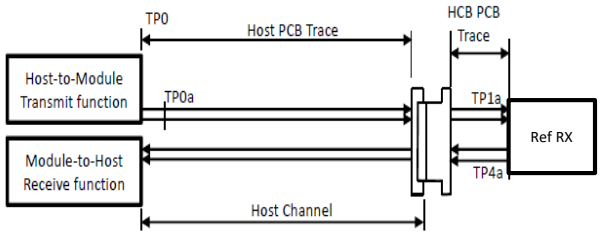
Link & Device Configurations

- **Data Rate: 106.25 Gbps, PAM-4**
- **Test Pattern:** QPRBS13, 1M Symbols (for waveform simulations)
- **Target BER: 10^{-5}**
- **TX Die**
  - VOD: 750 mV-pp (TP0a amplitude)
  - 20%-80% Rise/Fall Time: 6.16 ps
  - TX FIR:
    - Configuration:
      - 4 taps, 2 pre-taps and 1 post-tap
      - Range: Pre-tap 1: [-0.2, 0], Pre-tap 2: [0, 0.1], Post-tap1: [-0.1, 0]
      - Step size: 0.02
  - RLM (level mismatch): 0.95
  - TX termination: 50 Ω (align with 802.3ck LR)
  - TX Capacitance: 130 fF (align with 802.3ck LR)
  - Jitter/Noise
    - DJ: *0.04 UI-pp (dual-Dirac, A_{DD})*
    - *RJ: 0.01 UI-rms (sigma$_{RJ}$)*
    - Noise: *~8.89mV-rms (SNR$_{TX}$=32.5dB)*

TX/Host Package

- Package model: Latest trending 802.3ck LR package
  - Length: 15mm and 30mm T-line + 1.8mm PTH
  - T-line/PTH parameters: a1=0.0009909, a2= 0.0002772, tau=6.14e-3 ns/mm, Zc$_{T\text{-}line}$=87.5Ω, Zc$_{PTH}$=92.5Ω
  - PCB Zc = 87fF
- Package crosstalk is < -60 dB (by design)

TP1a Test Topology



106.25 Gb/s C2M TP1a Link Simulations

Link & Device Configuration *(cont.)*

TP1a Reference RX

- Die Termination: 50 ohms
- Capacitance: 0 fF
- AFE Filter and CTLE
  - Parameter scaled from IEEE 802.3cd ref. CTLE

$$H_r(f) = \frac{1}{1-3.414214\cdot\left(\frac{f}{f_r}\right)^2+\left(\frac{f}{f_r}\right)^4+j\cdot 2.613126\cdot\left(\frac{f}{f_r}-\left(\frac{f}{f_r}\right)^3\right)}$$

$$H_{CTF}(f)=G\cdot\frac{(10^{\frac{gdc2}{20}}+j\frac{f}{f_{z2}})}{(1+j\frac{f}{f_{zp}})}\cdot\frac{(10^{\frac{gdc}{20}}+j\frac{f}{f_{z1}})}{(1+j\frac{f}{f_{p1}})(1+j\frac{f}{f_{p2}})}$$

  - Baud: 53.125 Gsym/s
  - Option 1 (trending 802.3ck LR CTLE model)
    - *fp1 / fp2 / fz1 / fz2 / fzp = Baud ÷ 2.5 / 1.0 / 2.5 / 80 / 80*
  - Option 2 (proposed by Ali Ghiasi)
    - *fp1 / fp2 / fz1 / fz2 / fzp = Baud ÷ 1/0 / 1.883 / 2.862 / 40 / 40*
  - g_{DC}: *0 to -14dB*
  - g_{DC2}: *0 to -3dB*
  - G: 1.0 (constant)

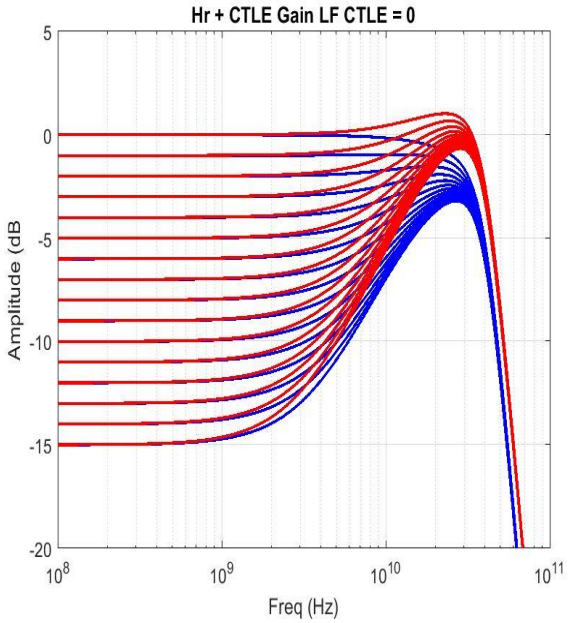
- FFE/DFE: 3 options
  - FFE-only
    - 5 Taps: 4 post-taps
  - FFE + DFE
    - FFE: 5 taps w/ 4 post-taps
    - DFE: 1 tap
  - DFE-only
    - 4 taps
  - Range:
    - FFE: First 1st post-cursors: +/-0.3 others: +/-0.1
    - DFE: First tap: +/-0.75, others: +/-0.2
- Jitter/Noise:
  - Input noise: *8.2e-9 V^2/GHz*

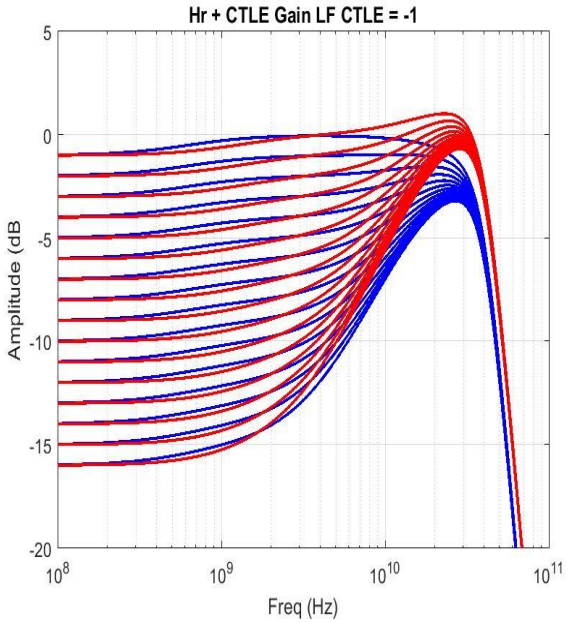
RX Package: None

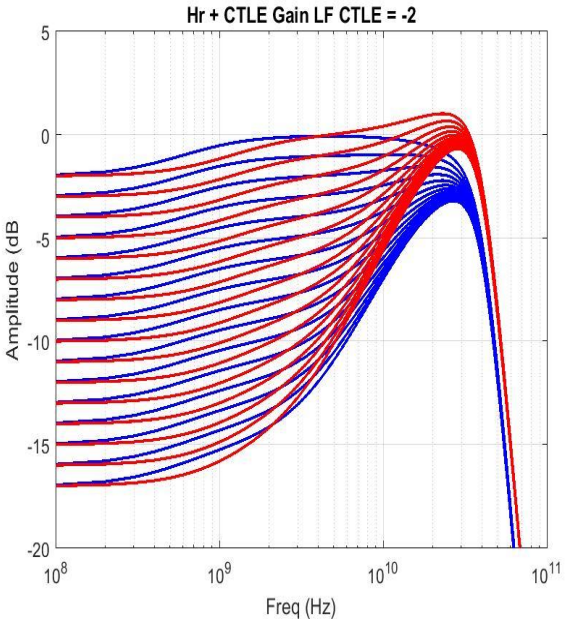
CTLE Comparison

Option 1 vs Option 2

Option 1
Option 2







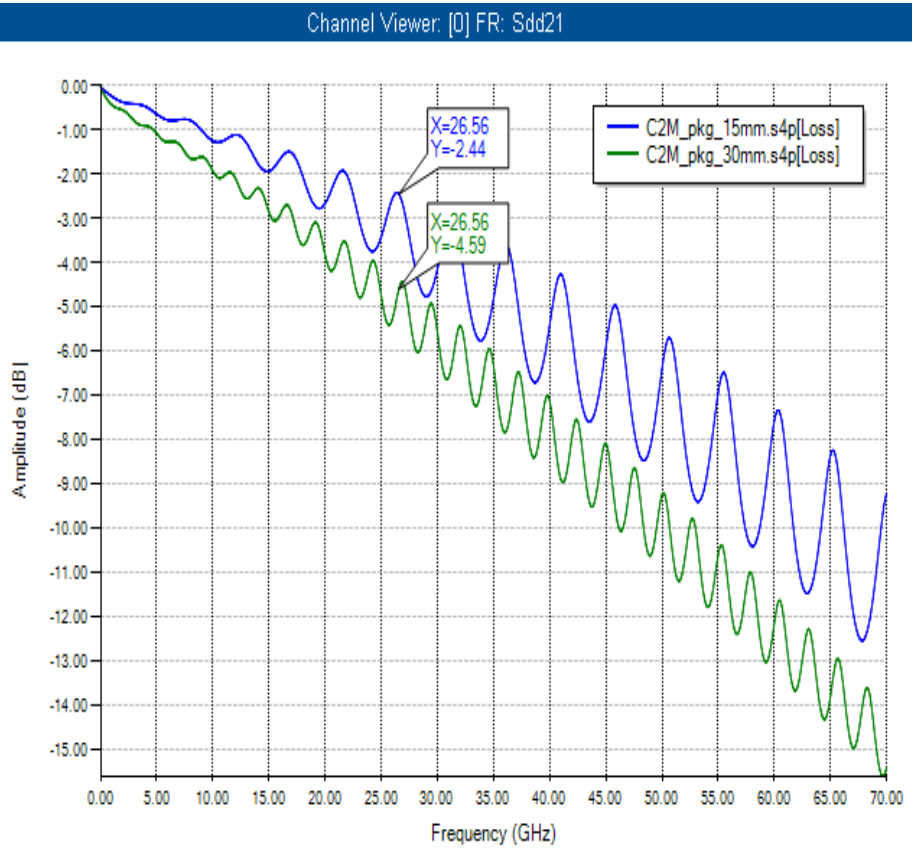
- CTLE Option 1
  - Current trending 802.3ck LR CTLE: fp1 / fp2 / fz1 / fz2 / fzp = Baud ÷ 2.5 / 1.0 / 2.5 / 80 / 80
- CTLE Option 2
  - Ali Ghiasi's design: fp1 / fp2 / fz1 / fz2 / fzp = Baud ÷ 1/0 / 1.883 / 2.862 / 40 / 40

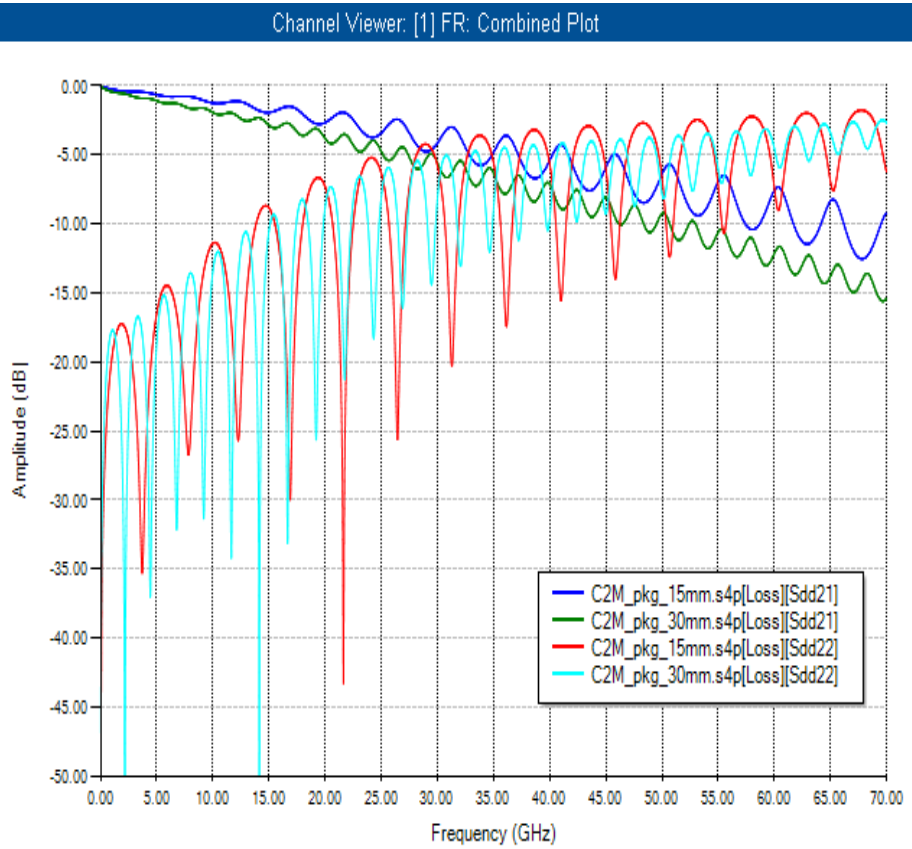
$$H_r(f) = \frac{1}{1-3.414214\cdot\left(\frac{f}{f_r}\right)^2+\left(\frac{f}{f_r}\right)^4+j\cdot 2.613126\cdot\left(\frac{f}{f_r}-\left(\frac{f}{f_r}\right)^3\right)}$$

$$H_{CTF}(f)=G\cdot\frac{\left(10^{\frac{gdc\,2}{20}}+j\frac{f}{f_{z2}}\right)}{\left(1+j\frac{f}{f_{zp}}\right)}\cdot\frac{\left(10^{\frac{gdc}{20}}+j\frac{f}{f_{z1}}\right)}{\left(1+j\frac{f}{f_{p1}}\right)\left(1+j\frac{f}{f_{p2}}\right)}$$

106.25 Gb/s C2M 15mm & 30mm Host Package Model

-- using latest trending 802.3ck LR Package Model





Test Channel Summary

Channel	Description	Insertion Loss (dB) @ 26.56 GHz	ICN (mV-rms)*
CH1	112G_16dB_(QSFPDD+module card)_TX7_L10	14.40 + TX Pkg	0.62
CH2	112G_16dB_(QSFPDD+module card)_TX7_L23	14.59 + TX Pkg	0.66
CH3	112G_16dB_(QSFPDD+module card)_TX3_L10	14.67 + TX Pkg	0.62
CH4	112G_16dB_(QSFPDD+module card)_TX3_L23	14.82 + TX Pkg	0.70
CH5	112G_16dB_(QSFPDD+module card)_TX7_Asic	14.76 + TX Pkg	1.22
CH6	112G_16dB_(QSFPDD+module card)_TX3_Asic	15.01 + TX Pkg	1.35

**: Channel files' f_{max} is less than f_{baud}. ICN results are informative. ICN is calculated with FEXT amplitude of 0.75$V_{peak-peak}$ and NEXT aggressor amplitude of 1.05$V_{peak-peak}$.*

Tentative 802.3ck C2M TP1a COM Configuration

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.375	V	
A_fe	0.375	V	
A_ne	0.525	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.65		min
c(-1)	[-0.2:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0.75		
b_max(2..N_b)	0.2		
g_DC	[-14:0.5:0]	dB	[min:step:max]
f_z	18.55345912	GHz	
f_p1	53.1	GHz	
f_p2	28.19968136	GHz	
g_DC_HP	[-3:0.5:0]		[min:step:max]
f_HP_PZ	1.3275	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	4	UI	
Include PCB	0	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	1		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_190303	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical

TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*50*	mm
z_bp (NEXT)	*50*	mm
z_bp (FEXT)	*50*	mm
z_bp (RX)	*50*	mm

- *COM 2.58 is used for this analysis*
- *CTLE option 2 and FFE-only RX is shown*

TP1a COM Analysis (w/ 30mm Host Package)

COM (dB) at BER 10^{-5}

Channel	Description	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH1	112G_16dB_(QSFPDD+module card)_TX7_L10	14.40	4.0546	4.7788	4.6263	4.1654	4.9098	4.744
CH2	112G_16dB_(QSFPDD+module card)_TX7_L23	14.59	3.7284	4.2897	4.0738	3.7962	4.4945	4.3185
CH3	112G_16dB_(QSFPDD+module card)_TX3_L10	14.67	4.1382	4.4585	4.5533	4.2782	4.84	4.5881
CH4	112G_16dB_(QSFPDD+module card)_TX3_L23	14.82	3.7017	4.0589	4.1239	3.884	4.4008	4.14
CH5	112G_16dB_(QSFPDD+module card)_TX7_Asic	14.76	3.4785	4.2293	3.9595	3.6615	4.4514	4.1675
CH6	112G_16dB_(QSFPDD+module card)_TX3_Asic	15.01	3.098	3.6456	3.6759	3.3394	4.171	3.8529

VEC (dB) at BER 10^{-5}

Channel	Description	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH1	112G_16dB_(QSFPDD+module card)_TX7_L10	14.40	8.5658	7.4701	7.6824	8.3828	7.2945	7.5177
CH2	112G_16dB_(QSFPDD+module card)_TX7_L23	14.59	9.1435	8.1845	8.5338	9.0184	7.8733	8.1396
CH3	112G_16dB_(QSFPDD+module card)_TX3_L10	14.67	8.4272	7.9266	7.7872	8.2026	7.3873	7.7369
CH4	112G_16dB_(QSFPDD+module card)_TX3_L23	14.82	9.1934	8.5588	8.4507	8.8605	8.0134	8.4242
CH5	112G_16dB_(QSFPDD+module card)_TX7_Asic	14.76	9.6297	8.2799	8.7282	9.2696	7.9373	8.3794
CH6	112G_16dB_(QSFPDD+module card)_TX3_Asic	15.01	10.4576	9.3001	9.2423	9.9193	8.3737	8.9159

VEO (mV) at BER 10^{-5}

Channel	Description	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH1	112G_16dB_(QSFPDD+module card)_TX7_L10	14.40	7.4211	11.3848	9.2988	9.3412	15.4262	14.5906
CH2	112G_16dB_(QSFPDD+module card)_TX7_L23	14.59	6.7299	10.4993	8.2461	8.1124	14.517	13.0106
CH3	112G_16dB_(QSFPDD+module card)_TX3_L10	14.67	7.1364	10.9073	9.0277	9.8908	15.5876	13.4592
CH4	112G_16dB_(QSFPDD+module card)_TX3_L23	14.82	6.4051	7.8986	7.9968	8.1083	14.2371	11.1627
CH5	112G_16dB_(QSFPDD+module card)_TX7_Asic	14.76	6.3367	10.2751	7.9812	7.8019	13.9108	12.2287
CH6	112G_16dB_(QSFPDD+module card)_TX3_Asic	15.01	5.4724	9.3145	7.0492	7.0979	13.4993	10.6407

CTLE option 2 improves VEO by ~3.5mV over CTLE option 1.

TP1a COM Analysis (w/ 15mm Host Package)

COM (dB) at BER 10^{-5}

Channel	Description	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH1	112G_16dB_(QSFPDD+module card)_TX7_L10	14.40	3.4599	4.3315	4.2494	3.5852	4.5501	4.6703
CH2	112G_16dB_(QSFPDD+module card)_TX7_L23	14.59	2.4272	3.7057	3.5759	2.3792	3.9268	3.8568
CH3	112G_16dB_(QSFPDD+module card)_TX3_L10	14.67	3.202	4.1359	4.083	3.1221	4.5596	4.2441
CH4	112G_16dB_(QSFPDD+module card)_TX3_L23	14.82	1.5176	3.4834	3.6585	1.8738	3.9564	3.8282
CH5	112G_16dB_(QSFPDD+module card)_TX7_Asic	14.76	1.6216	3.6047	3.2754	1.7839	3.7541	3.5611
CH6	**112G_16dB_(QSFPDD+module card)_TX3_Asic**	15.01	0.5624	3.5071	3.5177	0.8569	3.9986	3.6609

VEC (dB) at BER 10^{-5}

Channel	Description	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH1	112G_16dB_(QSFPDD+module card)_TX7_L10	14.40	9.6677	8.1195	8.248	9.4171	7.7919	7.6201
CH2	112G_16dB_(QSFPDD+module card)_TX7_L23	14.59	12.2594	9.1859	9.4352	12.41	8.7851	8.909
CH3	112G_16dB_(QSFPDD+module card)_TX3_L10	14.67	10.2198	8.431	8.5184	10.4016	7.778	8.2565
CH4	112G_16dB_(QSFPDD+module card)_TX3_L23	14.82	15.9009	9.6197	9.2754	14.2417	8.7336	8.9603
CH5	112G_16dB_(QSFPDD+module card)_TX7_Asic	14.76	15.3757	9.3791	10.0573	14.6257	9.0958	9.4644
CH6	**112G_16dB_(QSFPDD+module card)_TX3_Asic**	15.01	24.0553	9.572	9.5506	20.5427	8.6609	9.2708

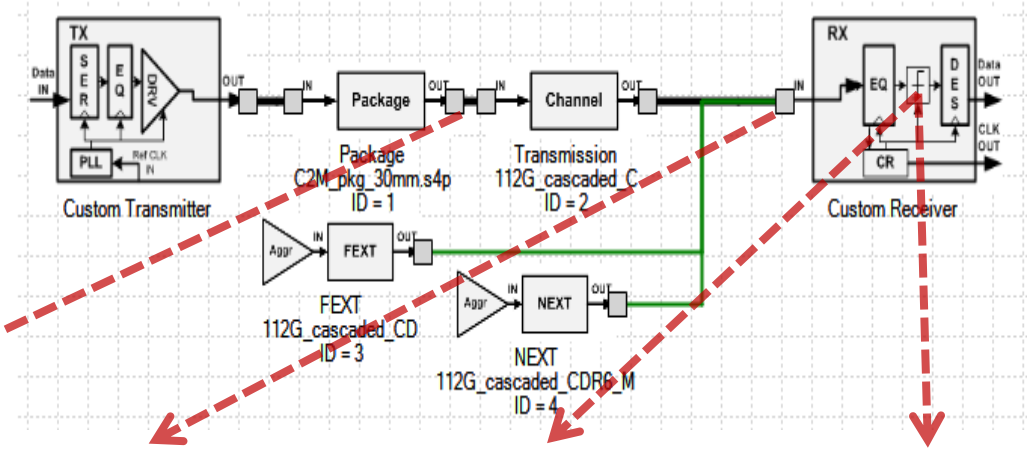
VEO (mV) at BER 10^{-5}

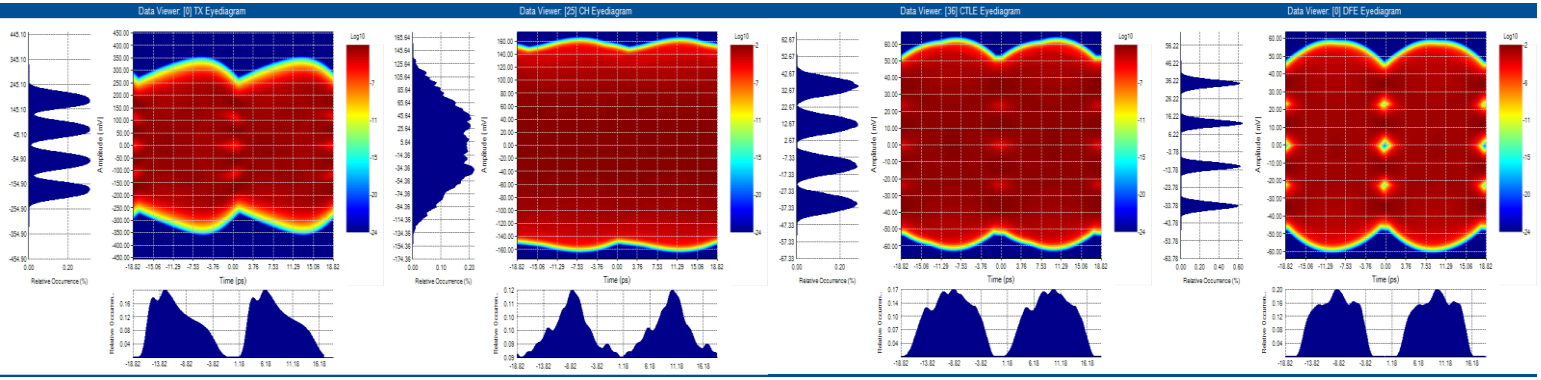
Channel	Description	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH1	112G_16dB_(QSFPDD+module card)_TX7_L10	14.40	8.8571	12.4524	10.1096	11.2927	16.9235	17.6447
CH2	112G_16dB_(QSFPDD+module card)_TX7_L23	14.59	5.513	14.952	8.3231	7.0648	14.8842	12.8339
CH3	112G_16dB_(QSFPDD+module card)_TX3_L10	14.67	7.0343	11.9659	9.6258	9.1439	16.9968	15.0962
CH4	112G_16dB_(QSFPDD+module card)_TX3_L23	14.82	3.761	14.7127	8.0978	5.7352	14.9661	12.6943
CH5	112G_16dB_(QSFPDD+module card)_TX7_Asic	14.76	4.2734	14.67	7.2187	6.1693	15.9815	12.2949
CH6	**112G_16dB_(QSFPDD+module card)_TX3_Asic**	15.01	1.4943	11.0235	7.6592	2.646	15.598	11.3229

CTLE option 2 improves VEO by ~3.3mV over CTLE option 1.

CH6 112G_16dB_(QSFPDD+module card)_TX3_Asic TP1a Simulation

w/ 30mm Host Package and RX CTLE Option 2 + FFE-only (Example shown)





TX Output

CH Output

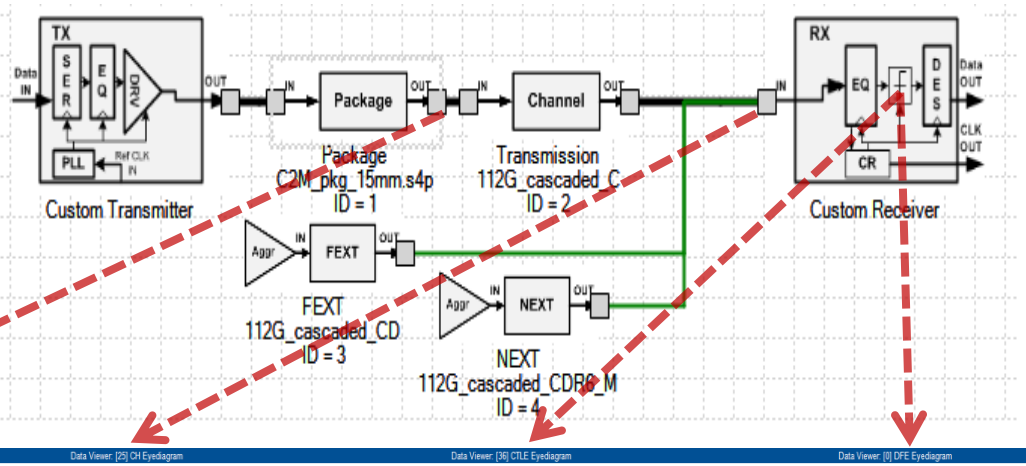
RX CTLE output

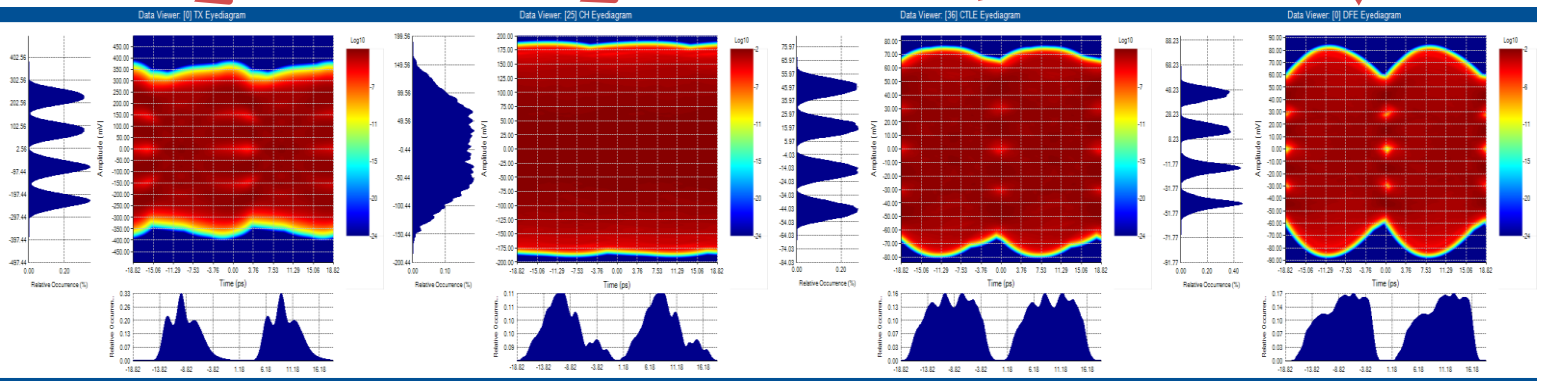
RX FFE output
EH=7.96mV EW=0.14 UI BER=1e-5

BER	EW (UI)	EH (V)
10^-1	0.65100	0.02140
10^-2	0.32800	0.01560
10^-3	0.23600	0.01230
10^-4	0.18200	0.00983
10^-5	0.14400	0.00796
10^-6	0.11300	0.00635
10^-7	0.09080	0.00498
10^-8	0.07230	0.00386
10^-9	0.05470	0.00286
10^-10	0.04000	0.00187
10^-11	0.02640	0.00112
10^-12	0.01370	0.00025

CH6 112G_16dB_(QSFPDD+module card)_TX3_Asic TP1a Simulation

w/ 15mm Host Package and RX CTLE Option 2 + FFE-only (Example shown)





TX Output

CH Output

RX CTLE output

RX FFE output
EH=5.01mV EW=0.06 UI BER=1e-5

BER	EW (UI)	EH (V)
10^-1	0.53000	0.02630
10^-2	0.21000	0.01630
10^-3	0.13100	0.01110
10^-4	0.08980	0.00752
10^-5	0.06150	0.00501
10^-6	0.03710	0.00251
10^-7	0.00000	0.00036
10^-8	0.00000	0.00000
10^-9	0.00000	0.00000
10^-10	0.00000	0.00000
10^-11	0.00000	0.00000
10^-12	0.00000	0.00000

CH6 TP1a Waveform Simulation Results

Eye Height (mV) at BER 10^{-5}

Channel	Parameter (Method)	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH6 + 30mm pkg	VEO (COM)	15.01	5.4724	9.3145	7.0492	7.0979	13.4993	10.6407
	Eye Height (Waveform)	15.01	6.16	8.70	7.00	7.96	13.11	11.59
CH6 + 15mm pkg	VEO (COM)	15.01	1.4943	11.0235	7.6592	2.646	15.598	11.3229
	Eye Height (Waveform)	15.01	3.66	11.93	9.74	5.01	17.69	10.19

Eye Width (UI) at BER 10^{-5}

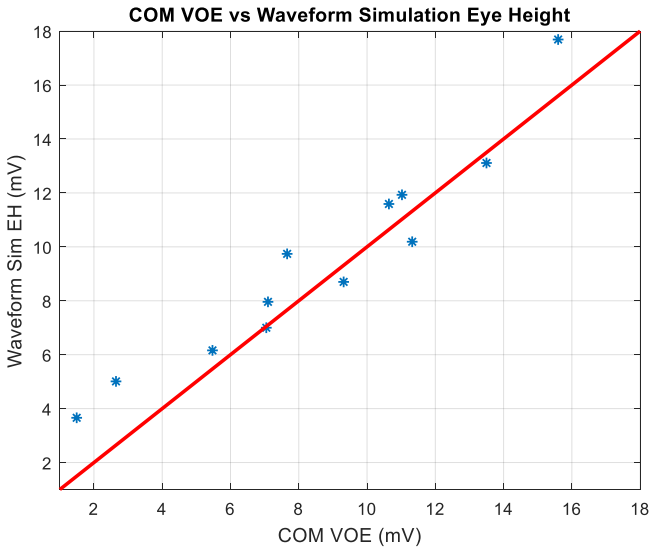
Channel	Parameter (Method)	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH6 + 30mm pkg	n/a (COM)	15.01	n/a	n/a	n/a	n/a	n/a	n/a
	Eye Width (Waveform)	15.01	0.13	0.15	0.13	0.14	0.17	0.16
CH6 + 15mm pkg	n/a (COM)	15.01	n/a	n/a	n/a	n/a	n/a	n/a
	Eye Width (Waveform)	15.01	0.05	0.12	0.11	0.06	0.12	0.1

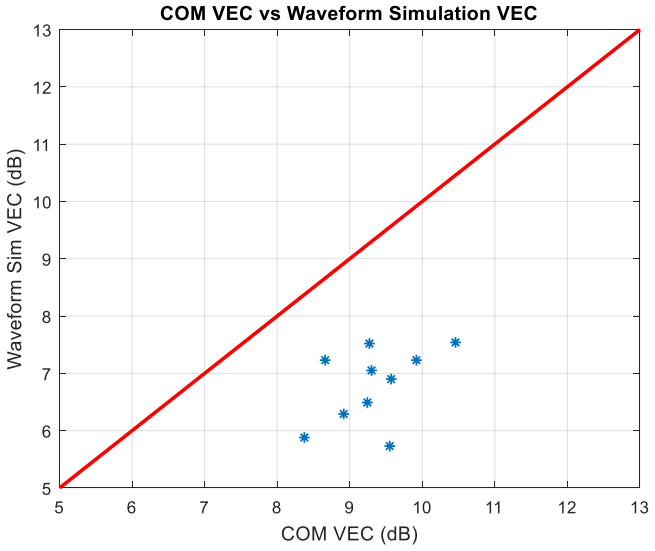
VEC (dB) at BER 10^{-5}

Channel	Parameter (Method)	IL (dB) @ 26.56GHz	CTLE: Option 1 (trending 802.3ck)			CTLE Option 2		
			FFE-only	FFE/DFE1	DFE-only	FFE-only	FFE/DFE1	DFE-only
CH6 + 30mm pkg	VEC (COM)	15.01	10.4576	9.3001	9.2423	9.9193	8.3737	8.9159
	VEC (Waveform)*	15.01	7.54	7.05	6.49	7.23	5.88	6.29
CH6 + 15mm pkg	VEC (COM)	15.01	24.0553	9.572	9.5506	20.5427	8.6609	9.2708
	VEC (Waveform)*	15.01	12.31	6.9	5.73	12.74	7.23	7.52

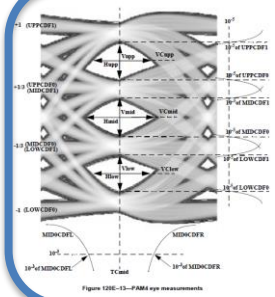
**: Waveform simulation's VEC is measured and calculated based on IEEE 802.3 Annex 120E*

CH6 TP1a COM and Waveform Simulation Results Comparisons





- Observations
  - Good correlation between COM VOE and waveform simulation eye heights
  - COM's VEC is worse than waveform simulations' by *~2-3dB due to:*
    - VEC calculation in COM2.58 does not follow the IEEE 802.3 120E.4.3, EQ (120E-4)



$$VEC = 20\log_{10}\left(\max\left(\frac{AV_{upp}}{V_{upp}}, \frac{AV_{mid}}{V_{mid}}, \frac{AV_{low}}{V_{low}}\right)\right) \text{ (dB} \qquad \text{(120E–4)}$$

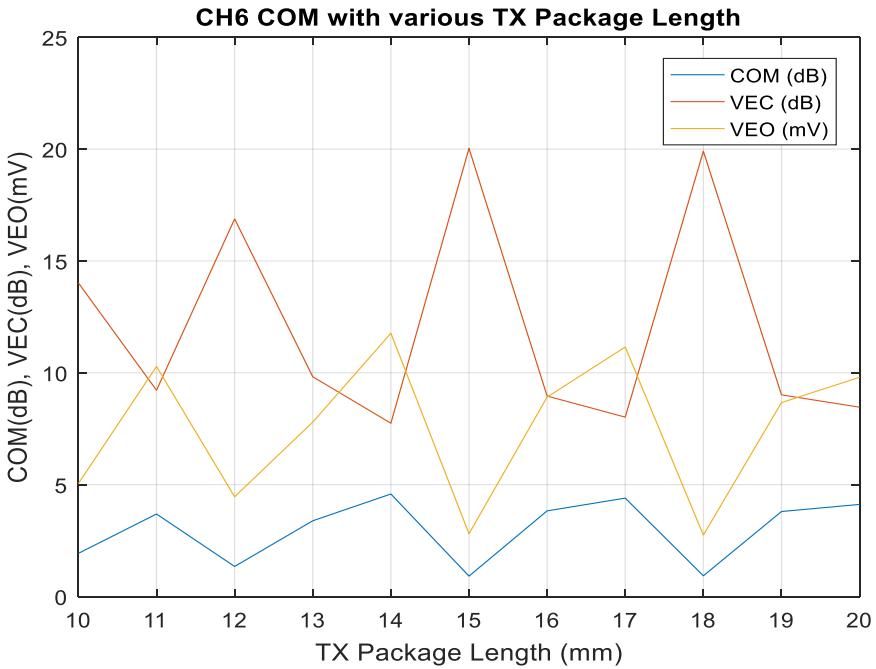
IEEE 802.3 Annex 120E

```
output_args.VEO_normalized = (A_s-A_ni)/A_s;
output_args.VEC_dB = -20*log10(output_args.VEO_normalized);
```

COM 2.58

    - Handling of SNR_{TX}, nonlinearity, and jitter/noise between COM and waveform simulations

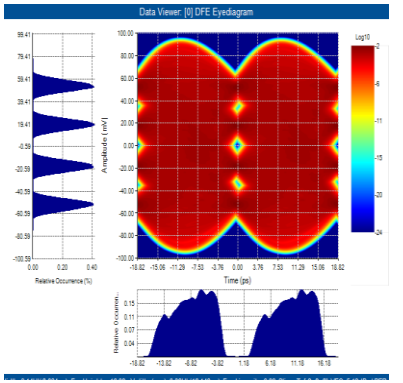
Bad TP1a Results with Short (15mm) Host Package w/ RX FFE-only Configuration



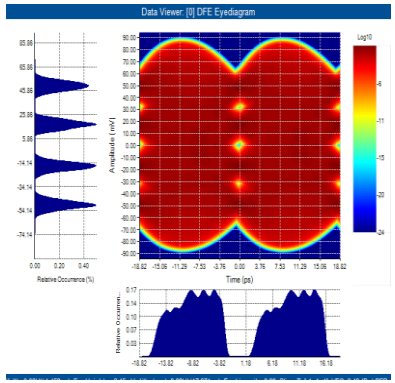
- Observation:
  - TP1a performance varied significantly with short TX Host package length
    - COM varies by ~3.7dB, VEC by ~12dB, VEO by 9mV when TX host package length changes from 10 to 20mm
    - This periodic COM/VEC/VEO variation seems natural
      - Reflection noise is caused between the package ends and is superimposed on the signal
      - Reflection noise amount at sampling time varies depending on the package length

Waveform Simulations with Physical 106/112Gbps Packages

- Two preliminary 106/112Gbps host packages
  - Similar IL and RL characteristics compared with currently trending 15mm host package
- Waveform Simulation Results
  - RX w/ CTLE option 2 + FFE-only configuration
  - Same TP1a simulation settings
  - Simulation results

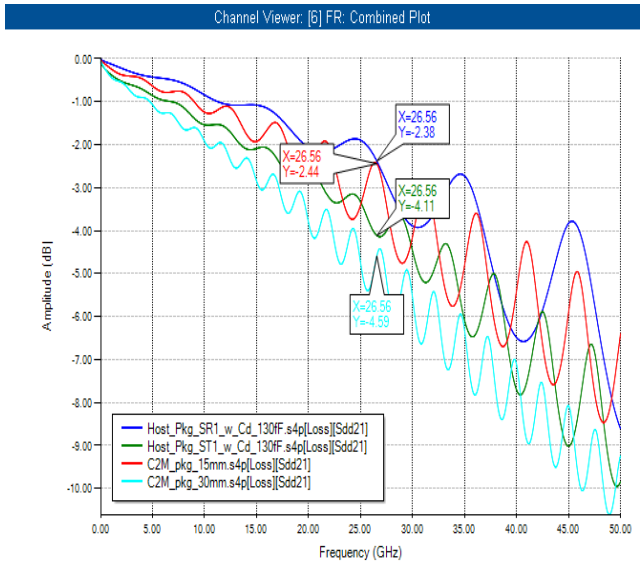


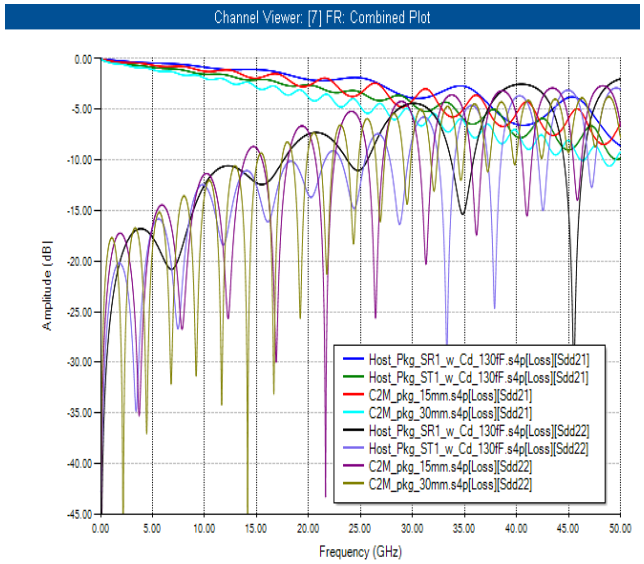
Host SR1 Package : RX FFE output EH=16.1mV EW=0.14 UI BER=1e-5



Host ST1 Package : RX FFE output EH=8.5mV EW=0.08UI BER=1e-5

  - Observed similar EH/EW variation trends as seen in COM analysis





Summary

- When host package is long (30 mm), 5-tap FFE, 4 tap FFE+1 tap DFE, and 4-tap DFE Ref EQs provides solution space with good margin
- When host package is short (15 mm), 4 tap FFE+1 tap DFE, and 4-tap DFE Ref EQs provides good solution space, but 5-tap FFE is challenged
- To improve the solution space for short package with 5-tap FFE Ref EQ
  - Reduce Cd and/or Cp
  - Further improve the performance of the ref CTLE
    - CTLE option 2 performs better than option 1 with the C2M configuration
  - Add 1-tap DFE
- The VEC calculation in the current COM2.58 does not follow the 120E.4.3, EQ (120E-4), needs to be fixed