New Insights on DFE Burst Error Impact for 100G KR/CR FEC

Ilya Lyubomirsky, Jamal Riani, and Sudeep Bhoja, Inphi Corp.

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Summary

- A new interleaved RS(544,514) FEC has been proposed in gustlin_3ck_01_0119 for mitigating potential burst error issues in 100G-KR/CR systems based on multi-tap DFE Rx architectures

- Some analysis has been provided in anslow_3ck_01_0918 showing BER error flaring can occur in multi-tap DFE Rx architectures when DFE taps are sufficiently large, and simulation results showed interleaved FEC may improve performance for some cases considered

- A major disadvantage of interleaved FEC is a significant increase of the FEC latency, as discussed in lyubomirsky_3ck_01a_0119. Moreover, detailed system analysis in lu_3ck_adhoc_01_022719 pointed out additional compatibility and complexity issues.

- As an alternative approach to interleaved FEC, the DFE burst error issue can be mitigated by properly constraining the DFE tap values, as shown in anslow_3ck_01_0119, and proposed in lyubomirsky_3ck_01a_0119

- In this work, we present new analysis on multi-tap DFE burst error effects: 1). showing the importance of accurately computing burst error statistics at each SNR; 2). simulations revealing small penalties on non-interleaved FEC when the DFE tap values are reasonably constrained

Simulation Method

1). We employ a Markov Chain technique to compute DFE burst error patterns and their probabilities (up to a maximum number of PAM4 symbol burst errors = 100 in our sims)

2). Using the results of 1)., compute a list L of Reed-Solomon (RS) symbol error patterns and their probabilities,

$L = \{E_0, E_1, E_2, \ldots, E_M\}$

E_j is an error event of RS symbol span $S(E_j)$ and number of errors $N(E_j)$

(E_0 is a special "zero" event with $S(E_0)=1$ and $N(E_0)=0$)

3). Using the list L and associated probabilities $P(E_j)$, spans $S(E_j)$, and number RS symbol errors $N(E_j)$, solve a recursive equation for $\boldsymbol{\pi(n,i)}$, the probability of i or more RS symbol errors in a block size n. See next slide for more details on this step.

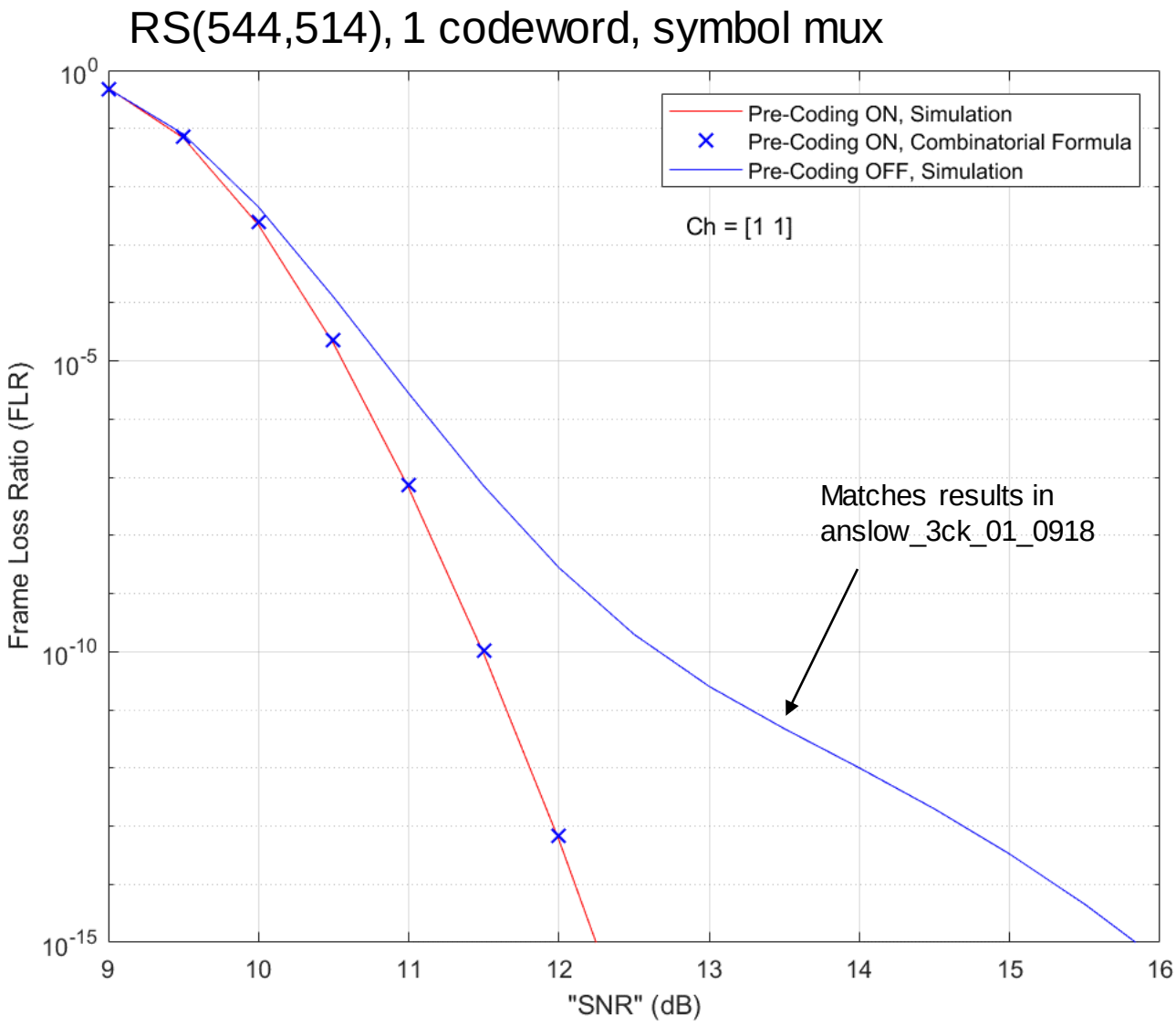
Recursive Equation for π(n,i)

$$\pi(n,i) = \sum_j P(E_j)\ \pi(n - S(E_j), i - N(E_j))$$

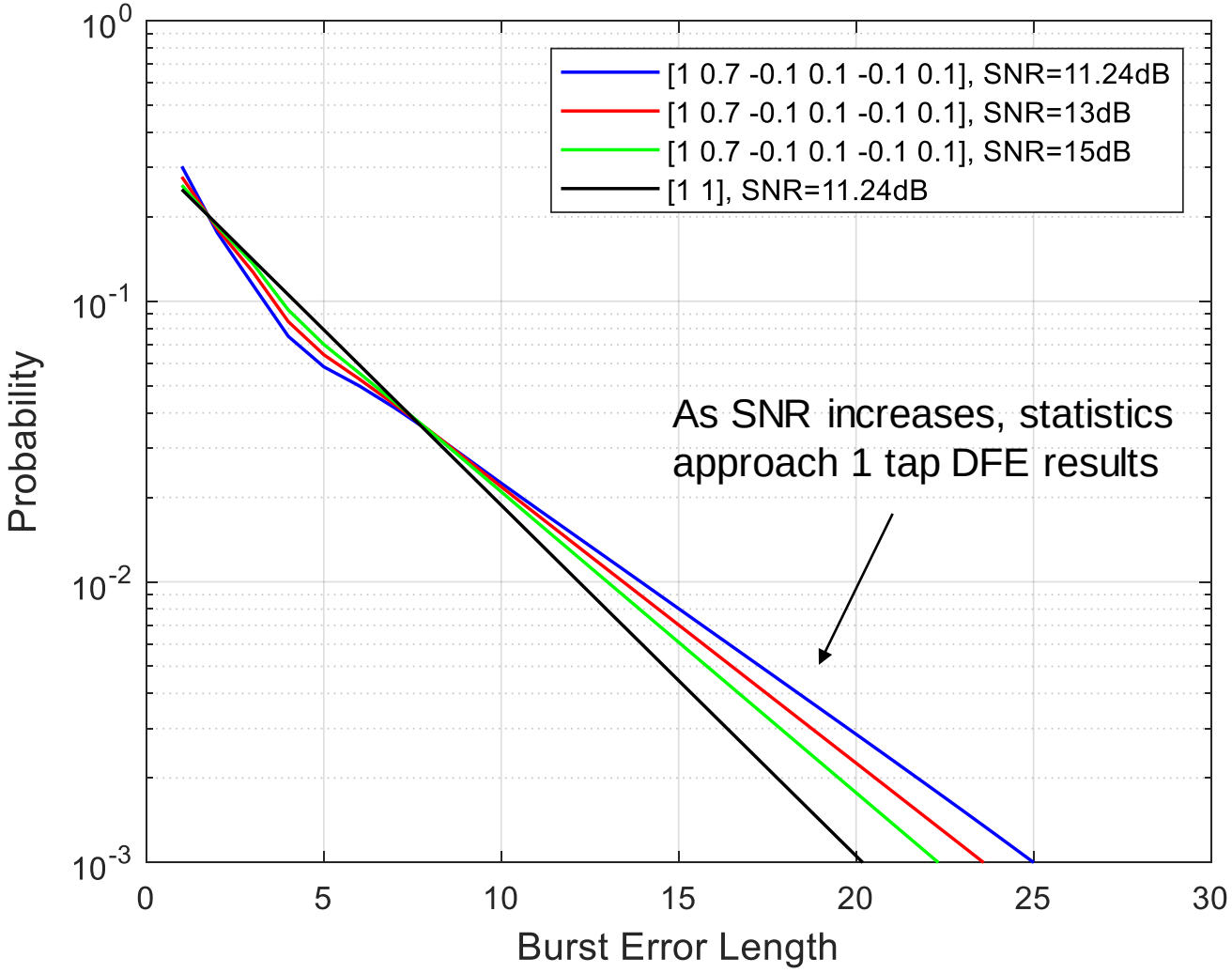
Initial conditions:

$$\pi(1,0) = 1$$
$$\pi(1,1) = \sum_{j \neq 0} P(E_j)$$
$$\pi(1,2{:}end) = 0$$

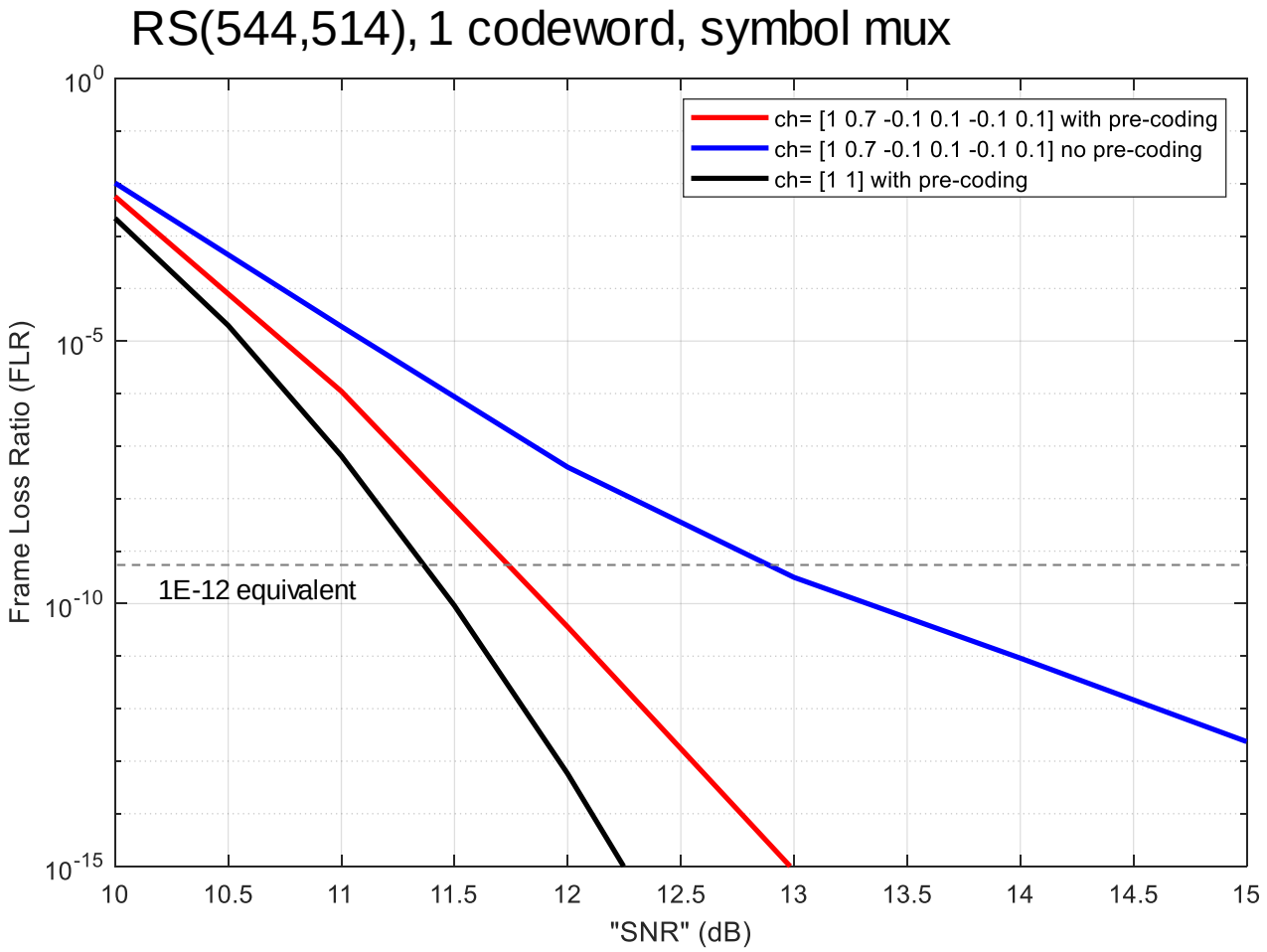
Simulation Results for 1-tap DFE



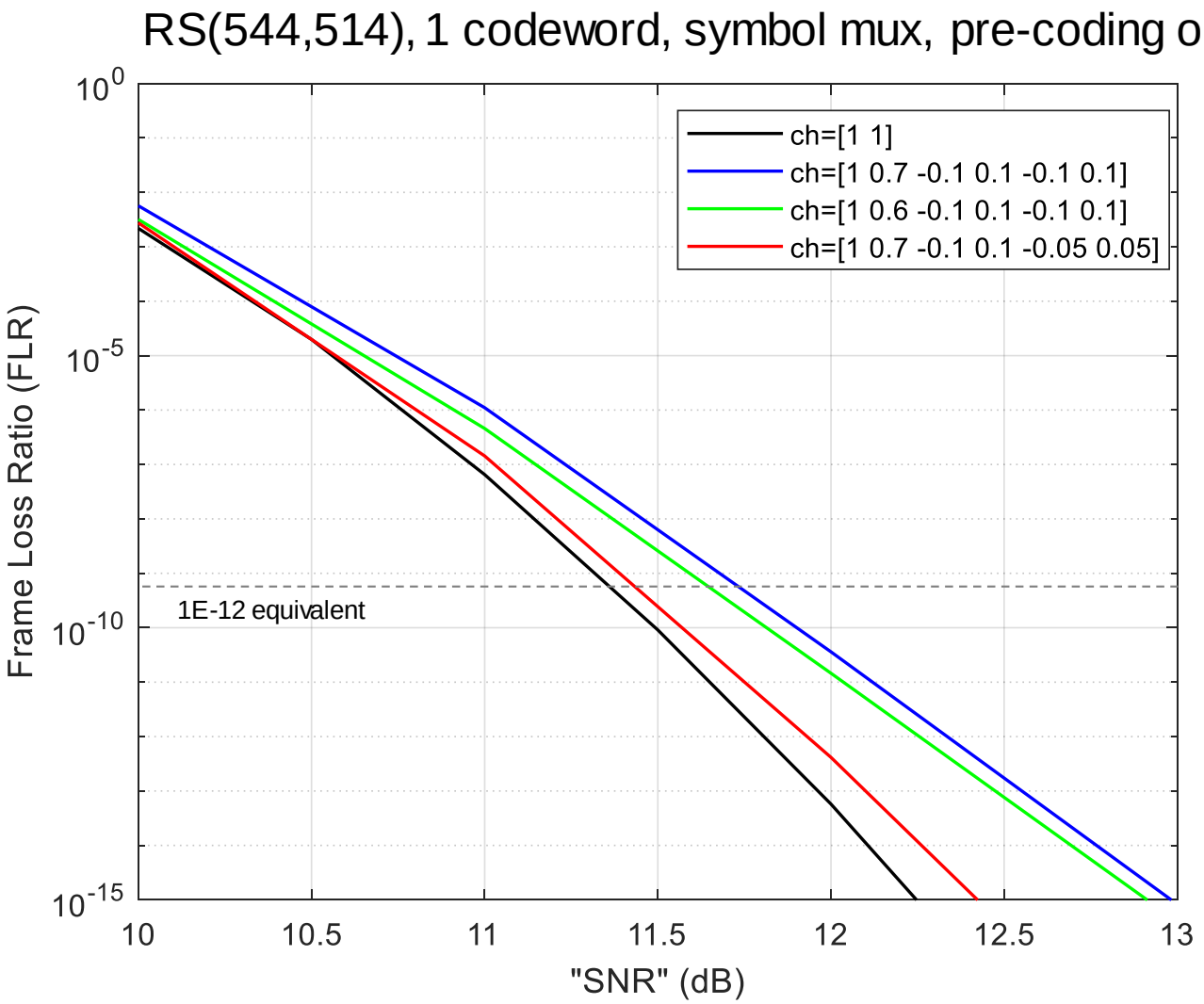
DFE Burst Error Length Statistics vs. SNR



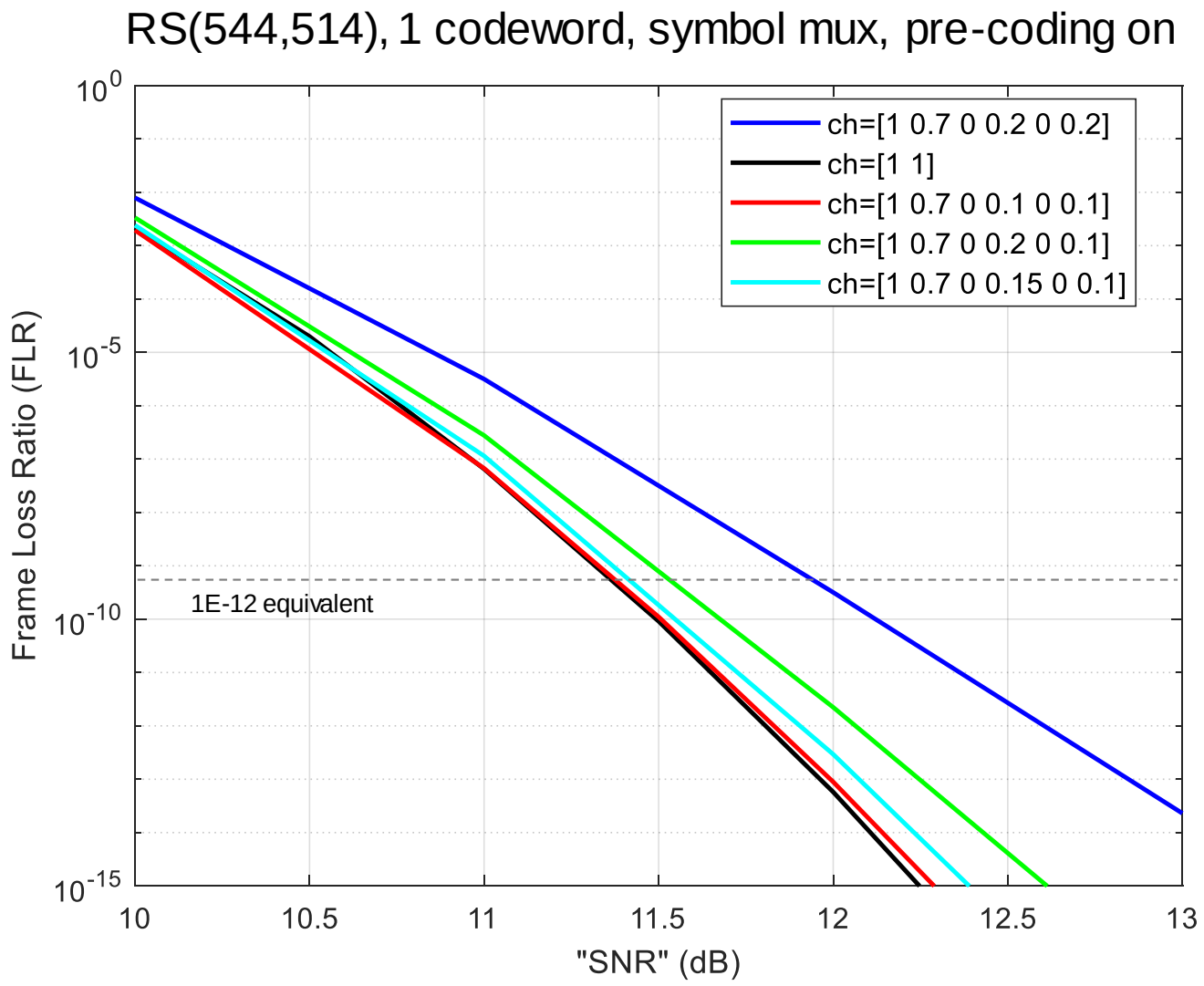
Simulation Results for Multi-Tap DFE [0.7 -0.1 0.1 -0.1 0.1]



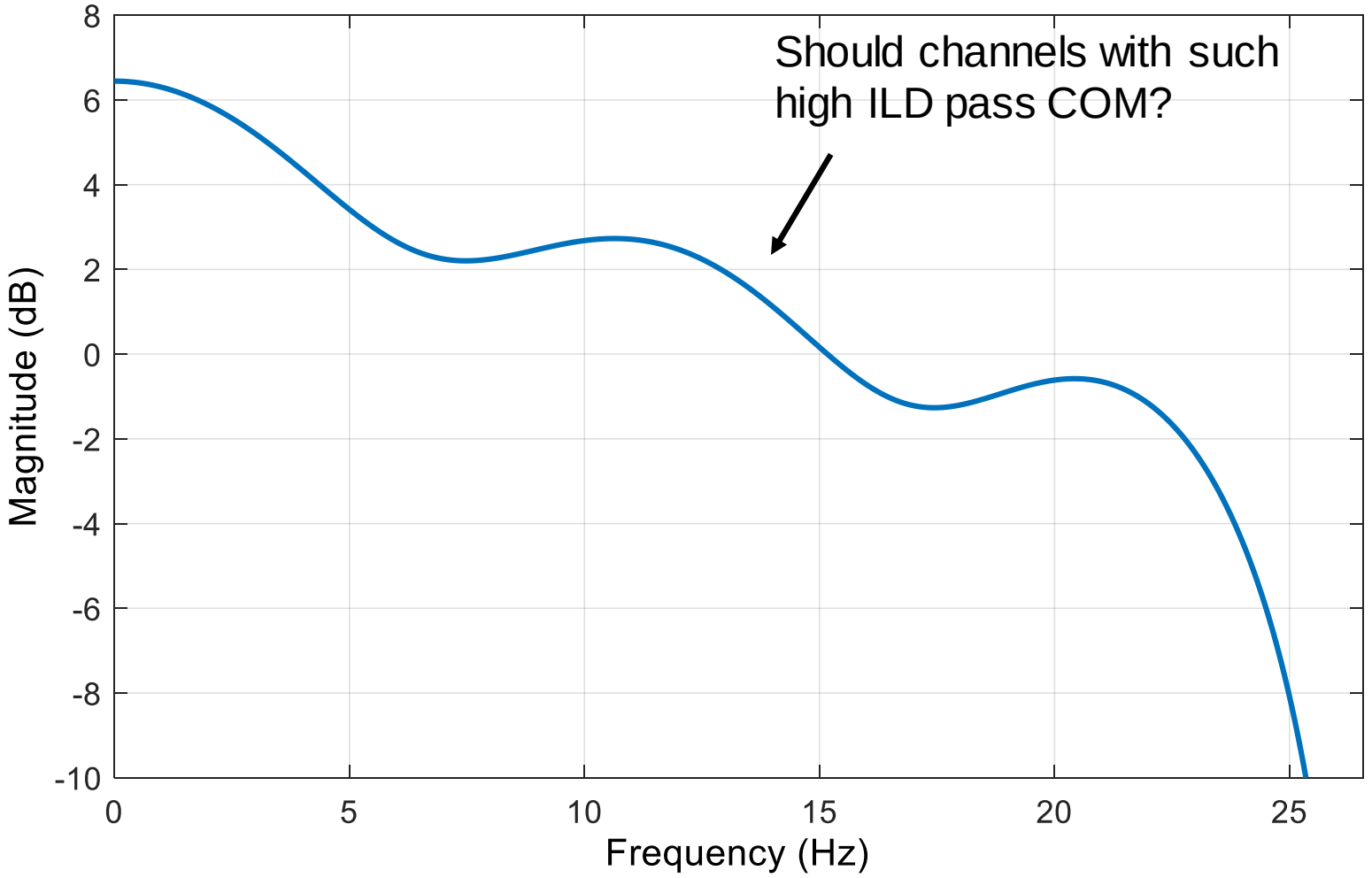
Impact of Reducing DFE Taps



Simulation Results for Multi-Tap DFE [0.7 0 0.2 0 0.2]



Frequency Response for h = [1 0.7 0 0.2 0 0.2]



Conclusions

- We presented new simulation results on the impact of DFE burst errors on non-interleaved RS(544,514) FEC, taking care to re-compute burst error statistics at each SNR value for higher accuracy.

- The simulation results confirm that multi-tap DFE implementations can mitigate the impact of burst errors by properly constraining the tap values. More work is required to determine the optimum tap constrains.

- We recommend not to burden 100G KR/CR system designs with the additional complexity and increased latency of interleaved FEC just to improve performance for some extreme cases of multi-tap DFE Rx implementations. Alternative high performance architectures exist, such as FFE+1-tap DFE.