100GE/200GE/400GE C2M Simulation Update

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Overview

This is to present C2M study results following sun_3ck_01b_0119.
Updates include:

- Package model assumptions
- New channels
- Whole-link simulation
- TP4 simulation
- TP1a simulation
- Reference receiver length sensitivity
- Host/module TX assumptions
- Finalize reference models:
  - A: 4-tap DFE (b1max=0.5)
    - A2: b1max = 0.2
  - B: 5-tap FFE with 1-tap DFE (FFE4post with DFE b1max=0.5)
  - C: 5-tap FFE (FFE4post)
  - D: 4-tap DFE (b1max reduced from 0.1 to 0.0. Only three DFE taps.)
- Simulations are done with COM tool v260.

Package Assumption

- The following module package is used for whole link and TP4 analysis.

C_d	0.85e-4	nF
C_p	0.65e-4	nF
Package trace length Z_p	2-10	mm
Package PTH	0	mm
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

- Host package loss characteristics is the same as for KR/CR. Cd=130fF and 110fF are studied.

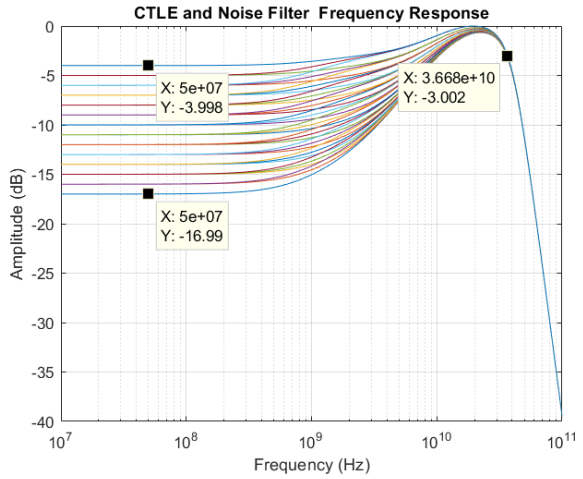
Straw poll #2

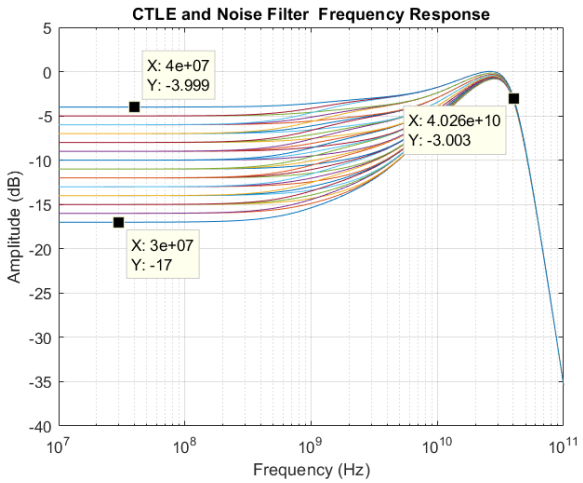
I would support using the following reference package model for the development of KR/CR/C2M-hostside COM baseline proposals:

- Slide 8 of benartsi_3ck_01_0119
- with Cd changed to TBD

Yes: 41 No: 0 Abstain: 13

CTLE Curves





CTLE and Noise Filter for Receivers A, A2, and B		
f_r	0.75	*fb
g_DC	[-14:1:-3]	dB
f_z	12.58	GHz
f_p1	20	GHz
f_p2	28	GHz
g_DC_HP	[-3:1:-1]	dB
f_HP_PZ	1.328125	GHz

CTLE and Noise Filter for Receivers C and D		
f_r	0.75	*fb
g_DC	[-14:1:-3]	dB
f_z	18.88	GHz
f_p1	28	GHz
f_p2	53.125	GHz
g_DC_HP	[-3:1:-1]	dB
f_HP_PZ	1.328125	GHz

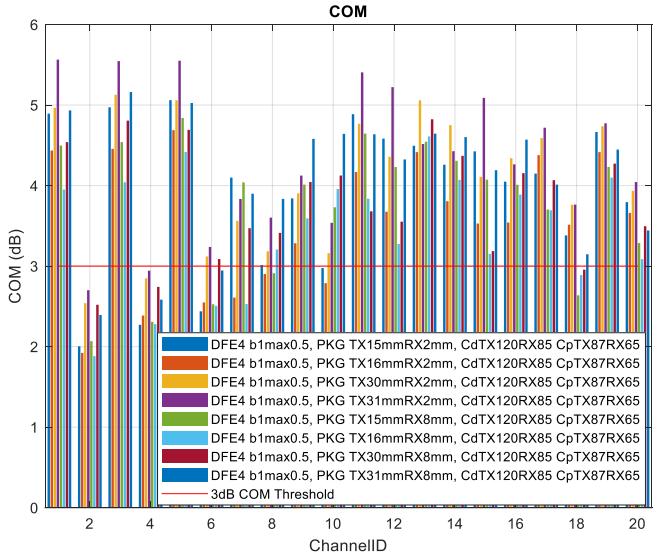
- CTLE bandwidth is lower for receivers with higher b1max.

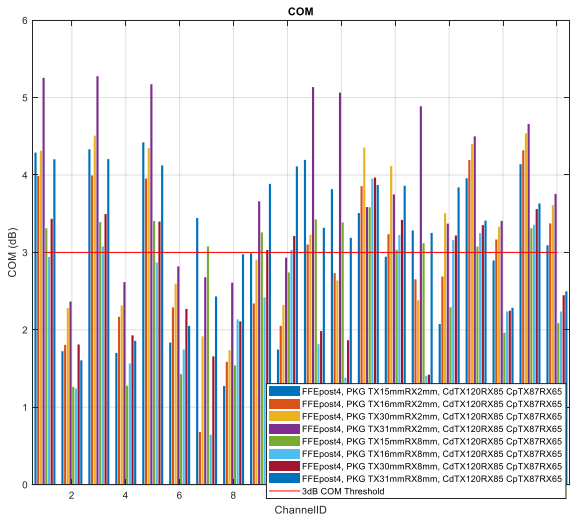
Channels Under Test

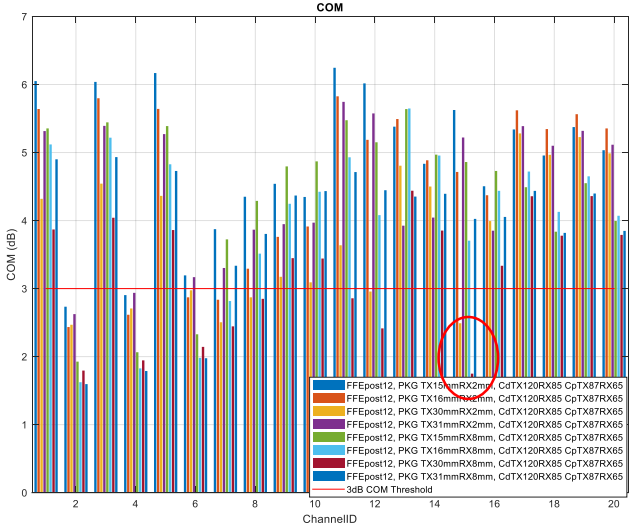
Channel ID	Channel Description	Insertion Loss at 26.5625GHz (dB)	ERL11* (dB)	ERL22* (dB)	ICN (mV)
1	mellitz_3ck_01_0518_C2M\9dB	8.95	16.35	9.82	2.28
2	mellitz_3ck_01_0518_C2M\10dB	9.96	7.84	6.35	4.53
3	mellitz_3ck_01_0518_C2M\11dB	11.16	18.29	10.11	1.93
4	mellitz_3ck_01_0518_C2M\12dB	12.18	8.50	6.78	3.99
5	mellitz_3ck_01_0518_C2M\13dB	13.12	20.09	10.94	1.68
6	mellitz_3ck_01_0518_C2M\14dB	13.87	8.86	7.41	3.19
7	tracy_100GEL_02_0118\long_barrel_via\TX5	16.48	15.00	7.65	0.91
8	tracy_100GEL_02_0118\long_barrel_via\TX6	16.08	14.36	9.12	0.90
9	tracy_100GEL_06_0118\Microvia\RX6	14.59	15.72	7.95	0.83
10	tracy_100GEL_06_0118\Microvia\RX5	14.57	16.22	9.03	0.93
11	lim_3ck_01_0319_QDD_new_pad\ch1	14.40	15.95	9.84	0.78
12	lim_3ck_01_0319_QDD_new_pad\ch2	14.60	14.65	9.74	0.82
13	lim_3ck_01_0319_QDD_legacy_pad\ch3	14.69	16.16	10.44	0.77
14	llim_3ck_01_0319_QDD_legacy_pad\ch4	14.84	14.92	10.34	0.86
15	llim_3ck_01_0319_QDD_new_pad\ch5	14.77	14.96	9.79	1.42
16	llim_3ck_01_0319_QDD_legacy_pad\ch6	15.02	15.28	10.42	1.55
17	ito_3ck_01\QSFP \bottom normal\	15.10	13.02	9.22	1.20
18	ito_3ck_01\QSFP \bottom worst\	15.58	12.71	8.09	1.14
19	ito_3ck_01\QSFP \top normal\	14.53	12.99	9.29	1.25
20	ito_3ck_01\QSFP \top worst\	14.49	12.65	8.04	1.21

- Parameters highlighted in red are worse than 9dB ERL, or 2.5mV ICN. Improvement is recommended.
- ERL is reported with the settings for reference receiver with 4-tap DFE at TP1a. ERL22 includes TX package.
- Channel 2, 4, 6, 7, 8 (channel names highlighted) cannot be supported by DFE4 and FFE12post, assuming 130fF host Cd.

Whole-Link Simulation, Cd=120fF

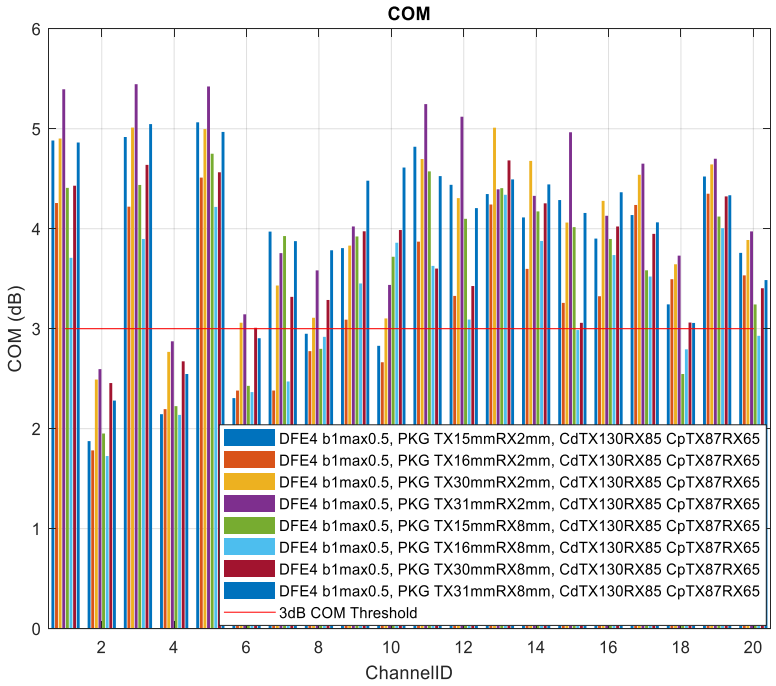


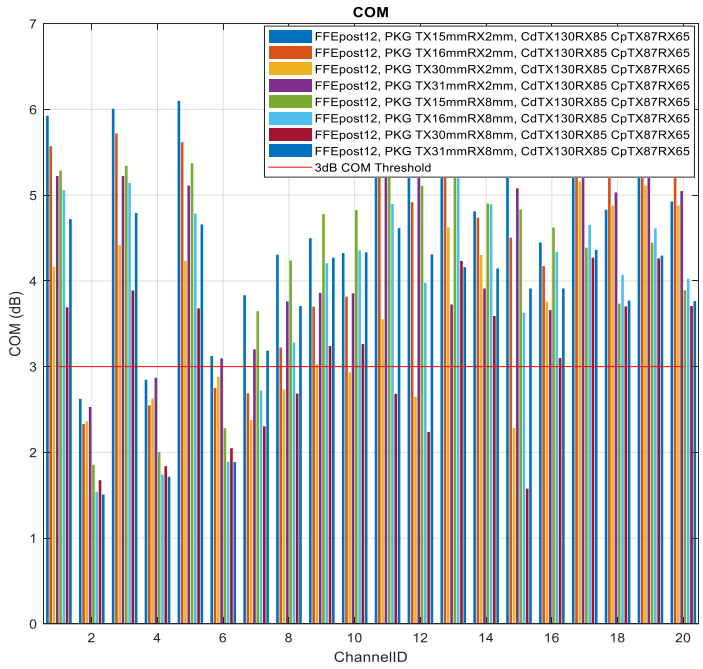




- 5-tap FFE is too weak for whole-link simulation.
- Some channels, e.g. ch15, has very low COM with 12-tap FFE. This dip does not happen to DFE4.
- DFE4 supports the most channels.
- Channel 2, 4, 6, 7, 8 can not pass both DFE4 with b1max0.5 and 12 post tap FFE.

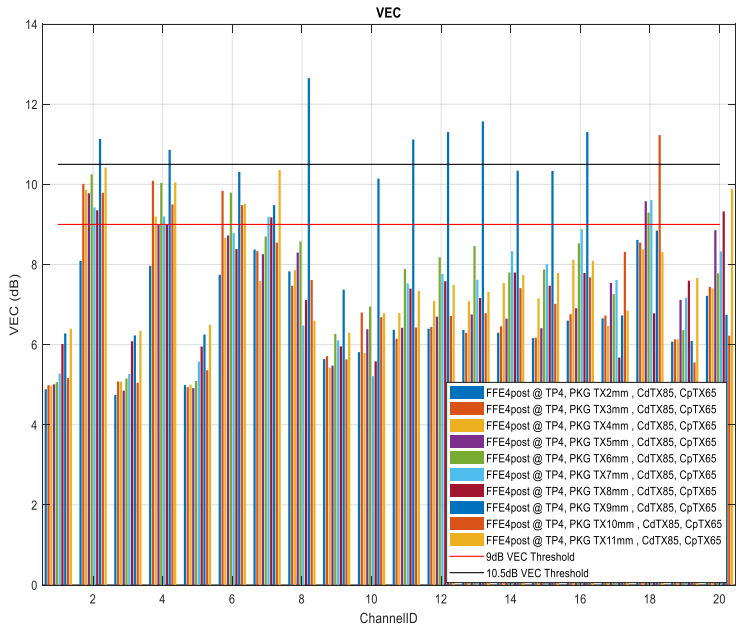
Whole-Link Simulation, Cd=130fF

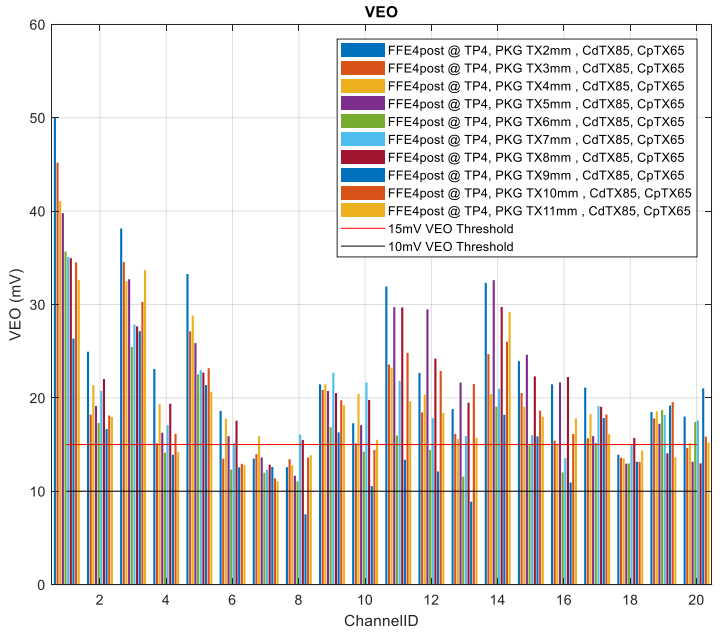




- Channels 2, 4, 6, 7, 8, 10 fail both receivers.

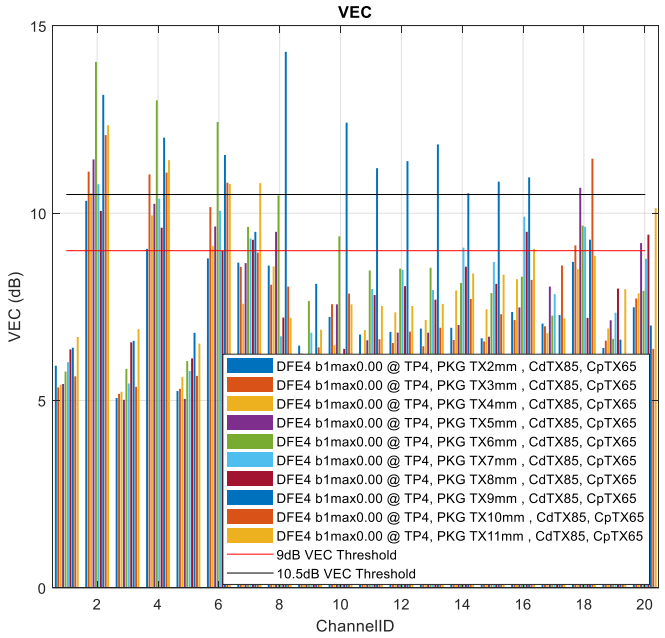
TP4 Simulation Results with Receiver C

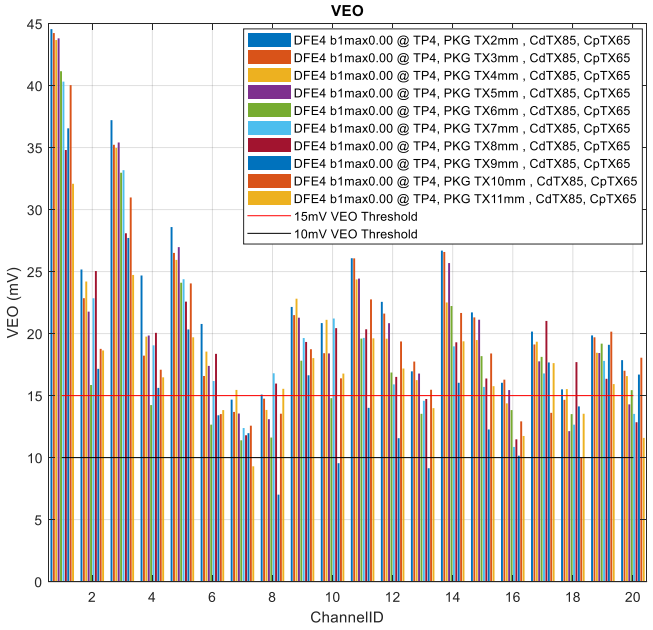




- Package traces between 2-11 mm are simulated.
- 9mm is beyond equalizer length and often has dramatically VEC degradation.
- All channels pass if module package is less than 8 mm.

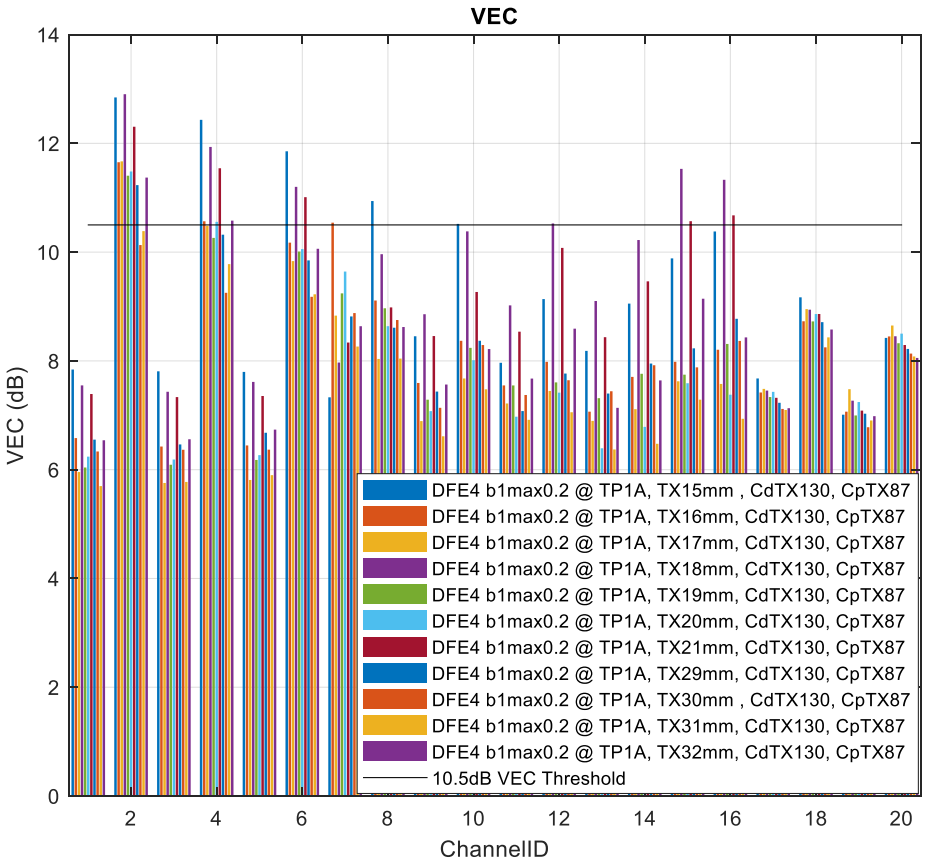
TP4 Simulation Results with Receiver D





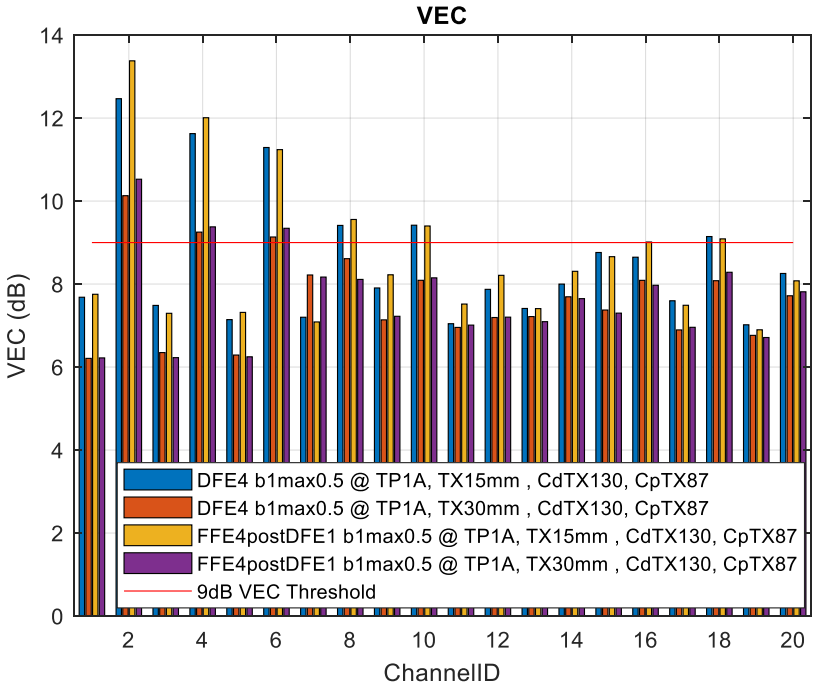
- Package traces between 2-11 mm are simulated.
- All channels pass if module package is less than 8 mm.

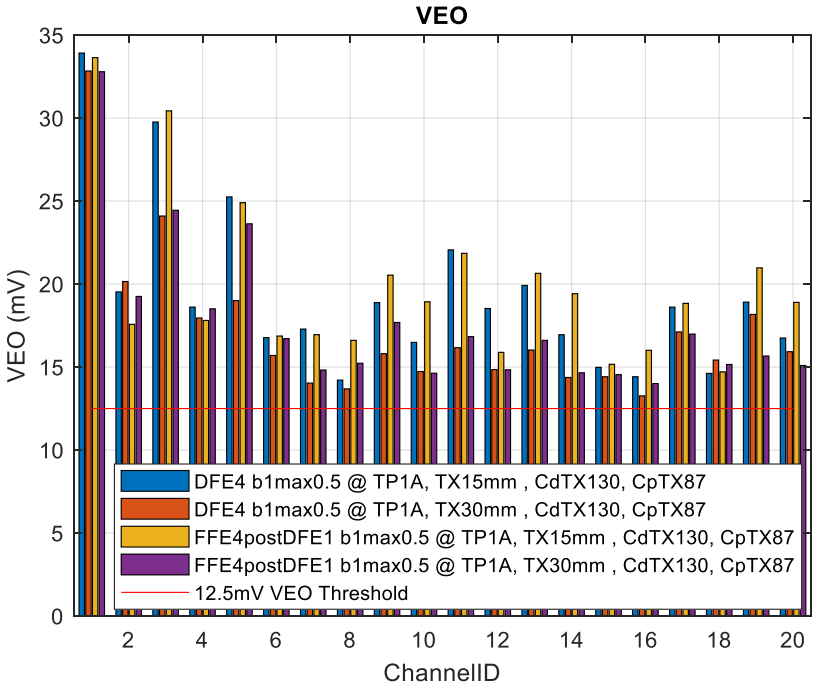
Host Package Length Sensitivity @ TP1a



- VEC spike occurs at package trace lengths 15mm, 18mm, etc.
- Receiver here is A2. If b1max=0.35, only channel #2, #4, #6 fail with host Cd 130fF and worst case package length.

TP1A Simulation with Receiver A and B, Host Cd 130fF

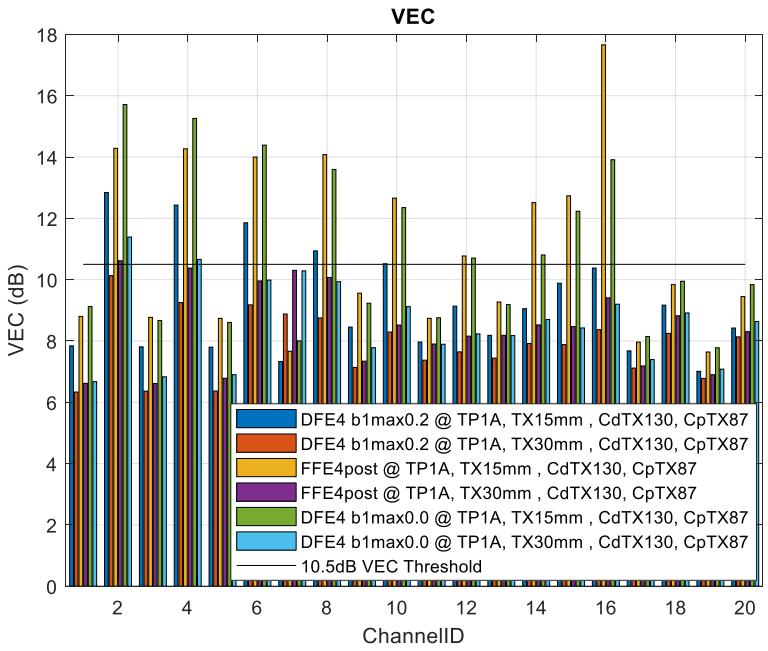


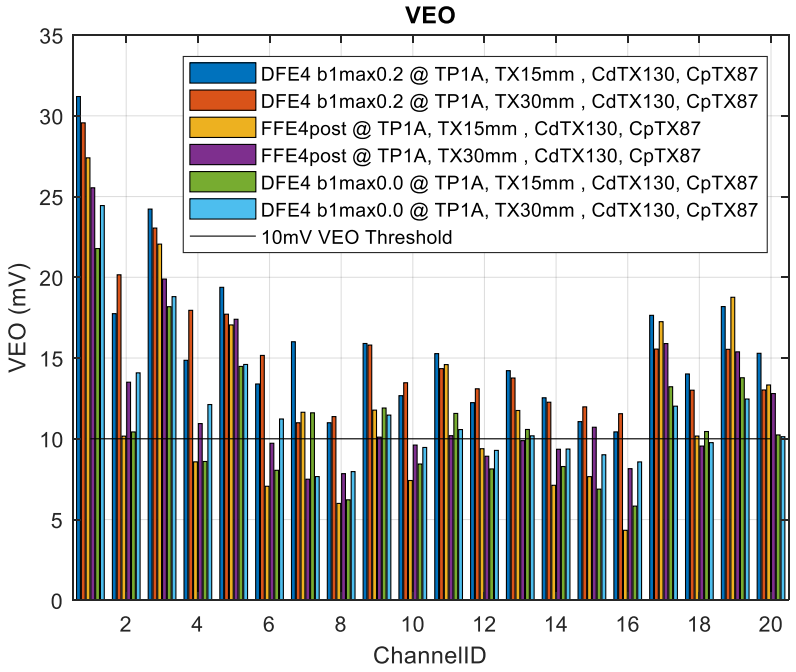


TP1a Criteria	Reference Receiver	VEC Threshold	VEO Threshold	Channels Failed
1	A, B	9dB	12.5mV	2, 4, 6, 8, 10, 18

- VEC threshold is set to 9dB.
- VEO threshold is set to 15mV.
- Receiver A and B have very similar performance.

TP1A Simulation with Receiver A2, C, D, host Cd 130fF



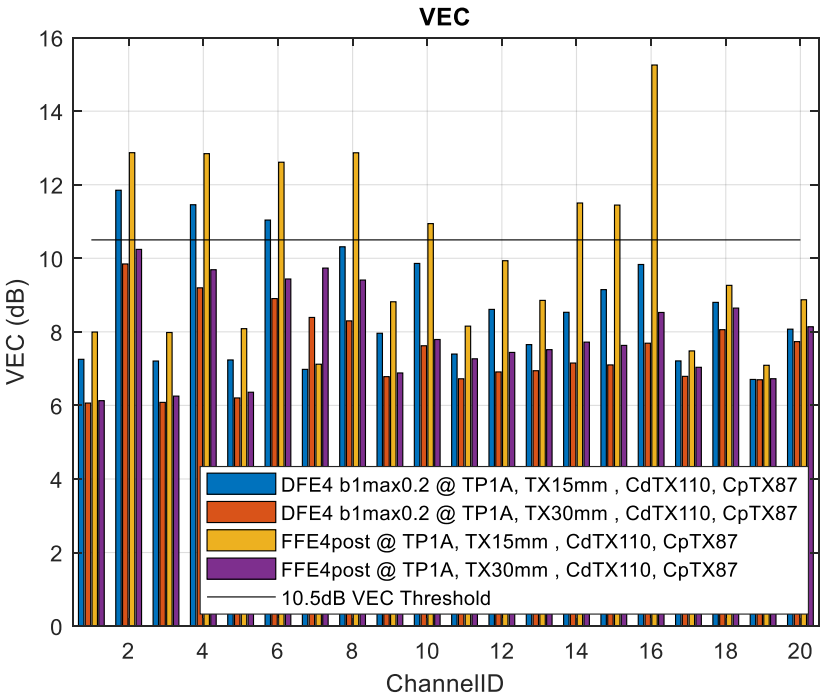


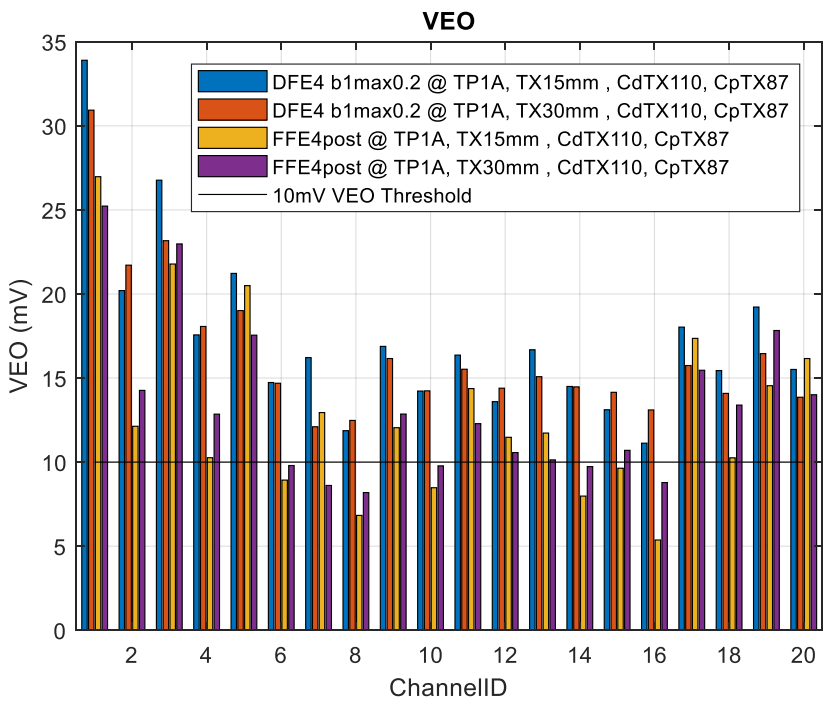
Possible TP1a Criteria	Reference Receiver	VEC Threshold	VEO Threshold	Channels Failed
1	A2	10.5dB	10mV	2, 4, 6, 8, 10
2	C, D	10.5dB	10mV	2, 4, 6, 8, 10, 12, 14, 15, 16, 18

- More channels fail with criteria #2.
- 10 channels fail with receivers C and D.
- VEC spike for receiver C with channel 16 is because of a reflection on post 5. Channel #16 is not so bad for whole-link simulation. Need to investigate the FFE algorithms.
- Receiver C and D pass/fail the same channels. Average VEC difference is within 0.16dB for 20 channels.

Receiver	C	C	D	D
Package	15mm	15mm	30mm	30mm
Average VEC	10.97	10.81	8.45	8.61

TP1A Simulation with Receiver A2, C, host Cd 110fF

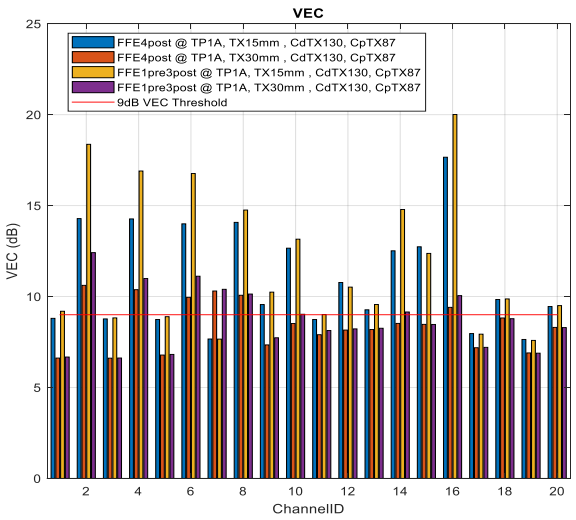


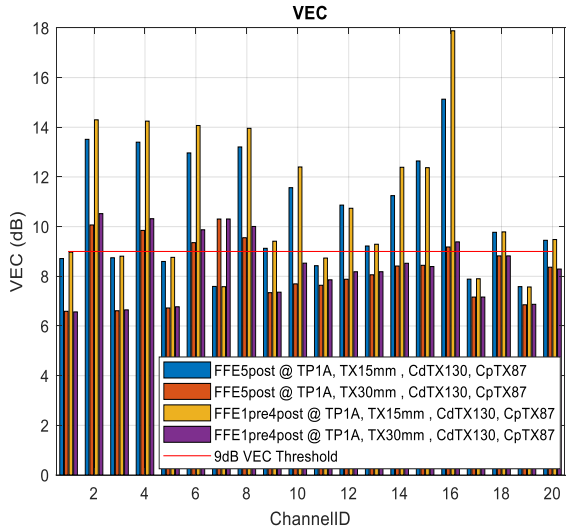


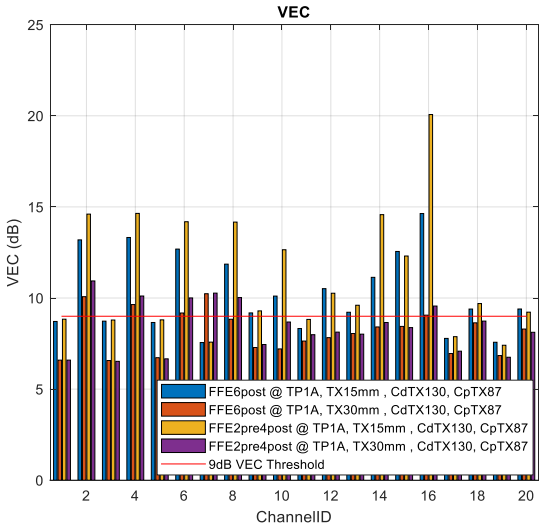
Possible TP1a Criteria	Reference Receiver	VEC Threshold	VEO Threshold	Channels Failed
1	A2	10.5dB	10mV	2, 4, 6
2	C	10.5dB	10mV	2, 4, 6, 8, 10, 14, 15, 16

- If Cd=110fF, there are still 8 channels fail with receiver C.

Receiver Length Sensitivity

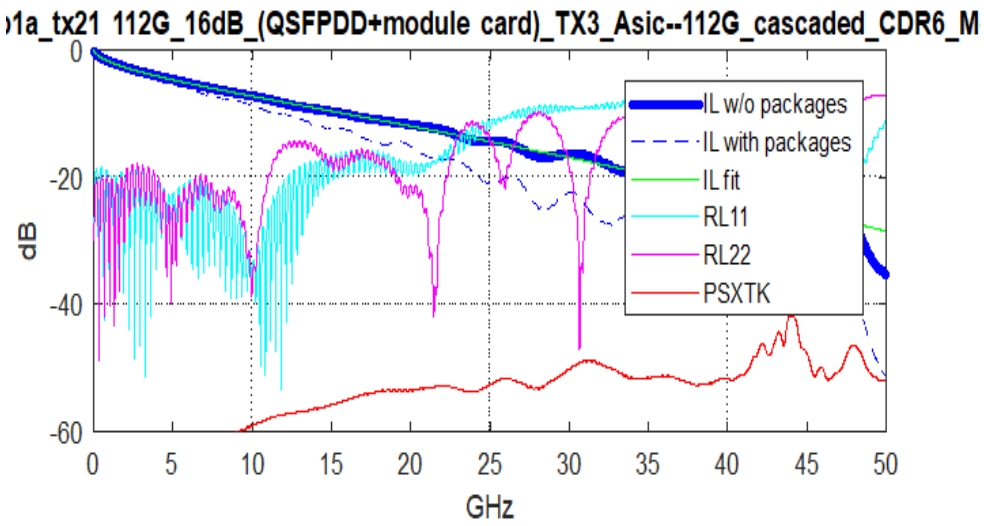


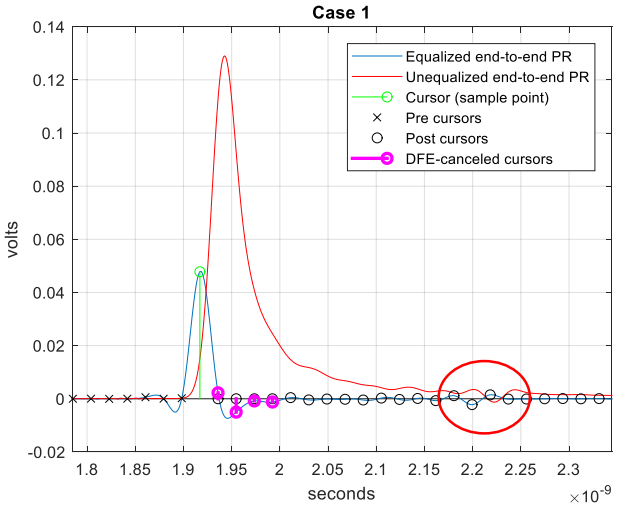


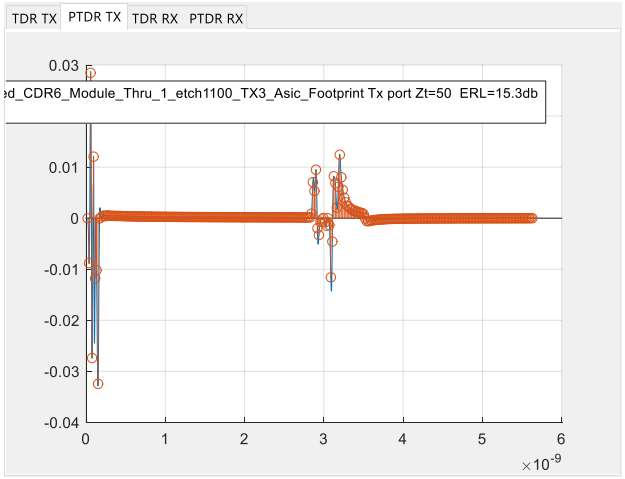


- Extra 1-2 taps do not help much in general. Only very few channels have VEC improvement. More study is needed whether these channels can be improved.
- Post-cursors help performance more than precursors.

Channel Analysis

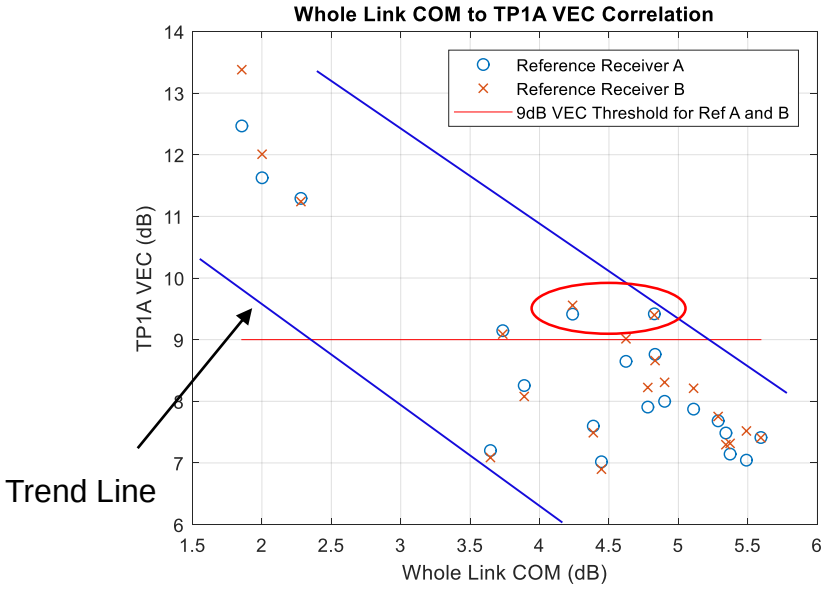


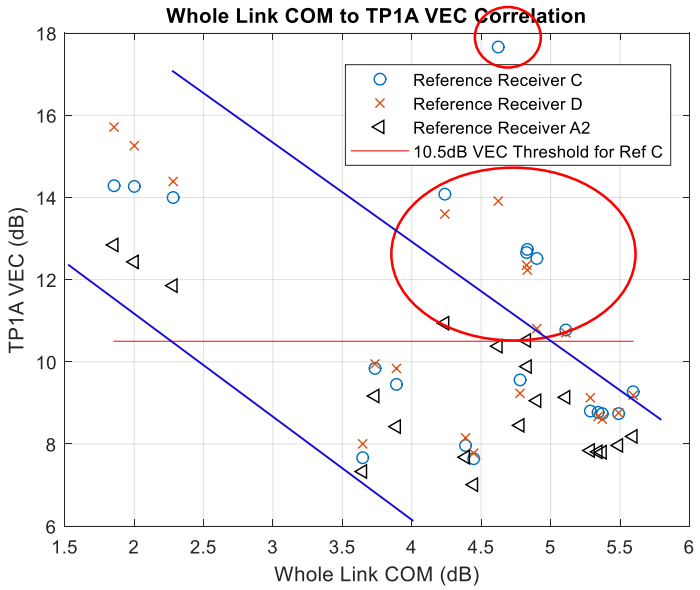




- TP1a simulation.
- Channel 16 with 21mm host package.
- Big reflections observed on tap 16.

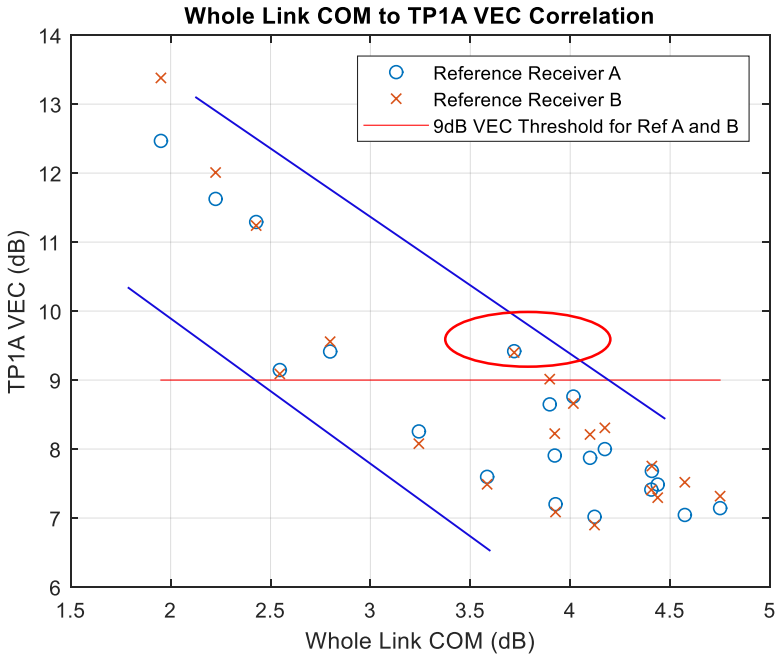
TP1a VEC Correlation to Whole-link COM

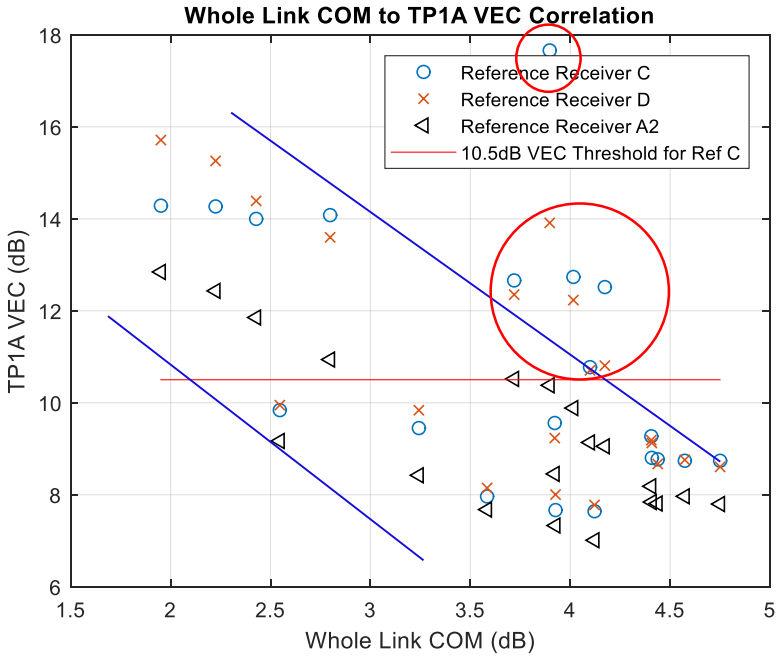




- With 15mm host and 8mm RX package. Whole-link receiver is FFE12 post.
- VEC Threshold for receiver A and B is 9dB, VEC threshold for A2, C, and D is 10.5dB .
- Mismatches are highlighted in red circles.
- A, A2, B have better correlation than C, D. C has the worst correlation. (see the red circle on the right figure!)
- sun_3ck_01b_0119 shows VEO has bad correlation to Whole-link COM. Better to use VEC.

TP1a VEC Correlation to Whole-link COM



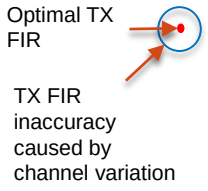


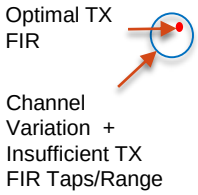
- Whole-link simulation is with 15mm host and 8mm RX package. Whole-link receiver is DFE4 with b1max=0.5.
- A and B have one mismatch. A2 has no mismatch.
- C has the worst correlation. One point is totally uncorrelated.

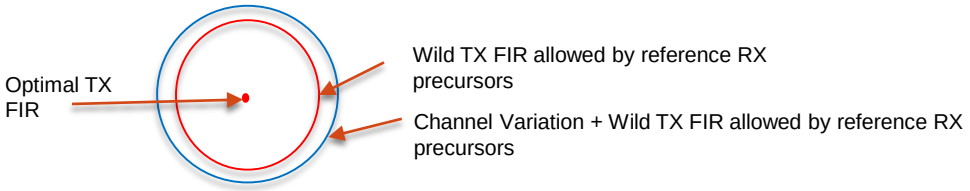
Reference v.s. Real Receivers

- Reference receiver is defined at TP1a without package, while Real receiver has to cover the whole link.
  - Reference receiver could use a real receiver architecture and set higher COM threshold.
  - Another way is to use a minimum performance receiver to qualify channel and signal quality at test points.
  - It is important to have correlation between reference receiver at TP1a and signal quality for the whole link.

- Shorter reference receiver usually allows simpler and broader implementations.
  - A long reference EQ forces real receiver to have long FFE/DFE to cover reflections covered by reference equalizer.
  - A reference EQ with unnecessary precursors allows wild TX FIR range. This forces real receiver to have even more precursors with wide range which are high cost for some real receivers.
    - TX FIR inaccuracy cannot be solved by a reference receiver with precursors. Instead real receiver has to tolerate wild range allowed by reference receiver precursors on top of TX FIR inaccuracy.
    - Tolerate TX FIR inaccuracy should be tolerated by a real receiver stronger than reference receiver.





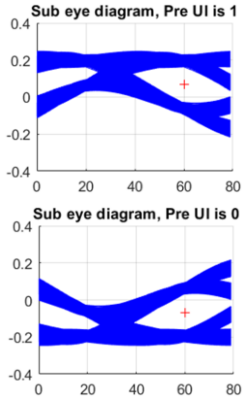


Receiver A and B

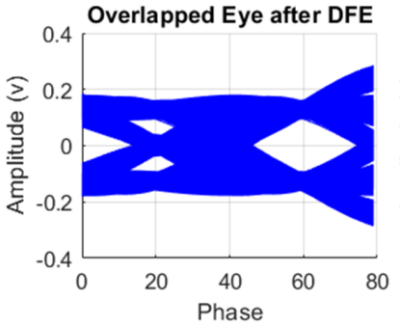
- Implementation wise A is DFE feedback. B is FFE pulse 1-tap DFE. As mathematical reference models, receiver A and B have similar performance.
- Receiver A works well with simple algorithms documented in Annex93A.
- Because DFE and FFE taps are overlapped, its adaptation depends on proper noise. New algorithms need to be documented. Existing Annex 93A and COM tool uses ZF algorithm which is good for DFE.

Eye Diagram of DFE Receivers

- DFE is equivalent to slice input signal at multiple reference levels controlled by prior symbols.
- Eye diagram with DFE is constructed simply by aligning these reference levels.

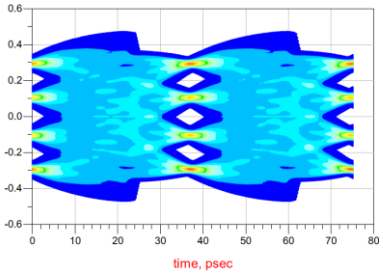


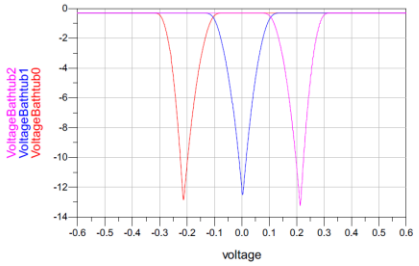
Align reference levels

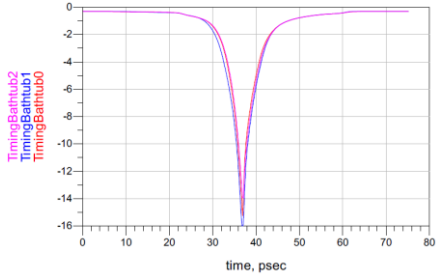


Eye Diagram with DFE (This example is with NRZ signaling for simplicity.)

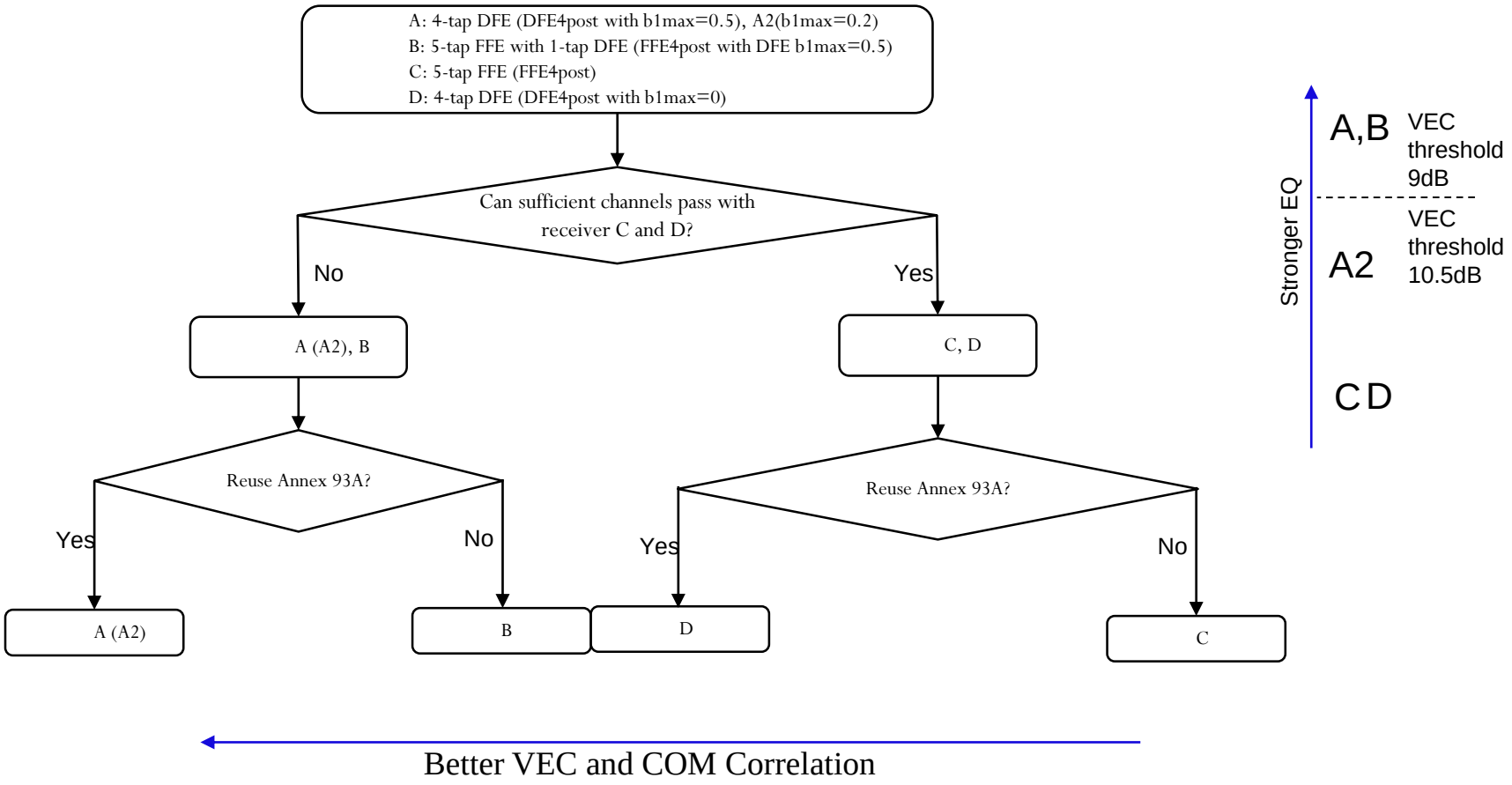
- Eye high, eye width, and bathtub with DFE receivers are commonly used. For example, SERDES AMI model.







Reference Receiver Decision Tree



- B can have tighter b1max as well. More work is needed to figure out exact settings.

Conclusions

- Receivers A and B have very similar performance. Receiver A has only DFE and is easier to specify.
  - Receiver A2 is created to demonstrate b1max can be tightened to 0.2 as a TP1a reference receiver.

- If channels/packages cannot be aggressively improved, Receivers C (FFE4post) and D (DFEb1max0.0) are too weak as TP1a reference receivers. Relaxing VEC is a bad idea as bad channels will pass.

- VEC is correlated to whole link COM. COM is better correlated to VEC with receivers A/A2/B than D than C.

- VEC threshold 9dB is recommended for receiver A and B; 10.5dB is recommended for receiver A2, C, and D.

- Eye height, eye width can be calculated for all four receivers.

- A real receiver is expected to create enough margin in its own way to tolerate additional impairment from module package and channel variation.

Thanks!

Backup Slides

COM Configuration for TP1a Simulation

Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.3e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[2]		[test cases to run]		Port Order	[1 3 2 4]			Table 92–12 parameters		
z_p (TX)	[15 32; 1.8 1.8]	mm	[test cases]		RUNTAG	C2M_1218			Parameter	Setting	
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (FEXT)	[15 32; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]		COM Pass threshold	3.8	dB		board_Z_c	90	Ohm
C_p	[0.87e-4 0]	nF	[TX RX]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	119	mm
R_d	[45 50]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	119	mm
A_fe	0.41	V			Include PCB	0	logical				
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.6		min		N	300					
c(-1)	[-0.3:0.02:0]		[min:step:max]		TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(-3)	[-0.04:.02:0.0]		[min:step:max]		rho_x	0.3					
c(1)	[-0.1:0.05:0]		[min:step:max]		fixture delay time	0					
N_b	4	UI			Receiver testing						
b_max(1)	0.2				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]								
f_z	12.58	GHz			Noise, jitter						
f_p1	20	GHz			sigma_RJ	0.01	UI				
f_p2	28	GHz			A_DD	0.02	UI				
g_DC_HP	[-3.:1:0]		[min:step:max]		eta_0	8.20E-09	V^2/GHz				
f_HP_PZ	1.328125	GHz			SNR_TX	32.5	dB				
					R_LM	0.95					

- This spread sheet is for TP1a simulation with reference receiver A2

COM Configuration for TP4 Simulation

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[0.85e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[1]		[test cases to run]		Port Order	[2 4 1 3]			Table 92–12 parameters		
z_p (TX)	[2 10 ; 0 0]	mm	[test cases]		RUNTAG	C2M_1119			Parameter	Setting	
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (FEXT)	[2 10 ; 0 0]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
C_p	[0.65e-4 0]	nF	[TX RX]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	119	mm
R_d	[45 45]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	132	mm
A_fe	0.41	V			Include PCB	0	logical				
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.6		min		N	300					
c(-1)	[-0.3:0.02:0]		[min:step:max]		TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(-3)	[0.0:0.02:0.0]		[min:step:max]		rho_x	0.18					
c(1)	[-0.1:0.05:0]		[min:step:max]		fixture delay time	0					
N_b	4	UI			Receiver testing						
b_max(1)	0				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]								
f_z	18.88	GHz			Noise, jitter						
f_p1	28	GHz			sigma_RJ	0.01	UI				
f_p2	53.125	GHz			A_DD	0.02	UI				
g_DC_HP	[-3:1:0]		[min:step:max]		eta_0	8.20E-09	V^2/GHz				
f_HP_PZ	1.328125	GHz			SNR_TX	32.5	dB				
					R_LM	0.95					

- This spread sheet is for TP4 simulation with reference receiver D
- Assuming module TX has 2 precursors

COM Configuration for Whole-Link Simulation

Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		tx_package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		tx_package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			rx_package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
C_d	[1.3e-4 0.85e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical		rx_package_tl_tau	6.141E-03	ns/mm
z_p select	[1]		[test cases to run]		Port Order	[1 3 2 4]			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
z_p (TX)	[15 32 ; 1.8 1.8]	mm	[test cases]		RUNTAG	C2M_1119					
z_p (NEXT)	[2 10 ; 0 0]	mm	[test cases]		COM_CONTRIBUTION	0	logical		Table 92–12 parameters		
z_p (FEXT)	[15 32 ; 1.8 1.8]	mm	[test cases]		Operational				Parameter	Setting	
z_p (RX)	[2 10 ; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		ERL Pass threshold	10.5	dB		board_tl_tau	5.790E-03	ns/mm
R_0	50	Ohm			DER_0	1.00E-05			board_Z_c	90	Ohm
R_d	[45 45]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (TX)	119	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (NEXT)	119	mm
A_fe	0.41	V			Include PCB	0	logical		z_bp (FEXT)	119	mm
A_ne	0.6	V			TDR and ERL options				z_bp (RX)	132	mm
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.6		min		N	300					
c(-1)	[-0.3:0.02:0]		[min:step:max]		TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(-3)	[-0.04:.02:0.0]		[min:step:max]		rho_x	0.18					
c(1)	[-0.1:0.05:0]		[min:step:max]		fixture delay time	0					
N_b	4	UI			Receiver testing						
b_max(1)	0.5				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]								
f_z	12.58	GHz			Noise, jitter						
f_p1	20	GHz			sigma_RJ	0.01	UI				
f_p2	28	GHz			A_DD	0.02	UI				
g_DC_HP	[-3.:1:0]		[min:step:max]		eta_0	8.20E-09	V^2/GHz				
f_HP_PZ	1.328125	GHz			SNR_TX	32.5	dB				
					R_LM	0.95					

- This spread sheet is for TP1a simulation with reference receiver A

Host TX FIR Tap Weight

|C(-1)|	C(-2)	C(-3)
<=10%	0	0
>10% and <15%	2%	0
>15% < 20%	4%	0
>=20%	4 or 6%	-2%

- C(-3) is adapted to -2% when |C(-1)| >= 20%. Figure is with FFE4post.