Representing Discontinuities for CR Host Board

David Katz
Liav Ben-Artsi
Marvell Semiconductor Inc.

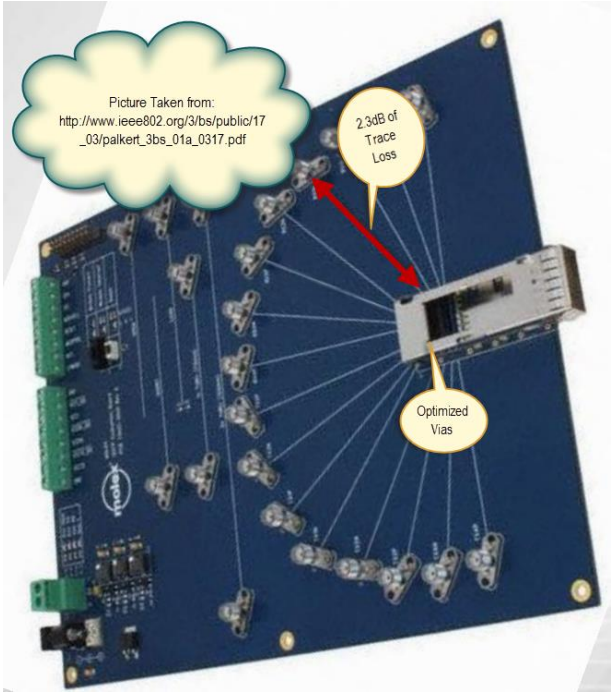
May 2019

Challenge Definition

- Basic Assumptions
  - Cable assembly MCB is optimized to best match the cable assembly and is as close as the connector can be to a seamless transition
  - µvias, or other high cost structures are acceptable
  - Impedance variance to be kept to a minimum for these test structures
  - Actual connector area to contain higher reflection via structures and higher production impedance variance.
  - Currently the “include PCB” section in COM does not account for the above discrepancies between MCB and actual PCB
- Challenge
  Update the “include PCB” section accordingly and include discontinuities, Xtalk and potentially other relevant phenomena

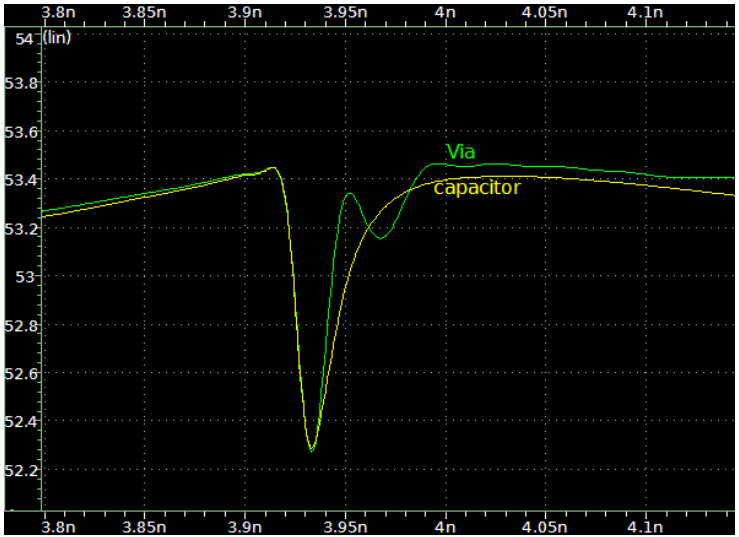
MCB Construction and Measurement Implications

- Cable assembly measurements include optimized structures and ~2.3dB of trace loss matched as best as possible to the cable
- In an actual host board the connector will be linked with through-hole via structures with minimal stubs
- Need as simple a representation as possible to the actual host board vias located at the connector area
- The representation needs to mimic the way actual host board vias would have looked from ~2.3dB away



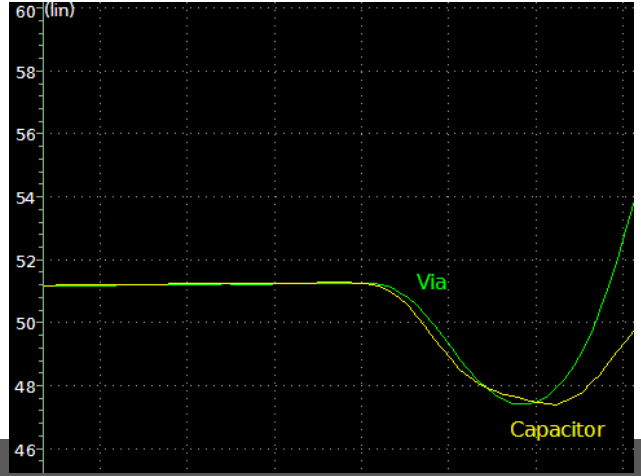
Correlating Extracted Optimized Via

- An optimized via structure placed at the connector of a host board was correlated to a capacitor discontinuity placed 2.3dB closer to the TDR
- The vias had 9 mil drill, 10 mil stub and optimized structure enabling them to be placed within the SMT connector area and a total length of ~2.7mm
- Excessive capacitance value was correlated to 19fF to be located @ the concatenation point to a measured MCB+cable assembly+MCB

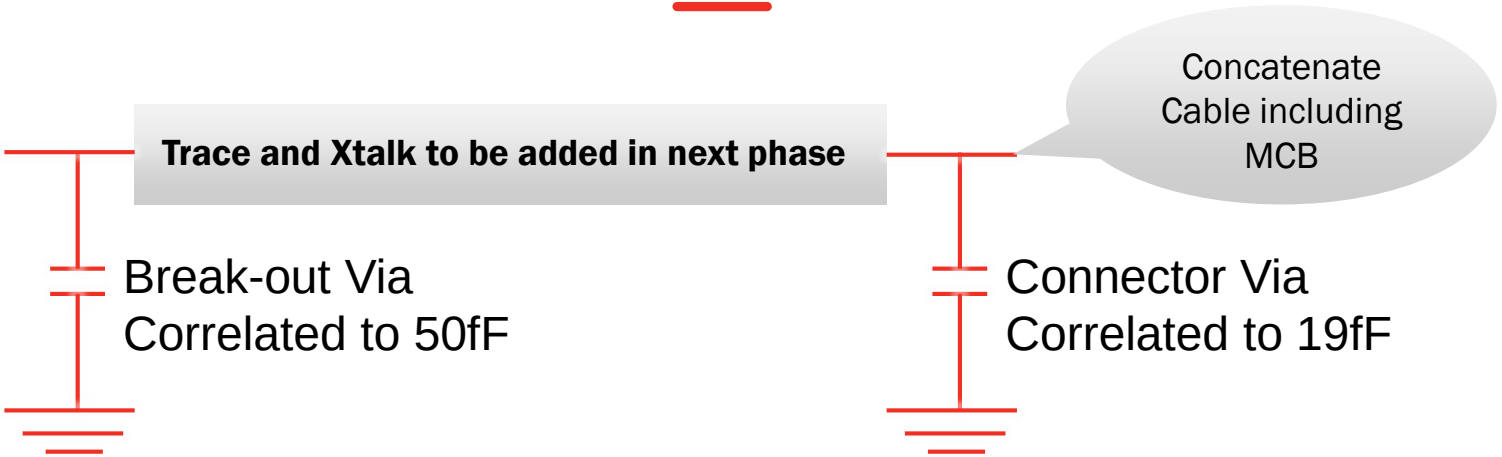


Chip Break-Out Area Phenomena

- The Chip Break-out area is characterized by via discontinuity, break-out traces cross-talk
- At this phase the break-out via excessive capacitance was correlated to a simple capacitor
- Further representation of crosstalk still to be evaluated and modeled accordingly
- An excessive capacitance of 50fF was correlated Further optimization of vias may be possible or required



Current Model to be Inserted as “Include PCB”



- Next phase to integrate crosstalk model and trace of agreed impedance and loss

“Include PBC” Status

- Vias were correlated to simple capacitance values
- A simple trace representation can be added to accommodate the end to end target loss including the MCB loss
  - At this phase cable performance can be examined
- Next phase:
  - Examine exact host board and escaping sections’ crosstalk
  - Find the appropriate methodology to account for Xtalk

Thank You