100G CR End-to-End Channel Analysis

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100G CR End-to-End Channel Model

- Add realistic ASIC package BGA and connector footprints as well in host PCB
- Several mated cable models used to create end-to-end channel
  - QSFP-DD 2m 26AWG
  - OSFP 2m 26AWG
  - OSFP 1.5m 28AWG
- Analyze COM impacts of the end-to-end channel
  - Use latest COM scripts 2.60, with config file dated 030119 (see backup slide)

End-to-End Channel Model Overview

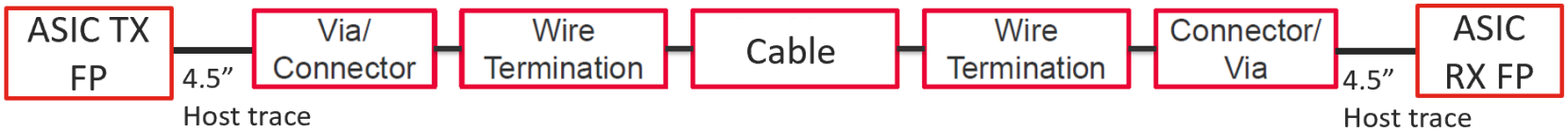
- Host PCB stack-up is 30 layers, 150mil thick, with Meg7 material
- Host PCB via stub length is modelled as 7mil
- Diff pair trace width/spacing is 4.5mil/8.5mil
- ASIC package BGA footprint is extracted in HFSS using the same PCB stack-up
- 16 pairs (8 Tx, 8 Rx) QSFP-DD or OSFP SMT Connector and host PCB footprint and wire termination are solved in HFSS

QSFP-DD Channel Buildup

- Channels 1a (new pair) / 2a (legacy pair)

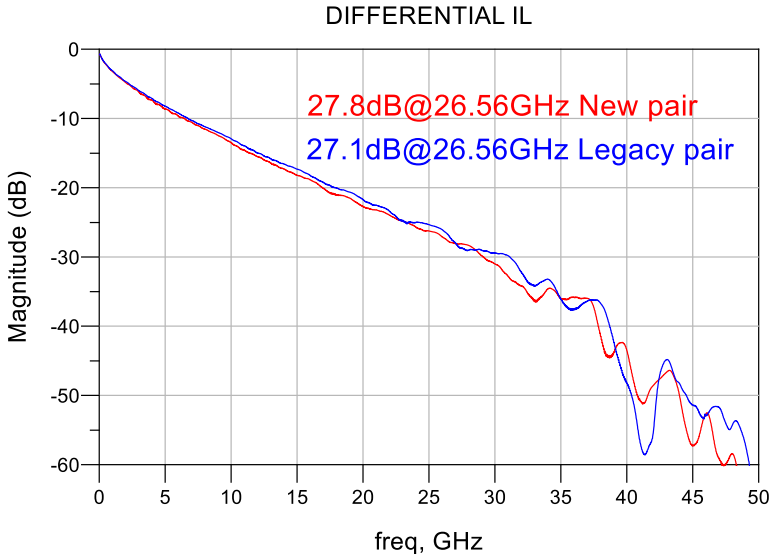
COM 6.5dB trace (table 92-12) + [QSFP-DD footprint & connector (new/legacy pair) + wire termination
+ 2m 26AWG cable + wire termination + QSFP-DD footprint & connector (new/legacy pair)] + COM 6.5dB trace (table 92-12)

- Channels 1b (new pair) / 2b (legacy pair)



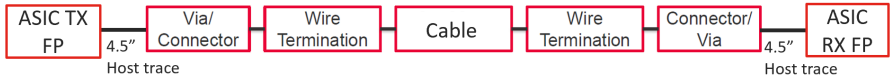
ASIC BGA footprint (mid length via) TX + host PCB trace 4.5” + [QSFP-DD footprint & connector (new/legacy pair) + wire termination
+ 2m 26AWG cable + wire termination + QSFP-DD footprint & connector (new/legacy pair)] + host PCB trace 4.5” + ASIC BGA footprint (long via) RX

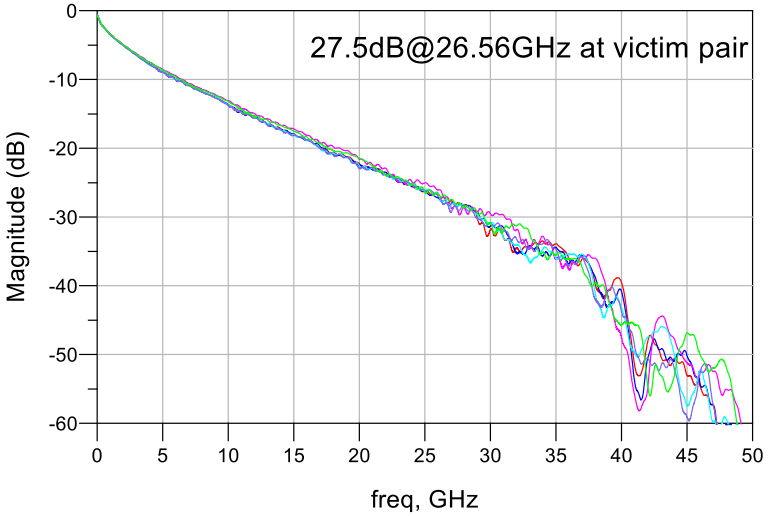
QSFP-DD Channel 1a/2a: Diff. Insertion Loss

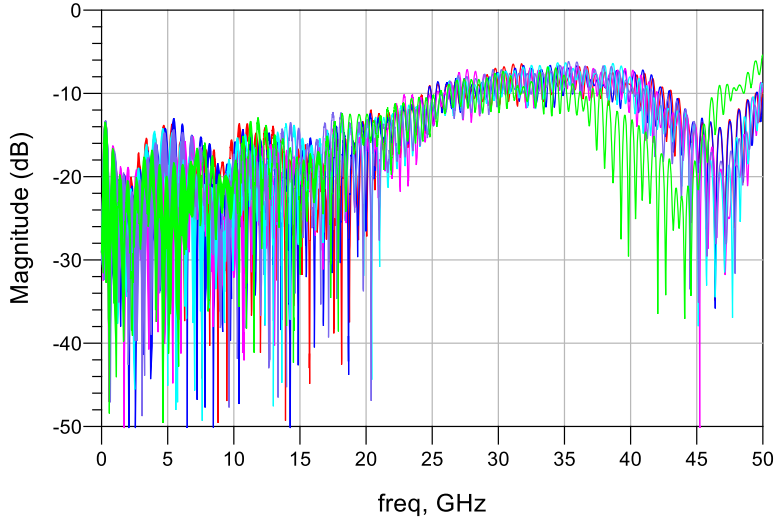


DUT	IL@26G ball to ball (dB)	FOM_{ILD} (dBrms)	ICN (mV)	COM case 1 (dB)	COM case 2 (dB)	ERL11 (dB)	ERL22 (dB)
Channel 1a (no BGA via, COM 6.5dB trace, host PCB via, new pair)	27.8	0.56	0.72	5.33	4.13	15.97	16.40
Channel 2a (no BGA via, COM 6.5dB trace, host PCB via, legacy pair)	27.1	0.67	0.54	5.66	4.55	15.93	16.54

QSFP-DD Channel 1b/2b: Diff. Insertion Loss, Return Loss

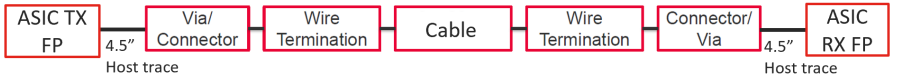






DUT	IL@26G ball to ball (dB)	FOM_{ILD} (dBrms)	ICN (mV)	COM case 1 (dB)	COM case 2 (dB)	ERL11 (dB)	ERL22 (dB)
Channel 1b (with BGA via, 4.5” host trace, host PCB via, new pair)	27.5	0.52	2.23	2.53	1.98	15.59	16.03
Channel 2b (with BGA via, 4.5” host trace, host PCB via, legacy pair)	27.1	0.63	2.22	2.67	2.30	16.73	17.20

QSFP-DD Channel 1b/2b: Far-end and Near-end Crosstalk

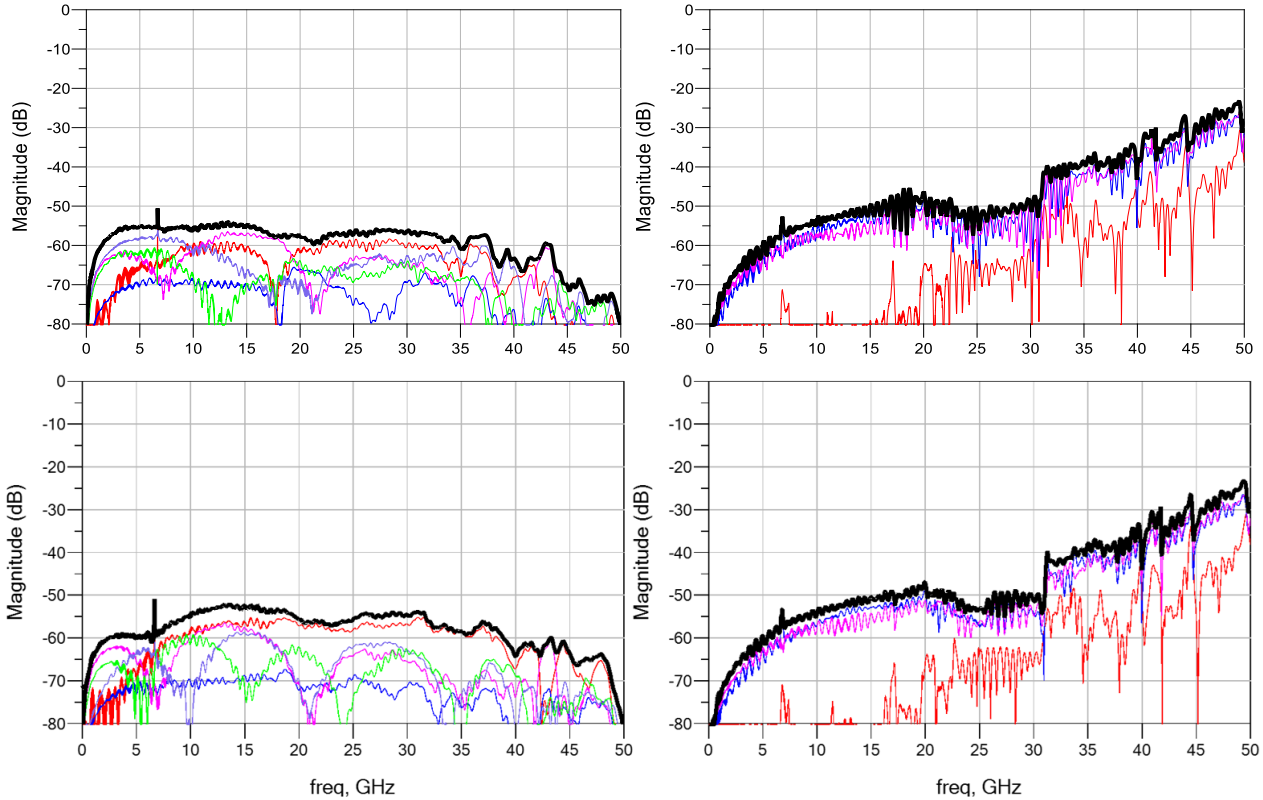


Far-end Crosstalk

Near-end Crosstalk

QSFP-DD Channel 1b (new pair)

QSFP-DD Channel 2b (legacy pair)

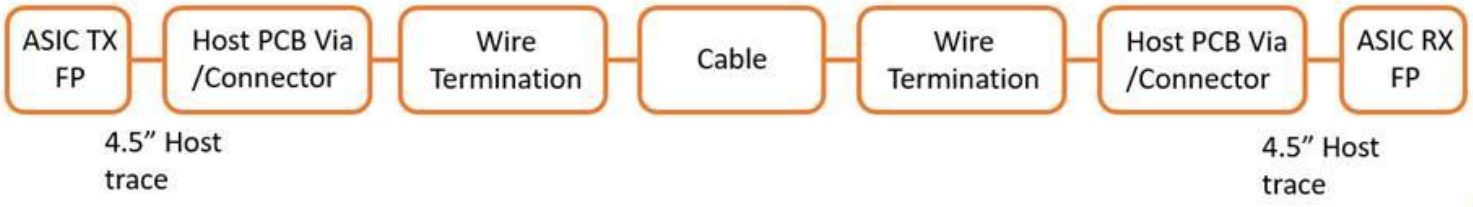


OSFP Channel Buildup

- Channel 1

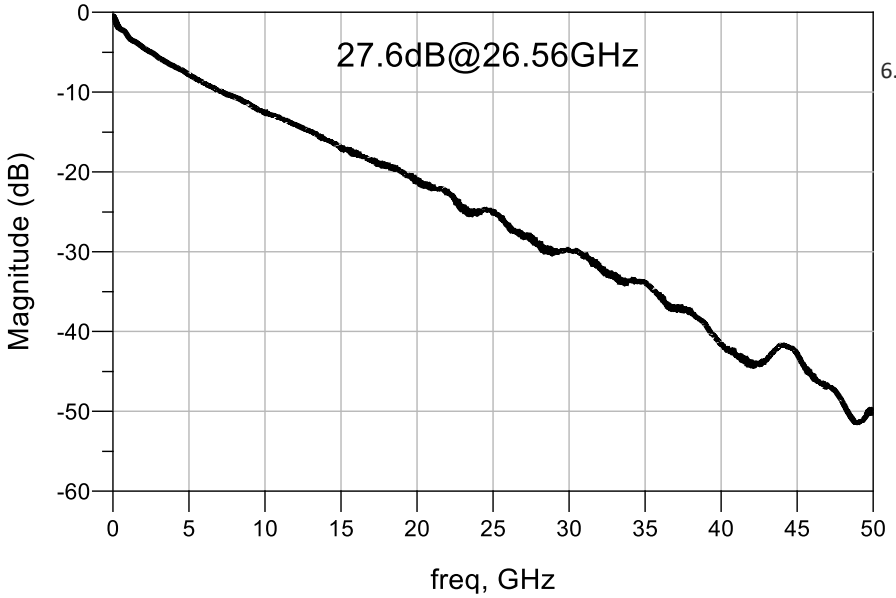
COM 6.5dB trace (table 92-12) + [OSFP footprint & connector + wire termination
+ 2m 26AWG cable + wire termination + OSFP footprint & connector] + COM 6.5dB trace (table 92-12)

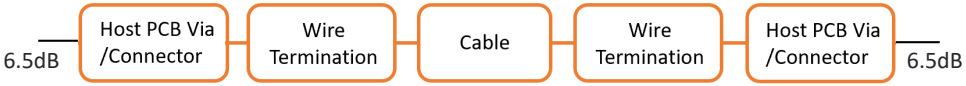
- Channel 2 (2m 26AWG cable) & Channel 3 (1.5m 28AWG cable)



ASIC BGA footprint (mid length via) TX + host PCB trace 4.5" + [OSFP footprint & connector + wire termination
+ 2m 26AWG / 1.5m 28AWG cable + wire termination + OSFP footprint & connector] + host PCB trace 4.5" + ASIC BGA footprint (long via) RX

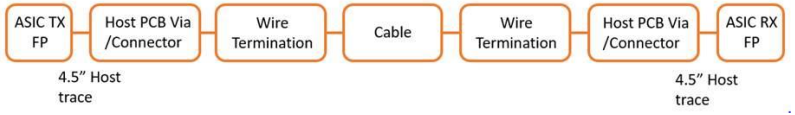
OSFP Channel 1: Diff. Insertion Loss

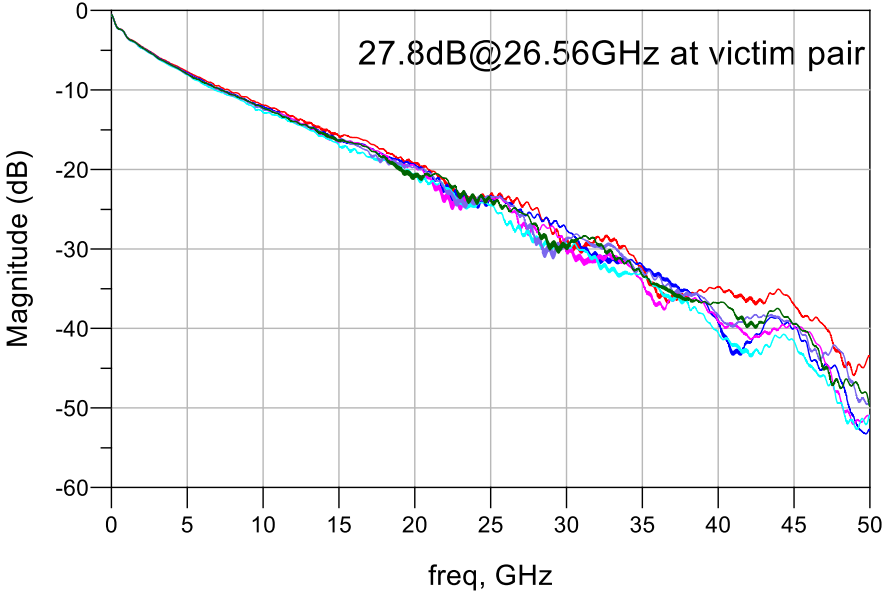


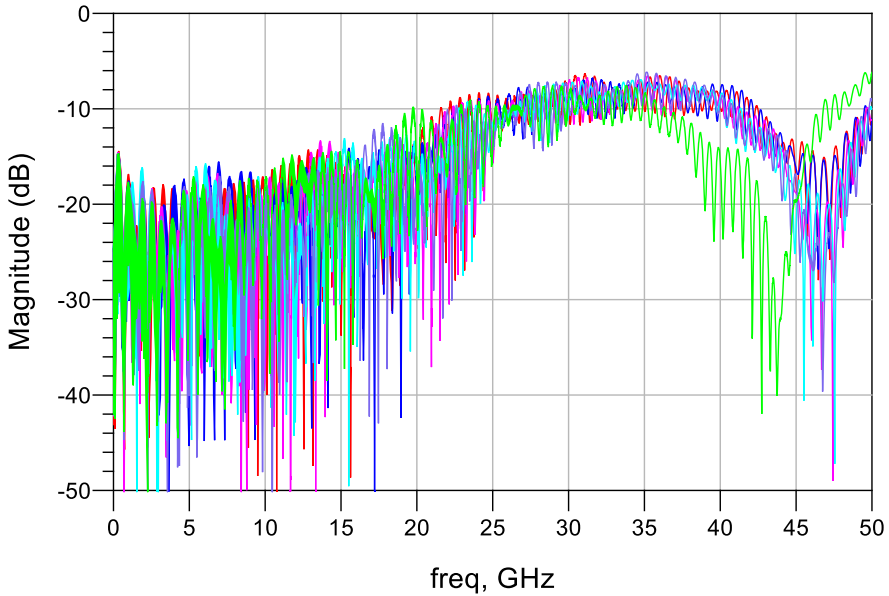


DUT	IL@26G ball to ball (dB)	FOM_{ILD} (dBrms)	ICN (mV)	COM case 1 (dB)	COM case 2 (dB)	ERL11 (dB)	ERL22 (dB)
Channel 1 (no BGA via, COM 6.5dB trace, host PCB via, 2m 26AWG	27.6	0.22	1.11	5.53	4.56	16.42	15.92

OSFP Channel 2: Diff. Insertion Loss, Return Loss

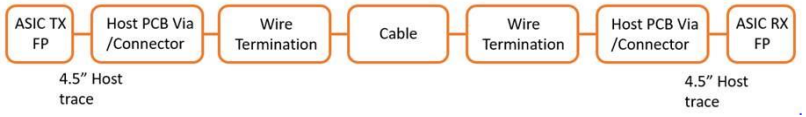


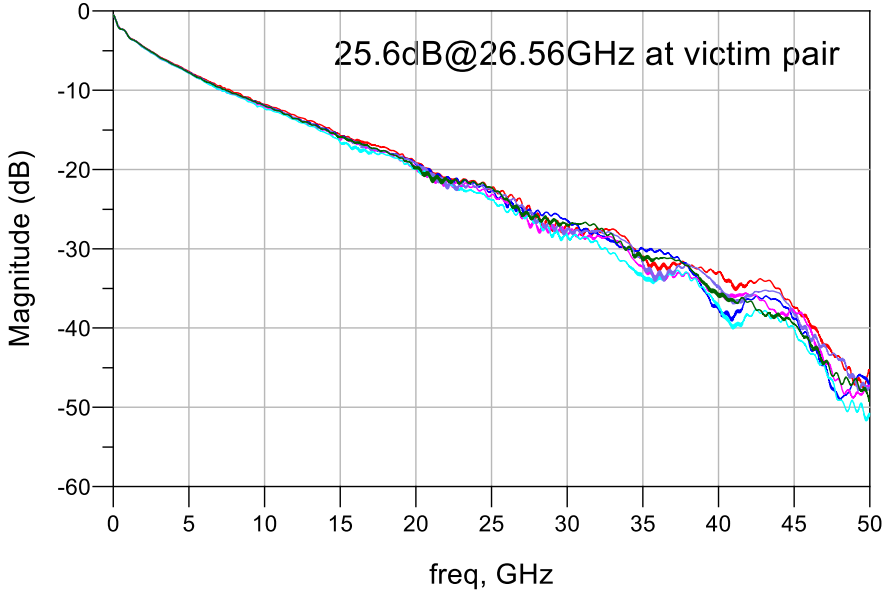


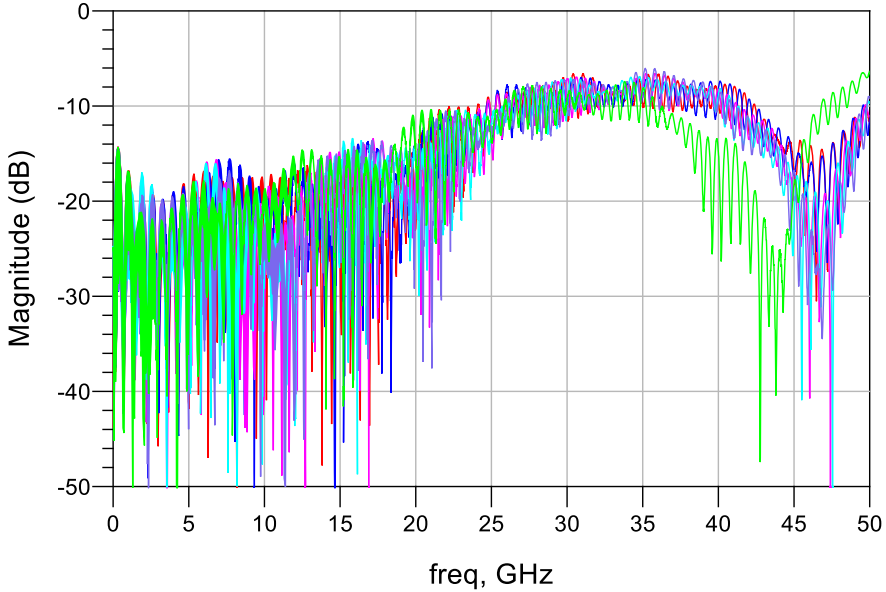


DUT	IL@26G ball to ball (dB)	FOM_{ILD} (dBrms)	ICN (mV)	COM case 1 (dB)	COM case 2 (dB)	ERL11 (dB)	ERL22 (dB)
Channel 2 (with BGA via, 4.5" host trace, host PCB via, 2m 26AWG)	27.8	0.25	2.49	3.28	2.71	17.44	16.81

OSFP Channel 3: Diff. Insertion Loss, Return Loss

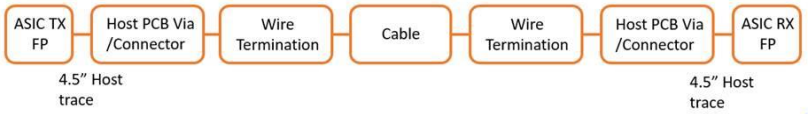






DUT	IL@26G ball to ball (dB)	FOM_{ILD} (dBrms)	ICN (mV)	COM case 1 (dB)	COM case 2 (dB)	ERL11 (dB)	ERL22 (dB)
Channel 3 (with BGA via, 4.5" host trace, host PCB via, 1.5m 28AWG)	25.6	0.20	2.34	3.95	3.41	17.97	17.81

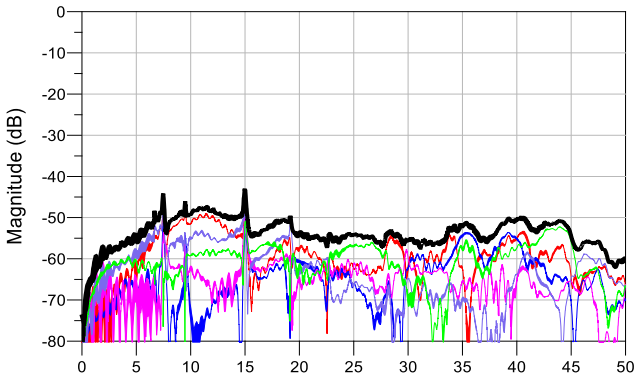
OSFP Channel 2/3: Far-end and Near-end Crosstalk

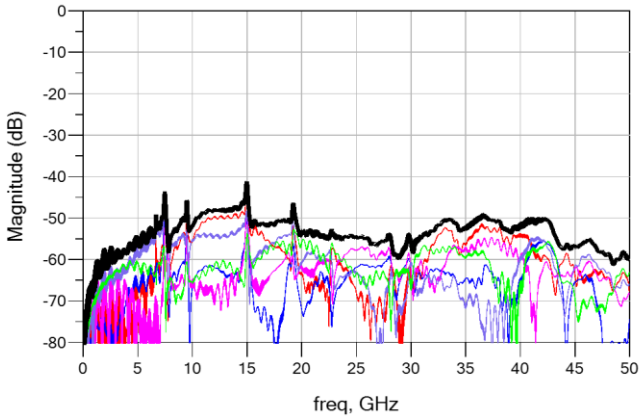


OSFP Channel 2 (2m 26AWG)

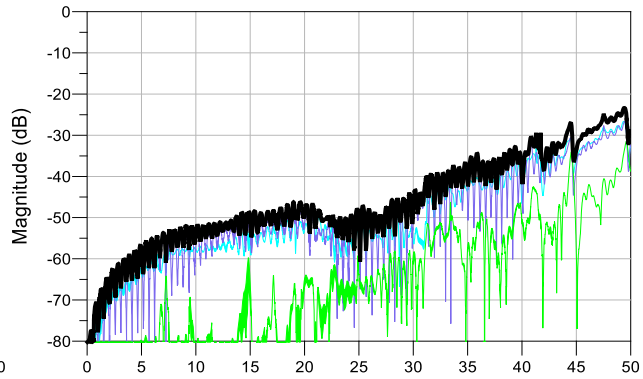
OSFP Channel 3 (1.5m 28AWG)

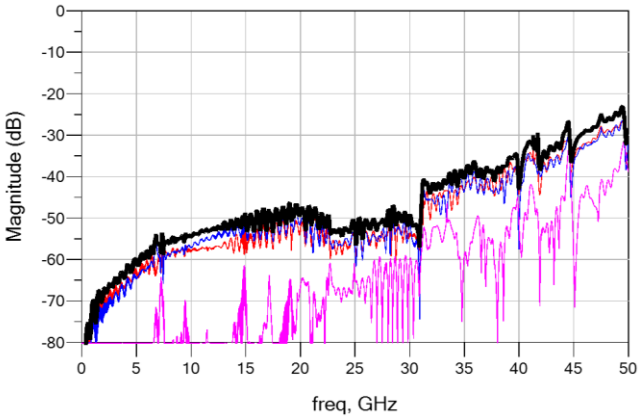
Far-end Crosstalk





Near-end Crosstalk





Analyzing the Results

- BGA footprint cannot be ignored in CR end-to-end channel
  - Interaction of die cap/package/BGA footprint cause nearly a 2dB COM impact
    - Data shows 1.85-2.25 ΔCOM
  - The cable assemblies appear to “pass” COM, but “fail” with realistic connector footprint, BGA footprint, and host trace.
- Algebraic method of concatenating IL doesn’t paint the whole picture
  - All end-to-end channels fit within the 28dB budget
    - Data shows end-to-end channel including 2m cable are 27.1-27.8dB
  - Nominal conditions were used for this analysis
- Only have a small subset of ***EARLY*** data…
  - 3dB COM seems in reach, but budget is tight!
  - We all hold a piece to the puzzle
  - … more work must be done.

Next Steps

- Analyze cable assemblies with manufacturing variation
- Rerun COM with new config spreadsheet incl. recent changes under discussions in KR track
- Continue development on connectors, host, cable, etc.

Key Takeaways

- Proceed with caution when doing algebraic concatenation of IL
- The BGA breakout cannot be ignored
- This was great collaborative work, but more work is needed!

Backup Slides

Config_com_ieee8023_93a100GEL-CR-030119

Table 93A-1 parameters		
Setting	**Units**	**Information**
53.125	GBd	
0.05	GHz	
0.01	GHz	
[1.1e-4 1.1e-4]	nF	[TX RX]
[1 2]		[test cases to run]
[12 32; 1.8 1.8]	mm	[test cases]
[12 32; 1.8 1.8]	mm	[test cases]
[12 32; 1.8 1.8]	mm	[test cases]
[12 32; 1.8 1.8]	mm	[test cases]
[0.87e-4 0.87e-4]	nF	[TX RX]
50	Ohm	
[50 50]	Ohm	[TX RX]
0.413	V	vp/vf=.694
0.413	V	vp/vf=.694
0.608	V	
4		
32		
filter and Eq		
0.75	*fb	
0.54		min
[-0.34:0.02:0]		[min:step:max]
[0:0.02:0.12]		[min:step:max]
[-0.06:0.02:0]		[min:step:max]
[-0.1:0.05:0]		[min:step:max]
24	UI	
0.85		
0.3		
[-20:1:0]	dB	[min:step:max]
21.25	GHz	
21.25	GHz	
53.125	GHz	
[-6:1:0]		[min:step:max]
0.6640625	GHz	

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.25**	
fixture delay time	0	enter sec
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

4.7 db/side

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*92.7*	mm
z_bp (NEXT)	*92.7*	mm
z_bp (FEXT)	*92.7*	mm
z_bp (RX)	*92.7*	mm