# Baseline proposal for Receiver noise model in COM for KR/CR

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# Outline

- Motivations
- System noise – model & impact
- Receiver noise – model & impact
- Appropriate levels of RX noise
- Baseline proposal for noise model in COM

# Motivation

- Currently, 'Eta_0' is applied in COM 2.60 for modeling system noise and/or receiver noise
- The following questions were raised
  - Which model is appropriate for system & receiver noise?
  - What's the impact to $COM_{min}$ budget?
- In [1], the authors highlighted COM is sensitive to wideband 'Eta_0'
  - 1.0 dB COM loss comparing Eta_0 = 16e-9 to 8e-9
- In [2], Richard proposed new "Bandlimited" model for system noise
- In [3], Adam reviewed all implementation allowance "bucket"
- In [5], Mau-Lin shared the following information
  - Impact to COM from 'band-limited' system noise modeled by [2] is small
  - 3 dB $COM_{min}$ budget may not cover impact from input-referred RX noise
- We tried to address the following topics here – by publication search
  - What's the appropriate level of RX noise?
- Observations
  - Bandlimited system noise has small impact to COM, may be ignorable
  - Most publications show RX noise with larger than $\eta_0$ = 1.64e-8

# System & Receiver Noise Models

- We model system & receiver noises in COM as below
- System noise
  - by Richard's 'Bandlimited' model [with 0.5 $mV_{rms}$]
- Receiver noise
  - by input-referred noise spectral density, $\eta_0$

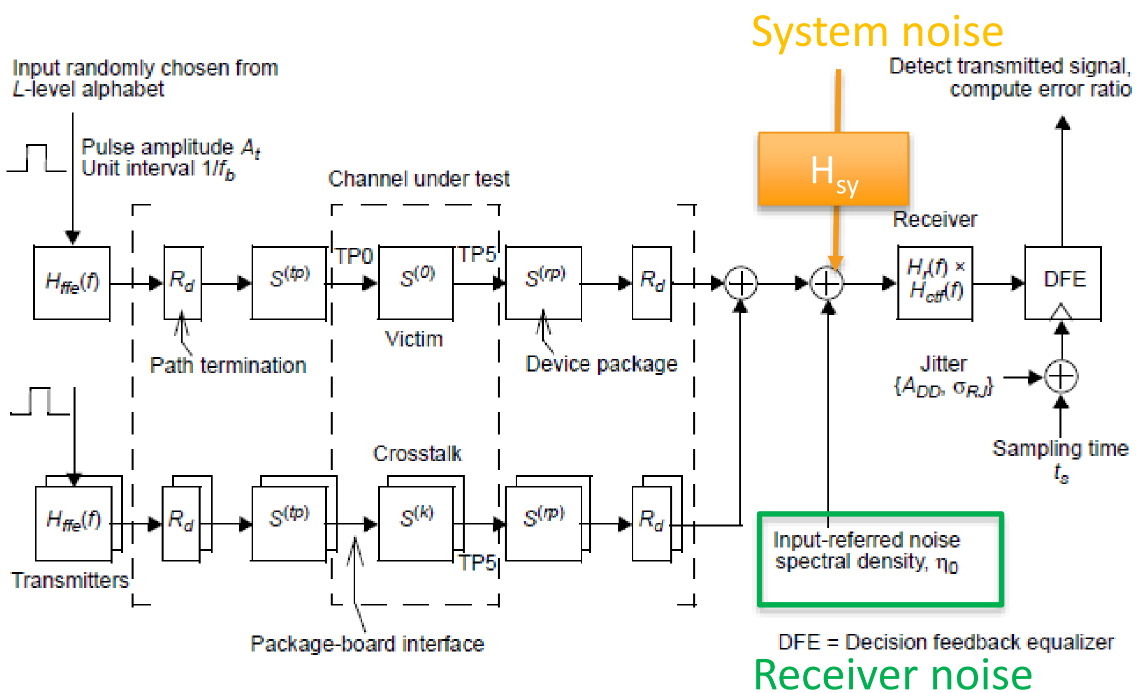
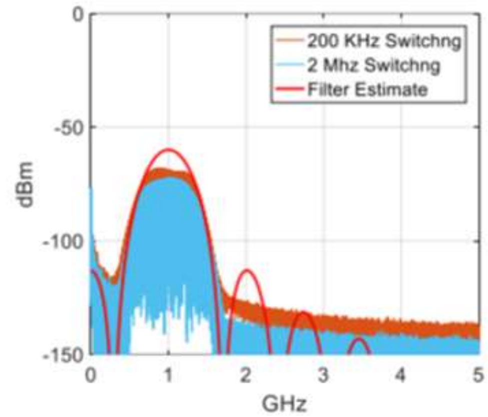



**Figure 93A–1—COM reference model**

# Bandlimited System Noise – Impact

- In [2], Richard proposed to adopt new model for system noise
- Analysis of 42 channels as [1]
- By COM 2.60
  - By enabling Richard's new system noise model by 'Bandlimited' style [2]
  - C_d = 120 fF
  - b_max[1] = 0.85, b_max[2..N_b] = 0.3




- We tried to evaluate performance impact by this new bandlimited system noise model
  - Case 1: 1mV system noise: use $\eta_0$ = 2.1238e-06 $V^2$/GHz
  - Case 2: 0.5mV system noise: use $\eta_0$ = 5.3096e-07 $V^2$/GHz
- We compared the COM loss by inc. system noise

- "Bandlimited" noise from external is NOT so critical to COM performance

| Noise ($mV_{rms}$) | COM Loss (dB, comparing to NO system noise) | | | |
|---|---|---|---|---|
| | Mean | Min | Max | Std |
| 1 | **0.58** | 0.22 | 0.93 | 0.15 |
| 0.5 | **0.21** | 0.06 | 0.36 | 0.07 |

# Receiver Noise – Impact to $COM_{min}$

| Conf. | Sys. Noise | RX Noise | COM loss in dB (to Conf. 1, which is w.o. RX noise) | | | |
|---|---|---|---|---|---|---|
| | | | Mean | Min | Max | Std |
| 0 | Off | Off | -0.21 | -0.36 | -0.06 | 0.07 |
| 1 | On | Off | 0 | 0 | 0 | 0 |
| 2 | On | $\eta_0$ = 0.82e-8 $V^2$/GHz | 1.52 | 0.18 | 3.61 | 0.83 |
| 3 | On | $\eta_0$ = 1.23e-8 $V^2$/GHz | 2.03 | 0.25 | 4.55 | 1.05 |
| 4 | On | **$\eta_0$ = 1.64e-8 $V^2$/GHz** | **2.46** | 0.32 | **5.29** | **1.21** |

- COM losses are quite different among different channels
  - Some are sensitive, while others are not
  - Would be better to include RX noise model in COM
- Take $\eta_0$ =1.64e-8 as reasonable level
  - ~2.5 dB COM loss contribute a lot to COM budget, if we don't include RX noise in COM
  - Can we take 2.5 dB from 3 dB $COM_{min}$ bucket just for two noise terms? → definitely not!
- Detailed analysis in [5]

# RX Noise Model – Noise Floor vs. Eta_0

- Boltzmann noise floor per Hz for a resistor is
  - $N_p = 10log10(k_b * T_k) + 30$
  - -172.88 dBm/Hz at 100° C (~= -173 dBm/Hz)
- Implementation noise figure (NF) : 10 ~ 20 dB
- Noise ($N_{RX}$ , dBm/Hz) = Thermal noise floor (-173) + receiver noise figure (NF)
  - $N_{RX} = 10log10\left(\frac{\eta_0}{R}/1e9 * 1e3\right)$

- What's the appropriate level?
  - ~15 dB NF? This is what we adopted in 802.3cd
    - Shall be independent of symbol rate!!
  - 0.5mV? It's critical to achieve this due to higher $f_b$!
- Action: tried to collect information from publications

| $\eta_0$ (V²/GHz) | $N_{RX}$ (dBm/Hz) | NF (dB) | $V_{rms}$ (mV @ $0.75f_b$) |
|---|---|---|---|
| 5.0119e-10 | -173.00 | 0.00 | 0.14 |
| 0.627e-8 | -162.03 | 10.97 | 0.50 |
| 0.82e-8 | -160.86 | 12.14 | 0.57 |
| 1.23e-8 | -159.10 | 13.90 | 0.70 |
| **1.64e-8** | **-157.85** | **15.15** | **0.81** |
| 2.51e-8 | -156.00 | 17.00 | 1.00 |

# Values for RX Noise – Publications

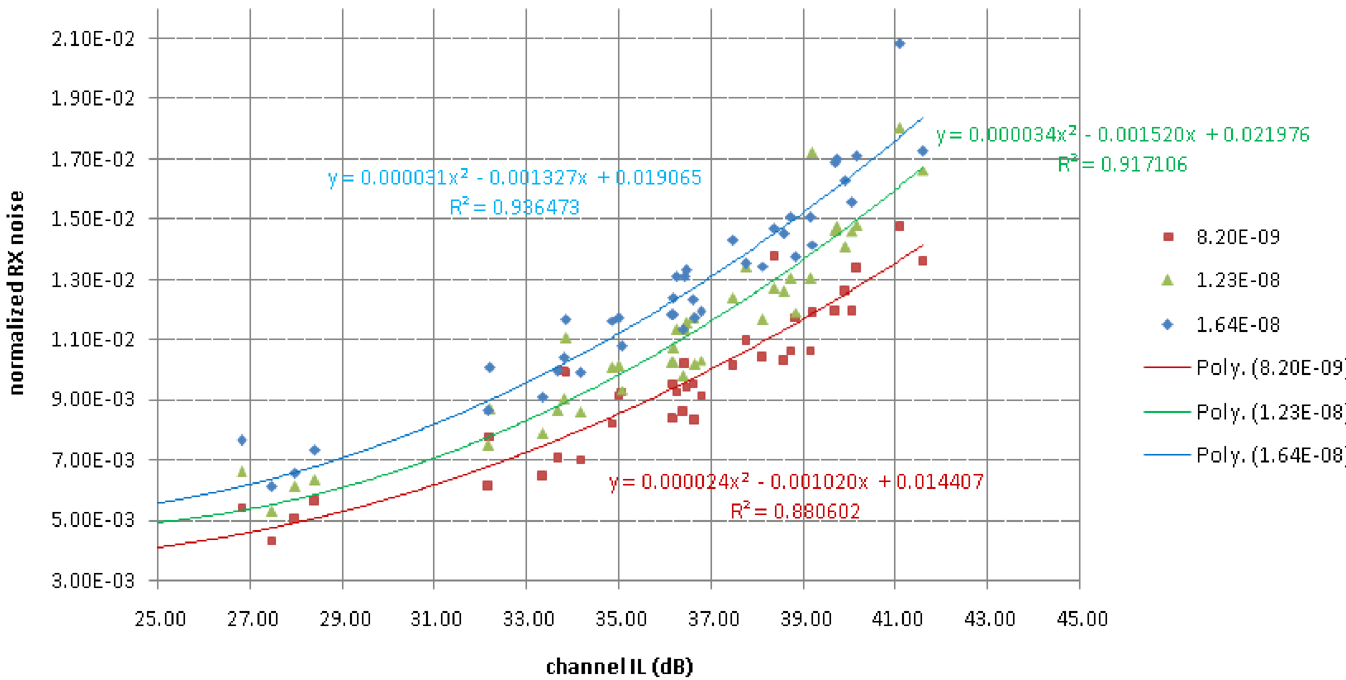
- Compare RX noise (@ input of ADC/Slicer) from different publications

| Pub. ID | | 1 | 2 | 3 [8] | 4 [7] | 5 [6] | 6 [9] |
|---|---|---|---|---|---|---|---|
| Title/Affiliation | | 802.3cd | 802.3ck | Esilicon | IBM | IBM | Huawei |
| Publisher / Year | | IEEE 2018 | IEEE | ISSCC 2019 | SVLSIC 2018 | ISSCC 2019 | 2019 JSSC |
| Rate (GHz) | | 50 | 100 | 50 | 50 | 100 | 64 |
| Modulation | | PAM4 | PAM4 | PAM4 | NRZ | PAM4/NRZ | PAM4 |
| Channel IL (dB) – bump2bump | | 30+5 | 28+8 | 42.5 | 32.5 | 19.2/37 | 29.5 |
| Process (nm) | | – | – | 7 | 14 | 14 | 16 |
| **Input-referred RX noise** | **Level ($mV_{RMS}$)** | **0.57** | **0.57** (TBD) | – | **1.8** | – | **1.2** |
| | $\eta_0$ ($V^2$/GHz) | 1.64e-8 | 8.2e-9 (TBD) | – | 8.64e-8 | – | 6.00e-8 |
| | NF (dB) | **15.15** | **12.14** (TBD) | – | **22.37** | – | **20.78** |
| **RX Noise @ ADC/Slicer** | **Level ($mV_{RMS}$)** | – | – | **2.2 (3.1 for 100G)** | – | **4.5** | – |

- Input-referred noise/NF: all are larger than 802.3cd
- RX noise @ ADC/Slicer: can't compare apple-to-apple
  - Esilicon has quit small value

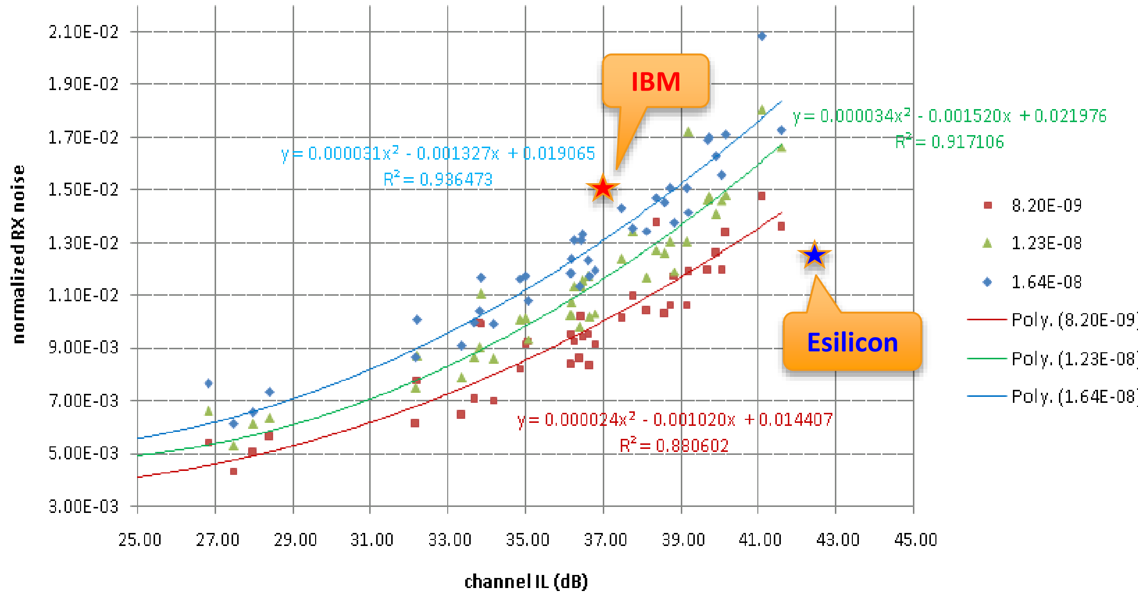
# RX noise @ input of ADC/Slicer

- RX noise @ input of ADC/slicer depends on
  - CTLE & VGA setting, input swing
- Applied COM analysis of 42 channels in [1] to calculate
  - Channel IL, CTLE setting
  - Set VGA gain as signal peak = (input swing / 2)
  - Derive 'normalized RX noise' = RX noise @ input of ADC/slicer divided by signal peak
- Three cases analyzed, with $\eta_0$ =
  - 8.2e-9
  - 1.23e-8
  - 1.64e-8
- Normalized RX noise correlates to IL well in quadrature form



# RX noise – correlation

| Pub. ID | | 3 [8] | 5 [6] |
|---|---|---|---|
| Author/Affiliation | | Esilicon | IBM |
| Rate (GHz) | | 50 | 100 |
| Channel IL (dB) | | 42.5 | 37 |
| Input swing (mVpdd) | | 500 | 600 |
| RX Noise @ ADC/Slicer | Level ($mV_{RMS}$) | 2.2 (3.1 for 100G) | 4.5 |
| | Normalized RX noise | 1.24e-02 | 1.5e-02 |
| Derived $\eta_0$ ($V^2$/GHz) | | | |

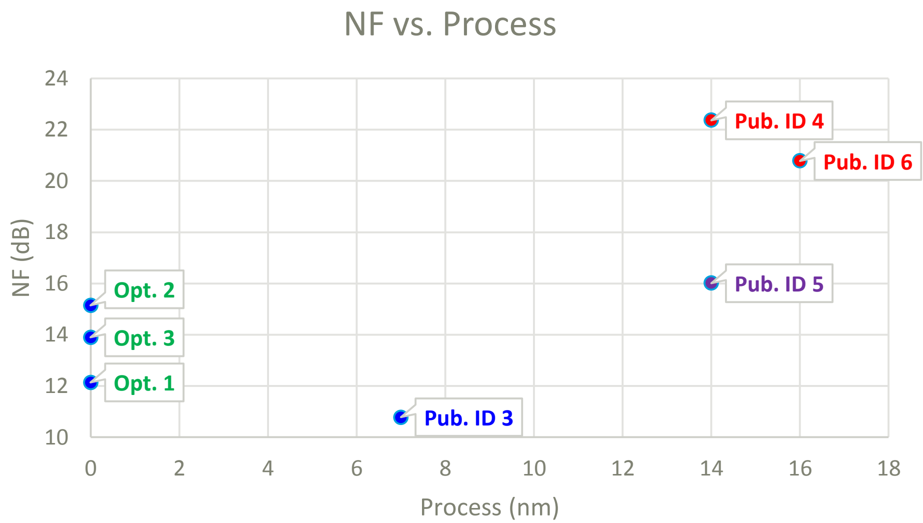



- By calculating ‘normalized RX noise’ of Esilicon and IBM & plot on the figure from COM analysis, we can derive $\eta_0$ as below
  - Pub. ID 3: $\eta_0$ ~= 6.0e-9
  - Pub. ID 5: $\eta_0$ ~= 2.0e-8
- From the above analysis, there are two groups by ‘RX noise’ viewpoint
  - Very ‘small’ RX noise ($\eta_0 < 8.2e-9$) : Pub ID. 3
  - Larger RX noise ($\eta_0 > 1.64e-8$) : Pub ID. 4, 5, 6

# RX Noise Level – Publications Compare

| Pub. ID | | Opt. 1 | Opt. 2 | Opt. 3 | 3 [8] | 4 [7] | 5 [6] | 6 [9] |
|---|---|---|---|---|---|---|---|---|
| Title/Affiliation | | 802.3ck | | | Esilicon | IBM | IBM | Huawei |
| Publisher / Year | | IEEE | | | ISSCC 2019 | SVLSIC 2018 | ISSCC 2019 | 2019 JSSC |
| Rate (GHz) | | 100 | | | 50 | 50 | 100 | 64 |
| Channel IL (dB) – bump2bump | | 28+8 | | | 42.5 | 32.5 | 37 | 29.5 |
| Process (nm) | | – | | | 7 | 14 | 14 | 16 |
| **Input-referred RX noise** | $\eta_0$ ($V^2$/GHz) | 0.82e-8 | 1.64e-8 | 1.23e-8 | ***6.0e-9*** | 8.64e-8 | ***2.0e-8*** | 6.00e-8 |
| | NF (dB) | **12.14** | **15.15** | **13.90** | ***10.78*** | **22.37** | ***16.01*** | **20.78** |
| **RX Noise @ ADC/Slicer** | **Level ($mV_{RMS}$)** | – | – | – | **2.2 (3.1 for 100G)** | – | **4.5** | – |

- RX noise variation among vendors are large
  - NF from 11 dB to 22 dB
  - NF from 16 ~ 22 dB even in 14 or 16nm
- Analog design doesn't benefit a lot from advanced process
- NF of Pub. ID 3 is very good



# Conclusions

- Bandlimited system noise model
  - Impact to COM is small & may be ignorable
- Receiver noise impacts to $COM_{min}$ bucket
  - Average of 2.46dB by $\eta_0$ = 1.64e-8 $V^2$/GHz
  - Variation is large, may require model for COM accuracy
- Appropriate RX noise level
  - Most publications show value larger than $\eta_0$ = 1.64e-8

# Proposal Options

- Based on the above analysis, we proposed the following proposal options for discussion

| Option | RX noise | | Sys. noise | $COM_{min}$ (dB) | Comments for consensus discussion |
|---|---|---|---|---|---|
| | $\eta_0$ ($V^2$/GHz) – "input referred" | Noise Factor, (dB) | $\eta_0$ ($V^2$/GHz) – bandlimited *1 | | |
| Option 1 | 0.82e-8 | 12.14 | NA | 3.0 | Present working spreadsheets |
| Option 2 | 1.64e-8 | 15.15 | 5.3096e-07 | 2.5 | Balanced missing/false alarm |
| Option 3 | 1.23e-8 | 13.90 | NA | 3.0 | Model only RX noise with more appropriate levle |
| Option 4 | 5.0119e-10 | 0 | 5.3096e-07 | 3.0 or TBD | Only consider resistor thermal noise and system noise. NF included in $COM_{min}$ budget |
| Option 5 | 1.64e-8 | 15.15 | NA | 3.0 | No system noise & 3.0dB margin |
| Option 6 | | | | | Something else |

- *1 The bandlimited "system" noise is modeled as proposed by Richard [2]

# References


- [1] Mau-Lin Wu, et al., "**COM Parameters Proposal for KR**", IEEE 802.3ck 2019 March Plenary Meeting [wu_3ck_01b_0319.pdf]
- [2] Richard Mellitz, "**Exploring System Noise, $\eta_0$ , for Usage in COM**", IEEE 802.3ck 2019 March Plenary Meeting [mellitz_3ck_01_0319.pdf]
- [3] Adam Healey, "**Considerations for the minimum COM limit**", IEEE 802.3ck 2019 March Plenary Meeting [healey_3ck_01_0319.pdf]
- [4] Beth Kochuparambil, "**Summary of System Discussion of Backplane Channels**", IEEE 802.3ck 2019 January interim Meeting [kochuparambil_3ck_01c_0119.pdf]
- [5] Mau-Lin Wu, et al., "**Discussion of System Noise & Receiver Noise in COM**", IEEE 802.3ck May 8th, 2019 ad-hoc meeting [wu_3ck_adhoc_01a_050819.pdf]
- [6] A. Cevrero, et al., "**6.1 A 100Gb/s 1.1pJ/b PAM-4 RX with Dual-Mode 1-Tap PAM-4 / 3-Tap NRZ Speculative DFE in 14nm CMOS FinFET**", IEEE ISSCC, p. 112-114, 2019.
- [7] P.A. Francese, et al., "**A 50GB/S 1.6PJ/B RX Data-Path with Quarter-Rate 3-Tap Speculative DFE**", IEEE Symp. VLSI Circuits, pp. 267-268, June 2018.
- [8] M. Pisati, et al., "**6.3 A Sub-250mW 1-to-56Gb/s Continuous-Range PAM-4 42.5dB IL ADC/DAC-BasedTransceiver in 7nm FinFET**", IEEE ISSCC, p. 116-118, 2019
- [9] P. A. Francese, et al., "**A 50GB/S 1.6PJ/B RX Data-Path with Quarter-Rate 3-Tap Speculative DFE**", IEEE Symposium on VLSI Circuits, pp. 267-268, 2018

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