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Representing imperfections for CR Host Board

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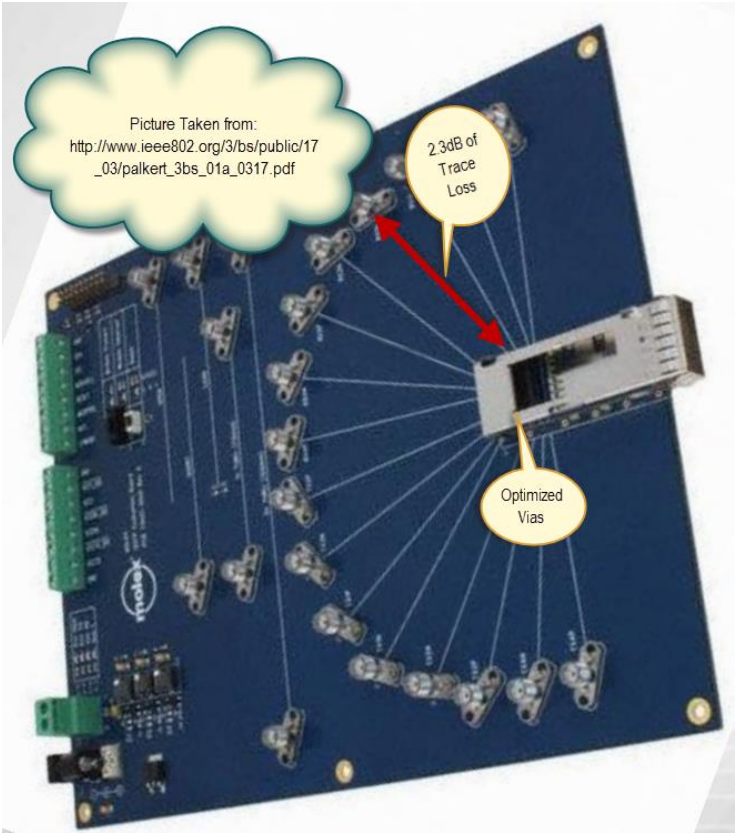
Challenge Definition – Presented During May Interim

- Basic Assumptions
  - Cable assembly MCB is optimized to best match the cable assembly and is as close as the connector can be to a seamless transition
  - µvias, or other high cost structures are acceptable
  - Impedance variance to be kept to a minimum for these test structures
  - Actual connector area to contain higher reflection via structures and higher production impedance variance.
  - Currently the “include PCB” section in COM does not account for the above discrepancies between MCB and actual PCB
- Challenge
  Update the “include PCB” section accordingly and include discontinuities, Xtalk and potentially other relevant phenomena

MCB Construction and Measurement Implications

- Cable assembly measurements include optimized structures and ~2.3dB of trace loss matched as best as possible to the cable
- In an actual host board the connector will be linked with through-hole via structures with minimal stubs
- Need as simple a representation as possible to the actual host board vias located at the connector area
- The representation needs to mimic the way actual host board vias would have looked from ~2.3dB away

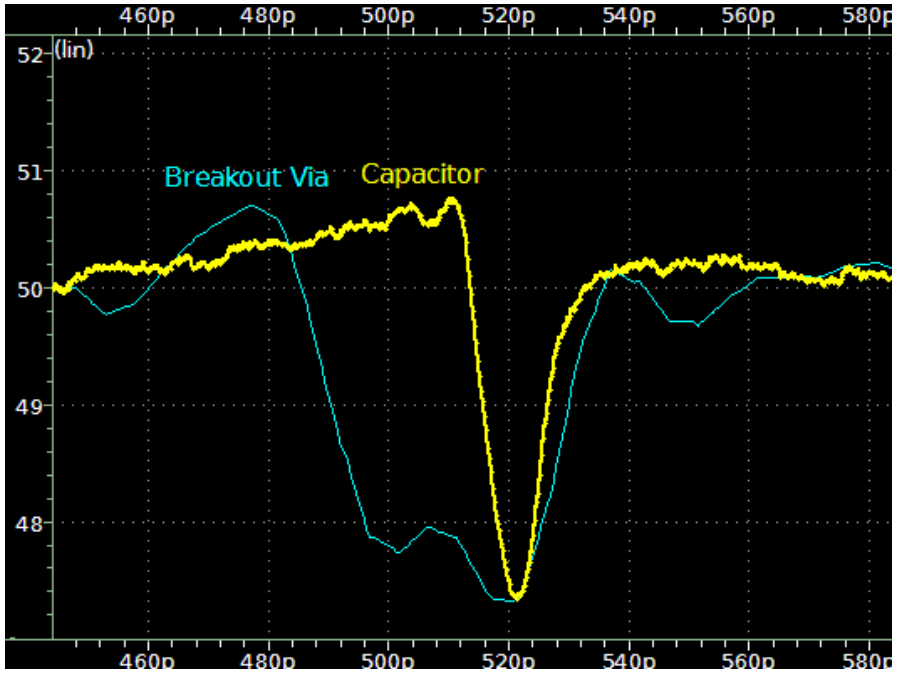


Correlating Extracted Optimized Via (May Interim)

- An optimized via structure placed at the connector of a host board was correlated to a capacitor discontinuity placed 2.3dB closer to the TDR
- The vias had 9 mil drill, 10 mil stub and optimized structure enabling them to be placed within the SMT connector area and a total length of ~2.7mm
- Excessive capacitance value was correlated to 19fF to be located @ the concatenation point to a measured MCB+cable assembly+MCB

Chip Break-Out Area Phenomena

- The Chip Break-out area is characterized by via discontinuity & break-out traces cross-talk
- Further optimization of break-out Via and correlating the impedance fall to an excessive capacitance resulted in a value of 29fF

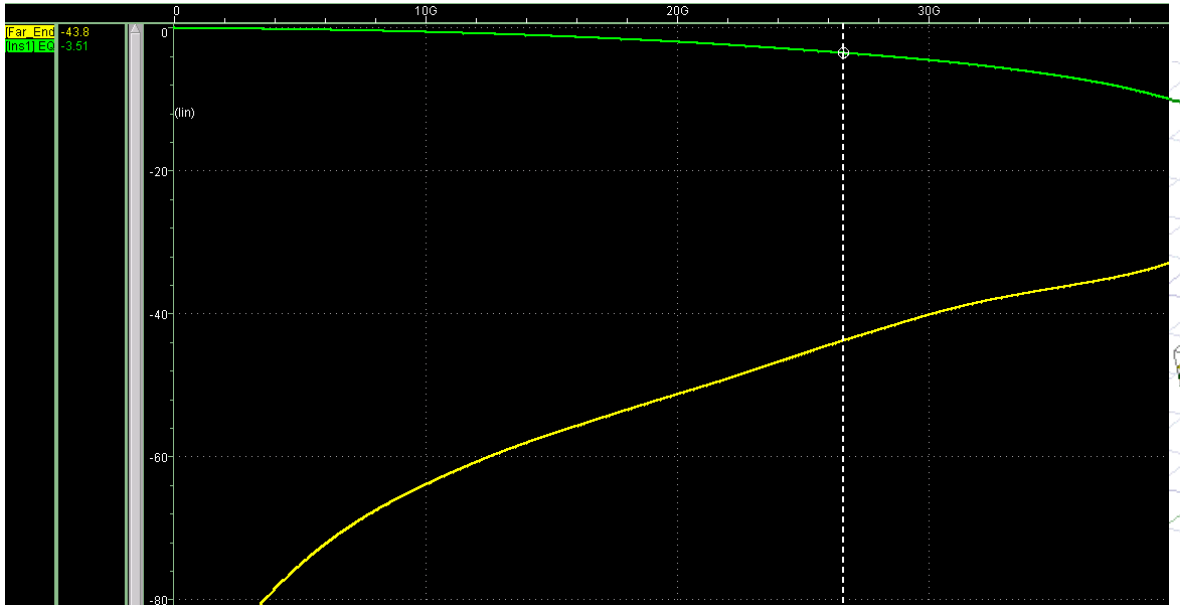


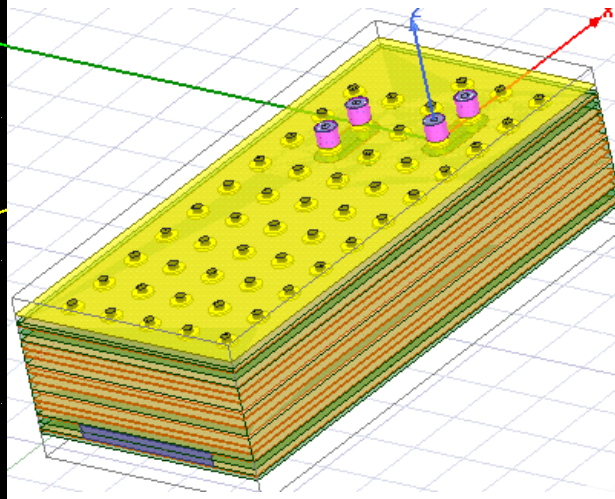
- Cascading only break-out lower loss discontinuity section to a cable and running with Include PCB=0 results in ~0.23 of lower COM compared to current include

PCB current case Cable	Case	COM
Thru_Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	org	6.021
Thru_Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	cascaded	5.798

Chip Break-Out Area Phenomena – XTalk.

- @ 50Gbps BO Xtalk was low enough to ignore… @100G?!
- Analyzed via pattern surrounded by GND (as was defined by a group of 802.3ck participants during discussions prior to this work done) and break-out traces Xtalk from ONE aggressor ➔ 40.29dB ICR
- Two statistically correlated aggressors ➔ 34.29dB
- Two statistically Uncorrelated aggressors ➔ 37.28dB

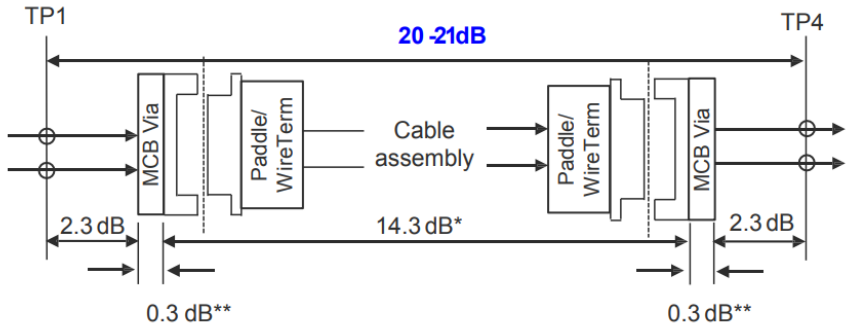


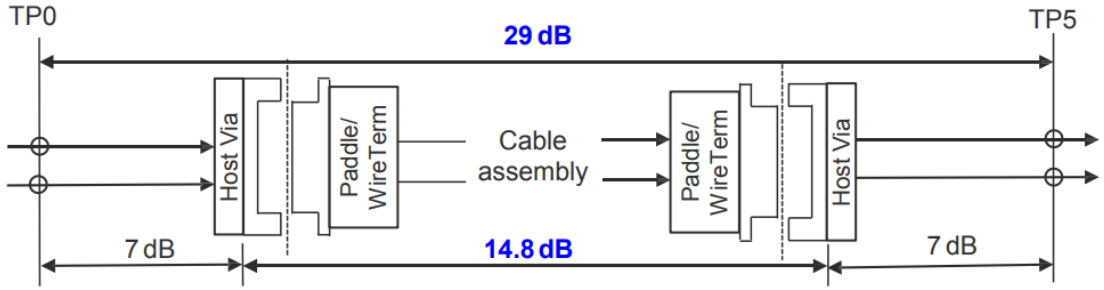


- Tx side testing: SNDR @ TP0 is -33dB – How would it look @ TP0a? Lower SNDR to account for Xtalk?!
- End2End COM: Accounting for two aggressors Xtalk on Tx or Rx side ONLY translates to an updated SNDR of 30.587dB / 31.62dB

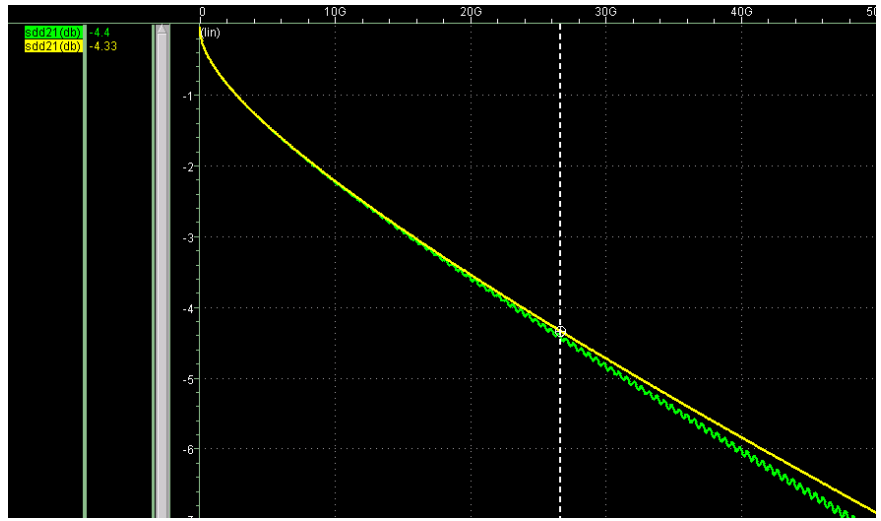
“Include PCB” Trace Loss

- As suggested in http://www.ieee802.org/3/ck/public/19_05/palkert_3ck_01b_0519.pdf
- TP0-TP1 Loss should follow ≈ 7dB-2.3dB-0.3dB = 4.4dB

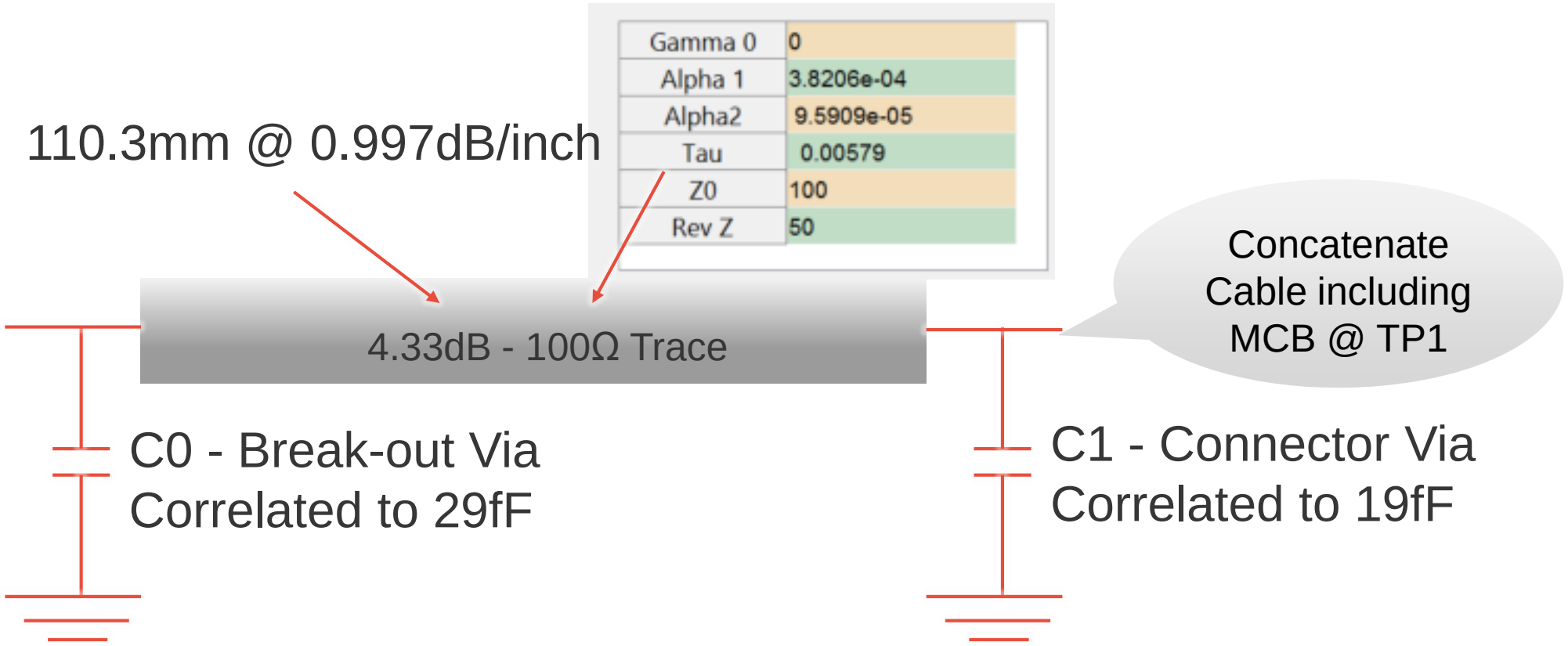




- Given Correlated capacitance, pure trace loss = 4.33dB ➔ 4.4dB by capacitance ripple



Current Model to be Inserted as “Include PCB”



Updated “Include PCB” Status & Tests

- Vias were correlated to simple capacitance values 29fF & 19fF
  - Added these two capacitances
- A simple trace representation is added between these vias to accommodate the end to end target loss taking into account MCB loss
  - Fit 4.33dB – 100Ω “Meg7 like” trace for parameters

Two phase examination was performed:

- Integrate suggestion into a “test” COM version and examine impact
- Alter SNDR to account for Xtalk and examine impact

Included In this Suggestion (&?)

- (Optimized) Discontinuities correlated, for simplicity to a simple pure cap
- A pure 100Ω trace – No manufacturing tolerance taken into account
- Two statistically correlated crosstalk aggressors only with ball-map pattern defined by the group
  - No aggressors @ Rx side; no aggressors in front of/behind the victim
- No manufacturing tolerance related cross-talk

Suggestion Impact

- DFE Case includes floating taps; Coil, or “NoCoil” had minor impact
- Impact of adding capacitance discontinuities = 0.354dB
- Impact of representing crosstalk by SNDR = ~0.7dB

Run case	Cable	SNDR	
Original	Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	33	5.934
C0=29ff; C1=19ff; SNDR=33	Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	33	5.58
C0=29ff; C1=19ff; SNDR=30.587	Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	30.587	4.883

- Three cables studied for the impact of representing Xtalk by SNDR ➔ 0.27dB (in Cable with worst COM) to 0.7dB (in Cable with best COM)

Case	Combined SNDR	Final COM
Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	33	5.663
Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	30.54	4.959
qsfpddmtf-dd-2m-qsfpddmtf_V2_	33	4.657
qsfpddmtf-dd-2m-qsfpddmtf_V2_	30.54	4.082
CAd2d__2p0m_awg28_m_BC-BOR_N_N_N	33	1.24
CAd2d__2p0m_awg28_m_BC-BOR_N_N_N	30.54	0.973

Suggestion Summary

It was shown that the current “include PCB” representation under accounts for actual host board imperfections.

A partial, simple representation is suggested to represent host PCB

Actions

- Add two capacitors C0 and C1 on both sides of the “include PCB” trace
- Capacitors & trace parameters & values should follow slide #9
- Add another crosstalk SNDR parameter (CSNDR = 34.29dB) Power-Sum CSNDR with Tx SNDR for an updated TxSNDR in case include PCB = 1

Thank You

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Back-up

Suggestion Impact

- DFE Case -No floating taps, 24 static taps; Coil, or “NoCoil” had minor impact
- Impact of adding capacitance discontinuities = 0.34dB
- Impact of representing crosstalk by SNDR = ~0.7dB

Cables	mode	sndr	
Thru_Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	org	33	6.021
Thru_Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	new	33	5.68
Thru_Tx7_TP1toTP4_OSFP100G_1p5m_28AWG	new	30.5	4.974
qsfpddmtf-dd-2m-qsfpddmtf_V2_	org	33	4.837
qsfpddmtf-dd-2m-qsfpddmtf_V2_	new	33	4.568
qsfpddmtf-dd-2m-qsfpddmtf_V2_	new	30.5	3.999