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100G C2M TP1a Channel/System Analysis

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IEEE 802.3ck 100G Electrical

Overview

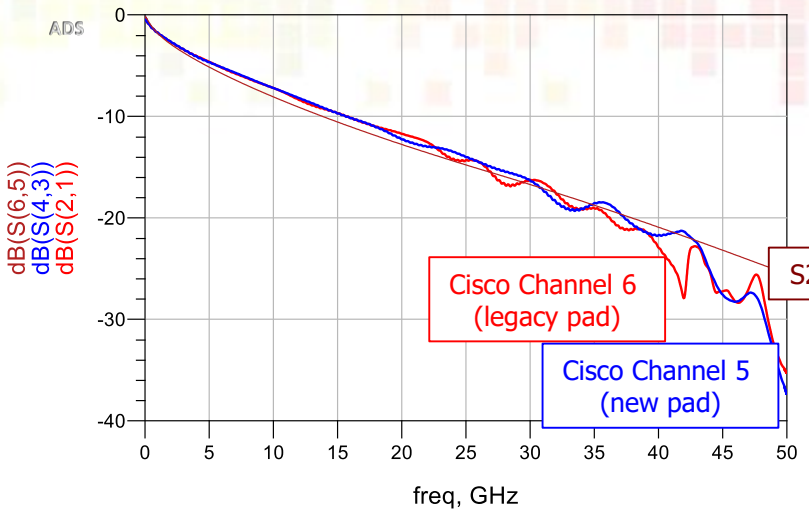
- An electrical equivalent model of one of the more difficult C2M channels is generated in order to determine penalties due to various channel elements

- An accurate, equivalent electrical model allows other scenarios to be evaluated such as the effect of artificially reducing host trace loss or possibly improving various channel elements to estimate expected gains in overall system performance

- Several cases were investigated for TP1a based on a 5-tap FFE reference receiver

Jane Lim C2M channels (as described in lim_3ck_01_0319)

Cisco "legacy" and "new pad" C2M channels

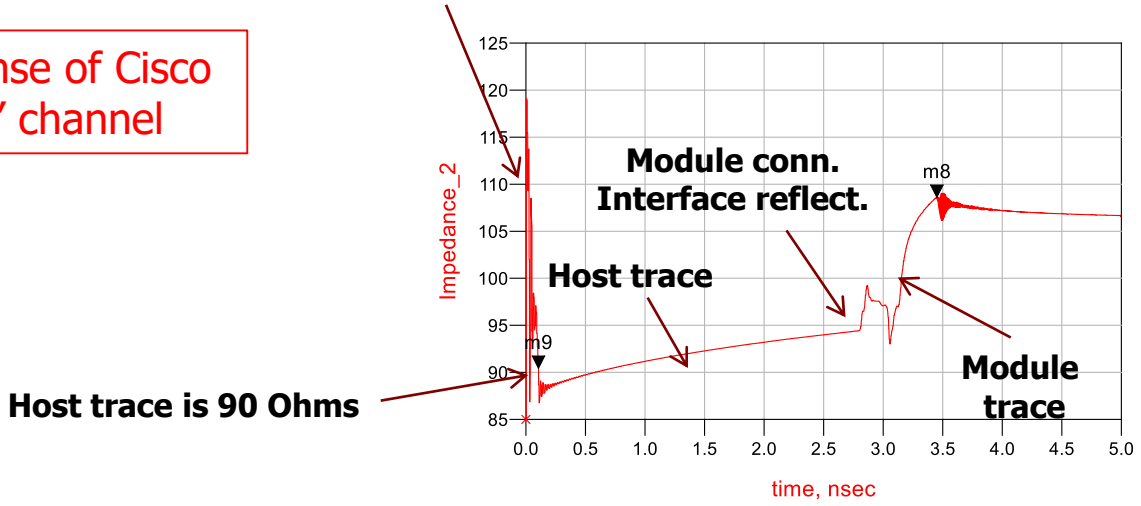


S21 of 13.3" 'Ed' Megtron-7 trace

FOMILD = 0.174 dB

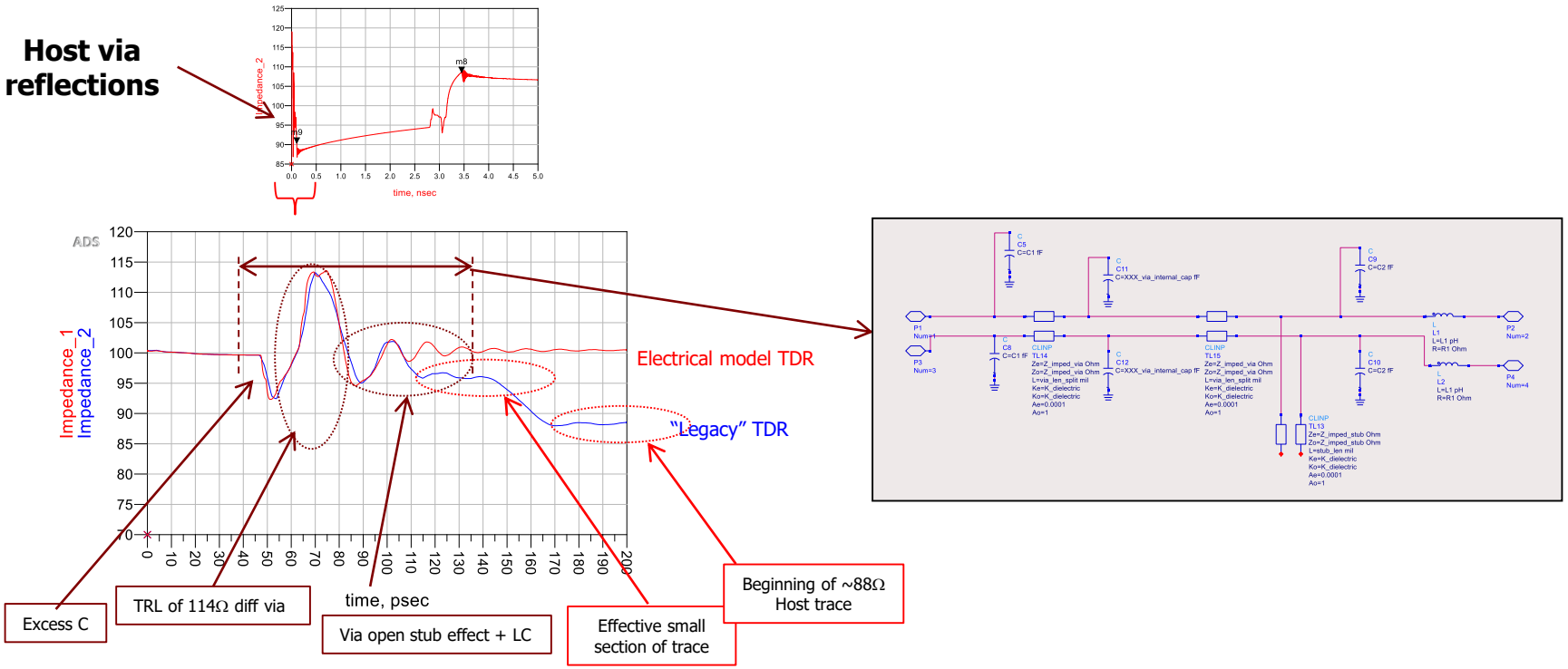
FOMILD = 0.159 dB

TDR response of Cisco "legacy" channel



Host via transition modeling (1/2)

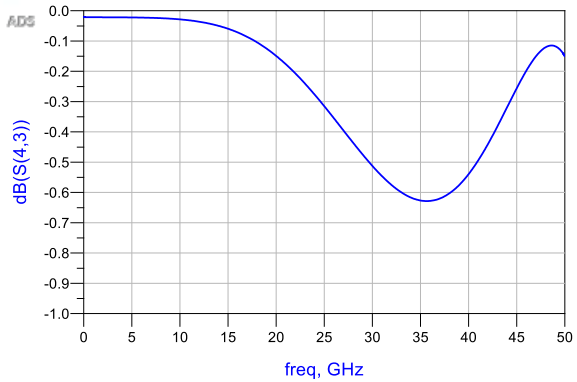
- **Creating an equivalent electrical model of the host via interconnect region using a TDR step response**
  - Channel TDR response was correlated with COM and ADS built-in TDR function

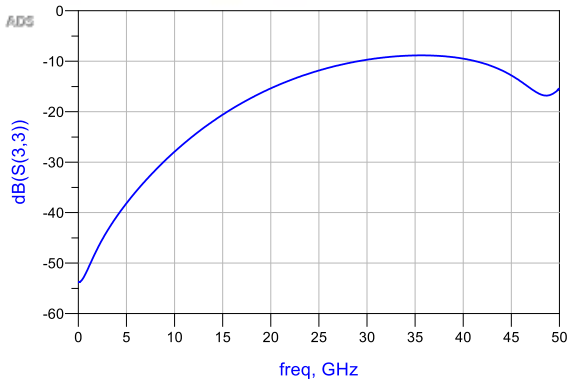


- **Electrical model is made up of transmission line and lumped component elements**

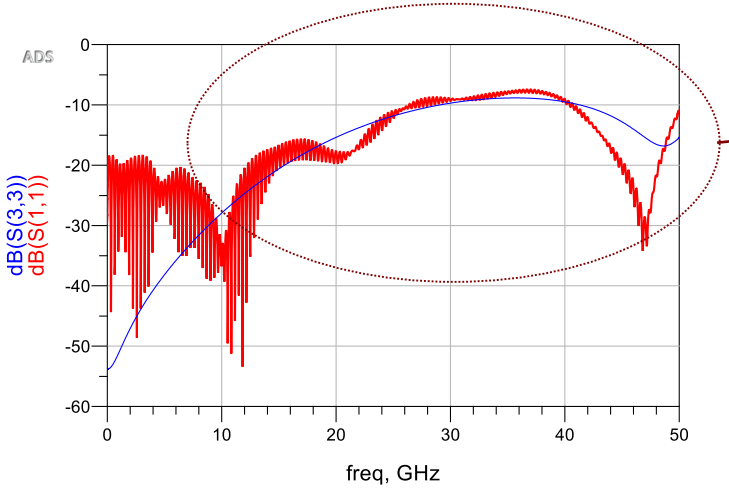
Host via transition modeling (2/2)

❑ S-parameters of electrical via transition model





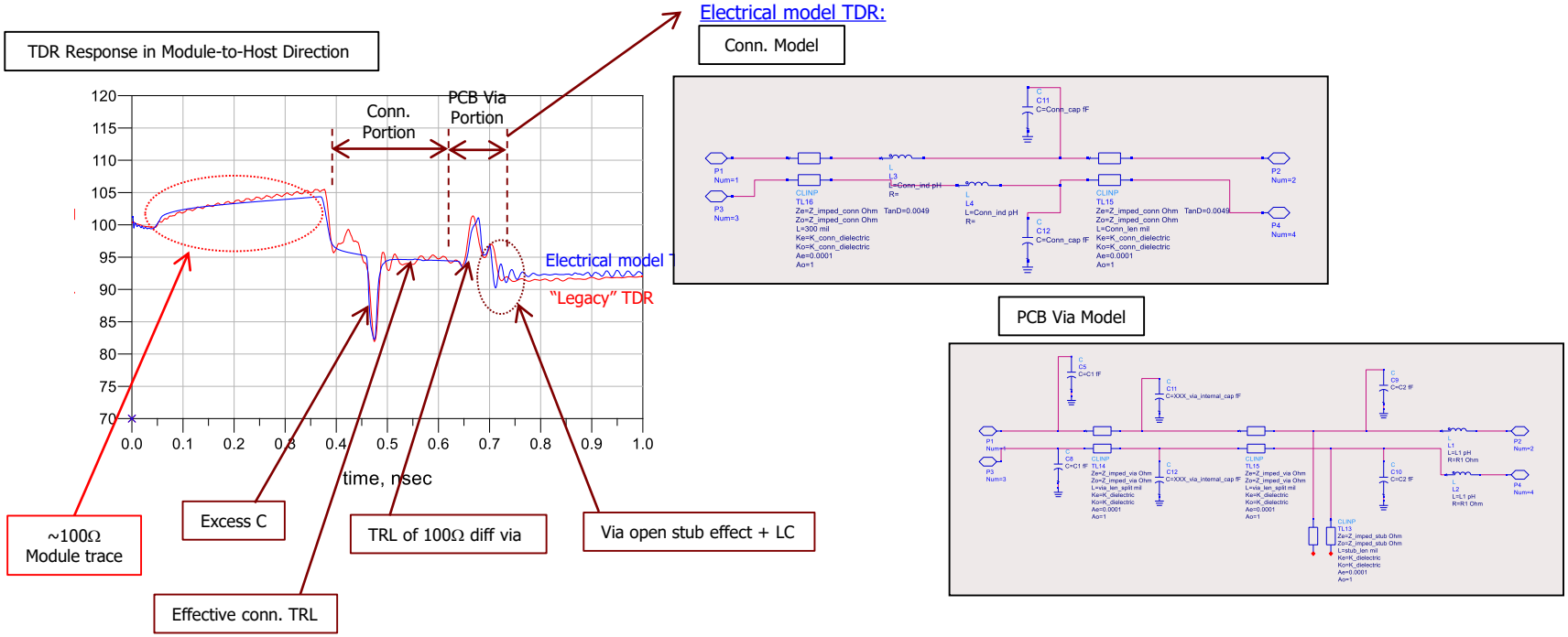
❑ Overlaying model S11 on channel S11



Appears that channel S11 performance is dominated by the via transition from 15-45 GHz !!

Module connector/via transition modeling

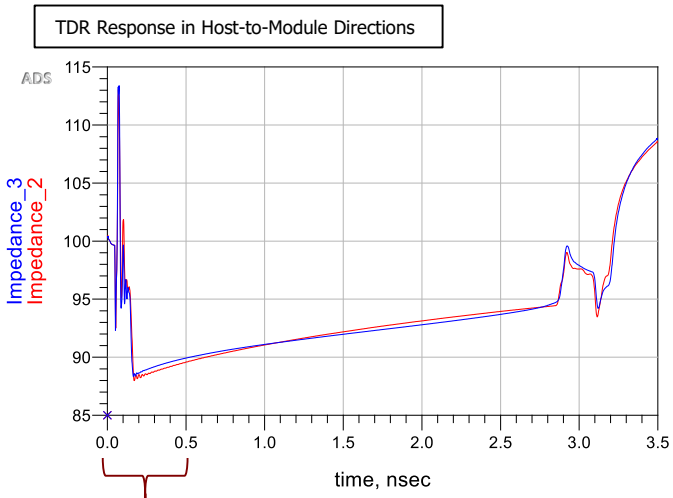
- **Creating an equivalent electrical model of the module connector/via region:**

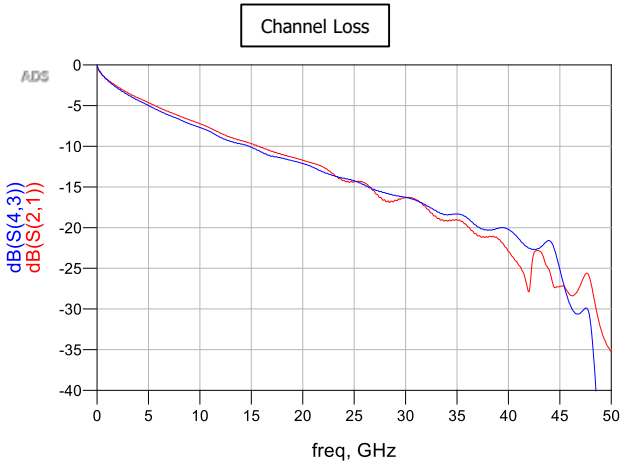


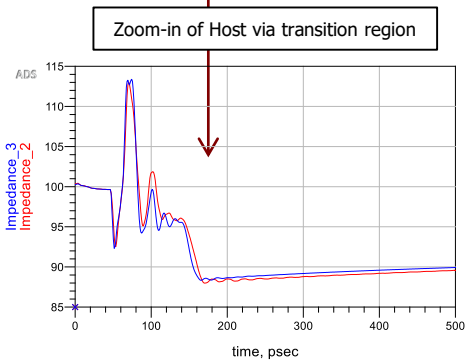
- **Observations:**
  - Connector “effective TRL” has 95Ω differential impedance
  - Connector seems to show a capacitive discontinuity
  - Module PCB via model approx. matches host via model

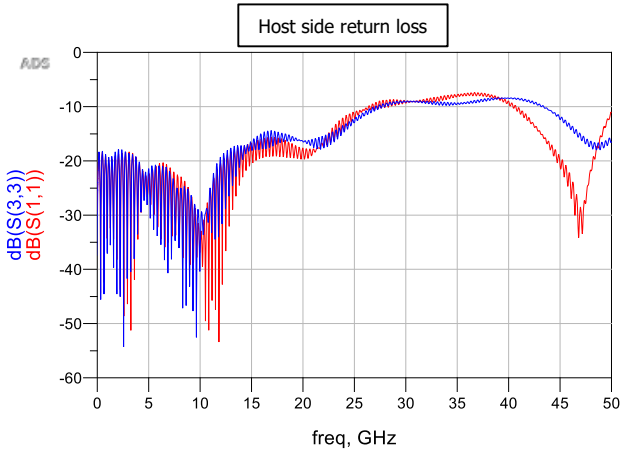
Electrical equivalent channel model responses vis-à-vis S-parameter channel

- Red curves – “legacy” channel
- Blue – Electrical equivalent model









Baseline COM setup

- COM results generated using com_ieee8023_93a_270.m
- Baseline COM excel configuration table in Backup section of this presentation for TP1a test point
- Equalization based on 3-tap Tx FIR (pre, main, post) and 5-tap Rx FFE (all post-cursors)
- Two test cases for Tx host package: z_p =12mm, z_p=31mm
- Comparing “legacy” with electrical equivalent channel performance with and without crosstalk

Channel Description	With Cross talk	FOM_ILD (dB)	12mm pack. VEC (dB)	12mm pack. COM (dB)	31mm pack. VEC (dB)	31mm pack. COM (dB)
“legacy” channel	No	0.174	8.17	4.30	9.76	3.42
	Yes		9.95	3.84	10.6	3.05
“equiv. electrical” channel	No	0.196	9.77	3.68	11.2	2.79
	Yes		10.1	3.27	12.1	2.47

- Equivalent electrical channel results show ~0.6dB degradation in COM performance wrt “legacy” channel
- Reasonable agreement between measured and modeled and looking for relative degradations which are important in overall understanding

Degradations from various channel discontinuities at TP1a

- Using the baseline electrical equivalent model and removing various channel transitions tells us the following:

Channel Description	Channel Construction	With Cross talk	FOM_ILD (dB)	12mm pack. VEC (dB)	12mm pack. COM (dB)	31mm pack. VEC (dB)	31mm pack. COM (dB)
“equiv. electrical” channel	Complete channel	Yes	0.196	10.1	3.27	12.1	2.47
“equiv. electrical” channel	Channel less host via transition	Yes	0.201	7.95	4.44	9.20	3.70
“equiv. electrical” channel	Channel less connector transition	Yes	0.131	8.44	4.13	9.78	3.41
“equiv. electrical” channel	Channel less host via and conn transitions	Yes	0.102	6.42	5.64	7.54	4.73

- Results indicate that host via and module connector transitions are approximately equally complicit in overall channel degradation

Effect of host channel length on performance at TP1a

- Decreasing electrical channel length to from ~6.8” to 0.5”

Channel Description	Channel Construction	With Cross talk	FOM_ILD (dB)	12mm pack. VEC (dB)	12mm pack. COM (dB)	31mm pack. VEC (dB)	31mm pack. COM (dB)
“equiv. electrical” channel	Complete channel – ~6.8” host trace	Yes	0.196	10.1	3.27	12.1	2.47
“equiv. electrical” channel	Channel with 4” host trace	Yes	0.188	7.10	5.06	8.15	4.71
“equiv. electrical” channel	Channel with 2” host trace	Yes	0.195	7.28	4.93	8.06	4.37
“equiv. electrical” channel	Channel with 1” host trace	Yes	0.210	6.61	5.46	7.90	4.48
“equiv. electrical” channel	Channel with 0.5” host trace	Yes	0.219	9.44	3.57	9.12	3.74

- Shortest host trace has performance similar to long trace
- Best COM margin obtained for the 4” host trace case

Degradations from various channel discontinuities at TP1a for very short channel

- **Using the baseline 0.5” host trace electrical equivalent model and removing various channel transitions tells us the following:**

Channel Description	Channel Construction	With Cross talk	FOM_ILD (dB)	12mm pack. VEC (dB)	12mm pack. COM (dB)	31mm pack. VEC (dB)	31mm pack. COM (dB)
“equiv. electrical” channel	Complete channel	Yes	0.219	9.44	3.57	9.12	3.74
“equiv. electrical” channel	Channel less host via transition	Yes	0.210	7.43	4.81	8.39	4.16
“equiv. electrical” channel	Channel less connector transition	Yes	0.095	6.25	5.81	6.55	5.49
“equiv. electrical” channel	Channel less host via and conn transitions	Yes	0.038	4.19	8.35	5.01	7.16

- **Indication that for very short channels the connector interface impacts performance more significantly than the host via interface**

Tuning approaches for long PCB vias

- **There are several common techniques for tuning or optimizing via structures for high frequency performance**

- **Some examples include tuning by varying via antipad diameters to change effective via capacitances within the fF range. Also, terminating open via stubs into some impedance to minimize reflections is also a possibility**

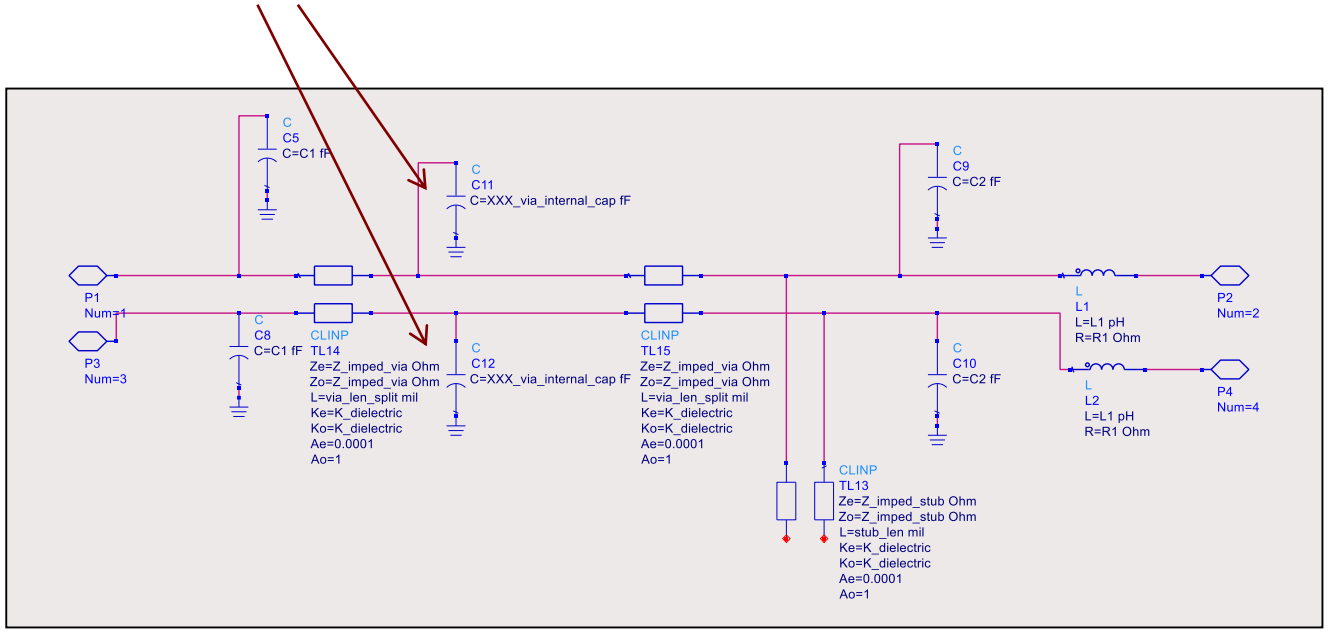
  (e.g. see Sanmina-SCI "Matched Terminated Stub VIA Technology for Higher Bandwidth Transmission in Line Cards and Back Planes", 2008)

- **It may be possible to optimize the long vias a little bit better to buy back some performance, specifically the vias at the host interface and potentially the vias at the module connector interface**

- **The following slides discuss one approach in more detail**

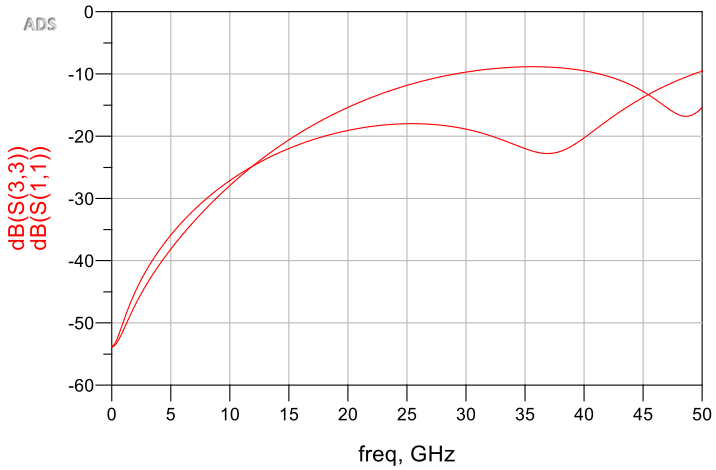
Possible gains from improving host via interface (1/3)

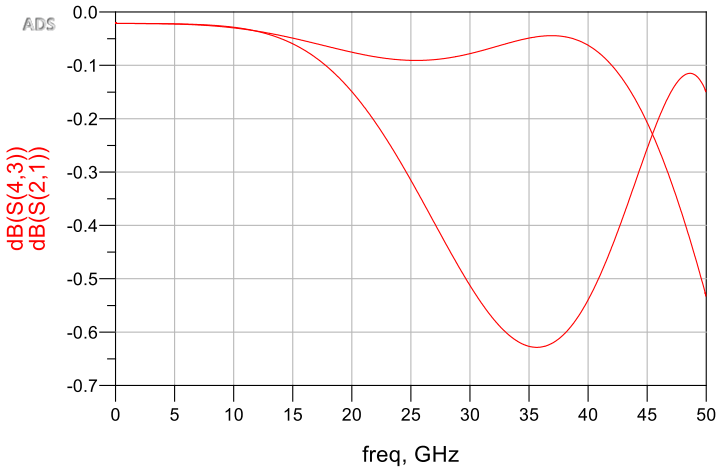
- **Host via appears to be inductive with a differential impedance of ~ 114Ω**
- **Perhaps some additional parasitic capacitance could be added by reducing the size of via antipad(s)**
  - Addition of 40fF significantly improves electrical model via performance



Possible gains from improving host via interface (2/3)

- **Improvement in via transition can be significant:**





Possible gains from improving host via interface (3/3)

- **Running COM on 6.8” and 0.5” channels with improved via performance yields:**

Channel Description	Channel Construction	With Cross talk	FOM_ILD (dB)	12mm pack. VEC (dB)	12mm pack. COM (dB)	31mm pack. VEC (dB)	31mm pack. COM (dB)
6.8” “equiv. electrical” channel	Baseline channel	Yes	0.196	10.1	3.27	12.1	2.47
6.8” “equiv. electrical” channel	Baseline channel with improved vias	Yes	0210	8.77	3.93	10.0	3.28
0.5” “equiv. electrical” channel	Baseline channel	Yes	0.219	9.44.	3.57	9.12	3.74
0.5” “equiv. electrical” channel	Baseline channel with improved vias	Yes	0.232	8.17	4.30	8.88	3.87

- **Higher performing vias on 6.8” channel yield a COM improvement of 0.6 - 0.8dB**
- **For the very short 0.5” channel COM improvements are only significant for the 12mm package (i.e. ~ 0.7dB)**
  - COM is passing here already

Summary and recommendations

- **One of the more “difficult” channels from the submitted electrical channels has been analysed and an equivalent circuit model generated.**
  - Good agreement shown between measured and modelled channel
- **Discontinuities associated with vias and connectors appear to have the most impact on COM.**
  - Reflections appear to be more important than loss
- **Channel improvements are possible and need to be considered for power saving.**
  - Capacitive tuning
  - Stub termination
- **With channel improvements, 5 tap FFE is sufficient**
  - No DFE required
  - No pre-cursors required
  - Keeping the channel equalization simple will keep the power dissipation lower
- **100G C2M should consider adopting a nominal 85Ω channel impedance as this appears to be used in practice**

Backup Material

COM Parameters Table for TP1a simulations

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0.1 0.1; 0.1 0.1]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.5		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	0		[min:step:max]
c(-3)	0		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

ffe_pre_tap_len	**0**	UI
ffe_post_tap_len	4	UI
ffe_tap_step_size	0	
fe_main_cursor_mi	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.125	
ffe_backoff	0	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	0	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
N_f	0	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps

yellow indicates WIP

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Thank You!