C2M Simulations with T-Coil Model

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Overview

- **Channel investigated are Lim 3/19 802.3ck channels**
- **COM analysis at TP1a, TP4, and TP5 with Lim channels**
  - Previously COM analysis were only with RC model
    - See ghiasi_3ck_01b_0519.pdf
  - Updated COM results also include T-Coil model
- **Best choice for reference equalizer**
- **Summary**

COM Code 2.70 Host-Module TP1a

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[15 30; 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	232	mm
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	232	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	232	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	4	UI			N_bx	4	UI				
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	1										

COM Code 2.70 Host-Module Slicer Input

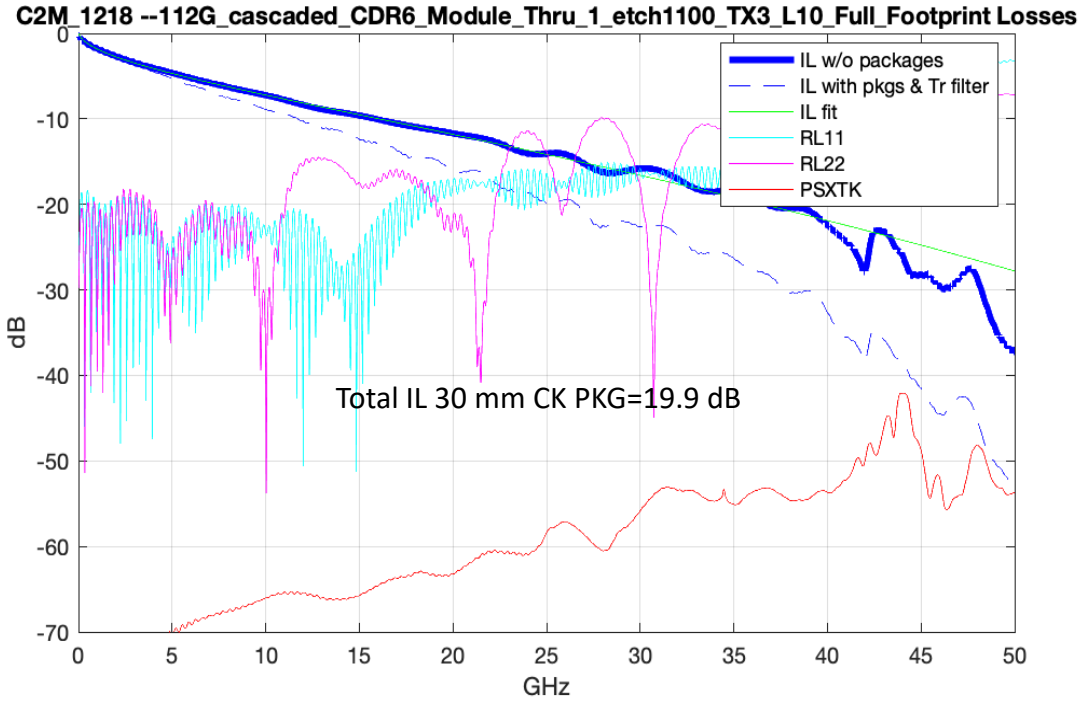
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0.85e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[15 30; 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	50	mm
z_p (RX)	[2 8 ; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	50	mm
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.9	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	1	UI			N_bx	4	UI				
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.35										
ffe_post_tap1_max	0.35										
ffe_tapn_max	0.2										
ffe_backoff	1										

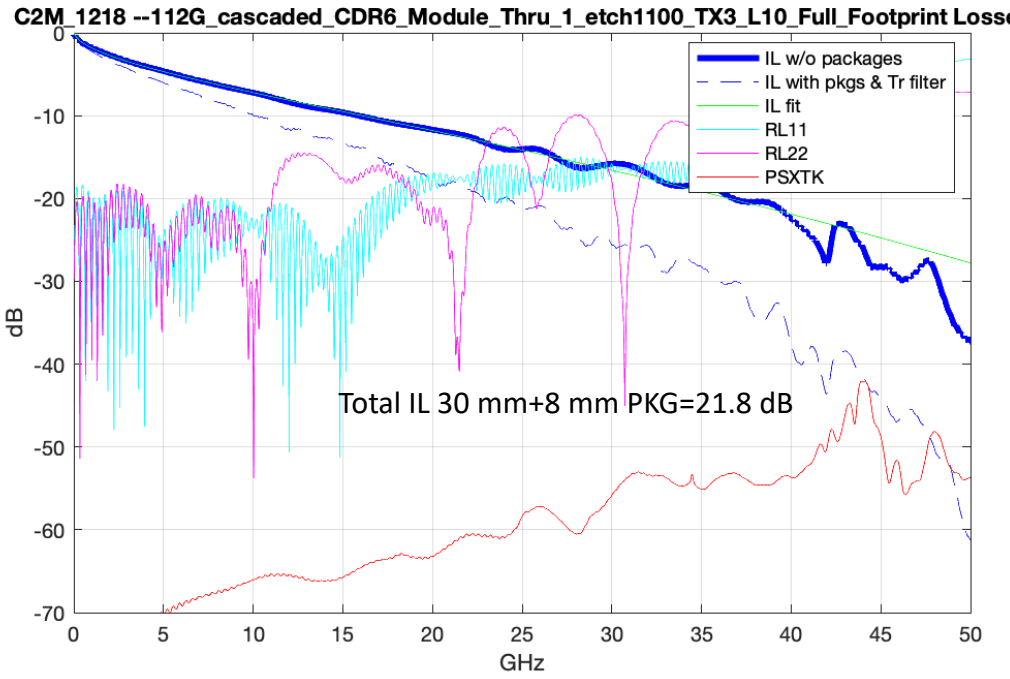
COM Analysis on Lim Channel 3 – ASIC to Module

- **Lim channel 3 (short via) Legacy QSFP-dd contacts includes retimer foot print at TP1a and slicer input**

TP1a FOM_ILD=0.2, ICN=0.77 mV, ICR=43, ERL11=16.5, ERL22=10.5
5T FFE: COM=6.3 (5.5) dB, EH=19.3 (14.5) mV, VEC=5.7 (6.5) dB
TX FIR [0.02, -0.14, 0.84, 0] Optimum
5T FFE(4 post)+1DFE: COM=6.4 (6.0) dB, EH=26.6 (21.8) mV, VEC=6.0 (6.0) dB
TX FIR [0.02, -0.14, 0.82, -0.02] Optimum
4DFE: COM=6.4 (5.8) dB, EH=20.5 (18.4) mV, VEC=6.6 (6.2) dB
TX FIR [0.02, -0.14, 0.84, 0] Optimum

Slicer Input FOM_ILD=0.2, ICN=0.77 mV, ICR=43, ERL11=16.5, ERL22=10.5
5T FFE: COM=4.7 (4.6) dB, EH=12.4 (12.6) mV, VEC=7.6 (7.6) dB
TX FIR [0.02, -0.14, 0.74, -0.1] Optimum
5T FFE(4 post)+1DFE: COM=5.3 (5.3) dB, EH=21.4 (17.0) mV, VEC=6.8 (6.7) dB
TX FIR [0.04, -0.2, 0.76, 0] Optimum
4DFE: COM=5.0 (5.3) dB, EH=18.1 (15.4) mV, VEC=7.1 (6.8) dB
TX FIR [0.02, -0.14, 0.84, -0.02] Optimum





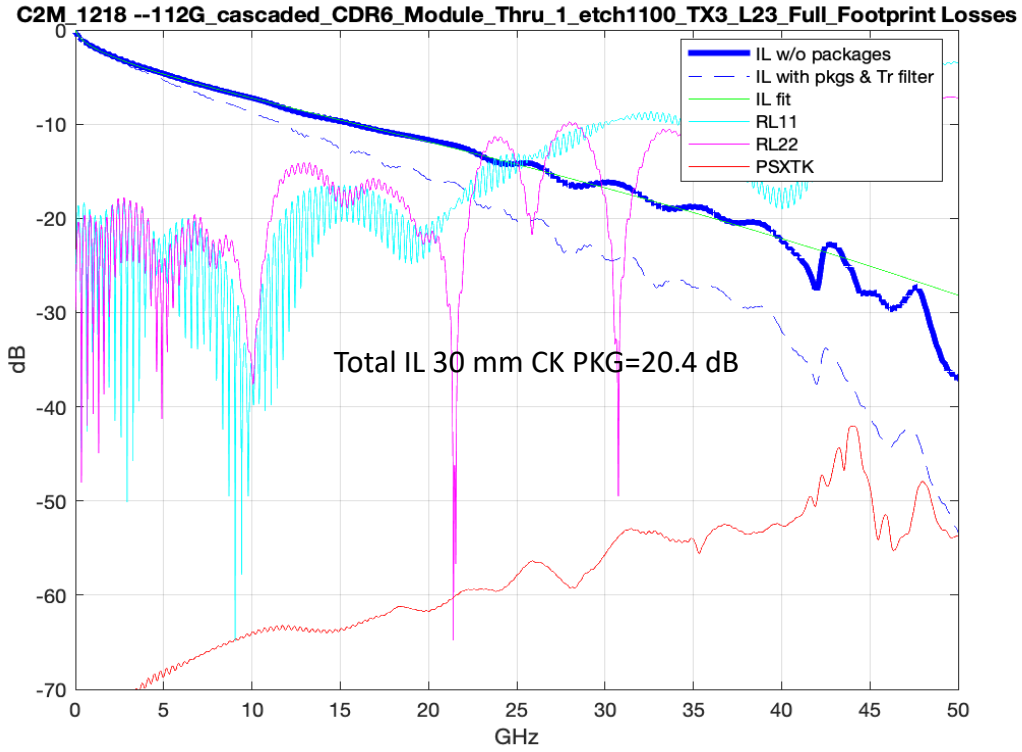
Result in x(y) are for 15(30) mm PKG.

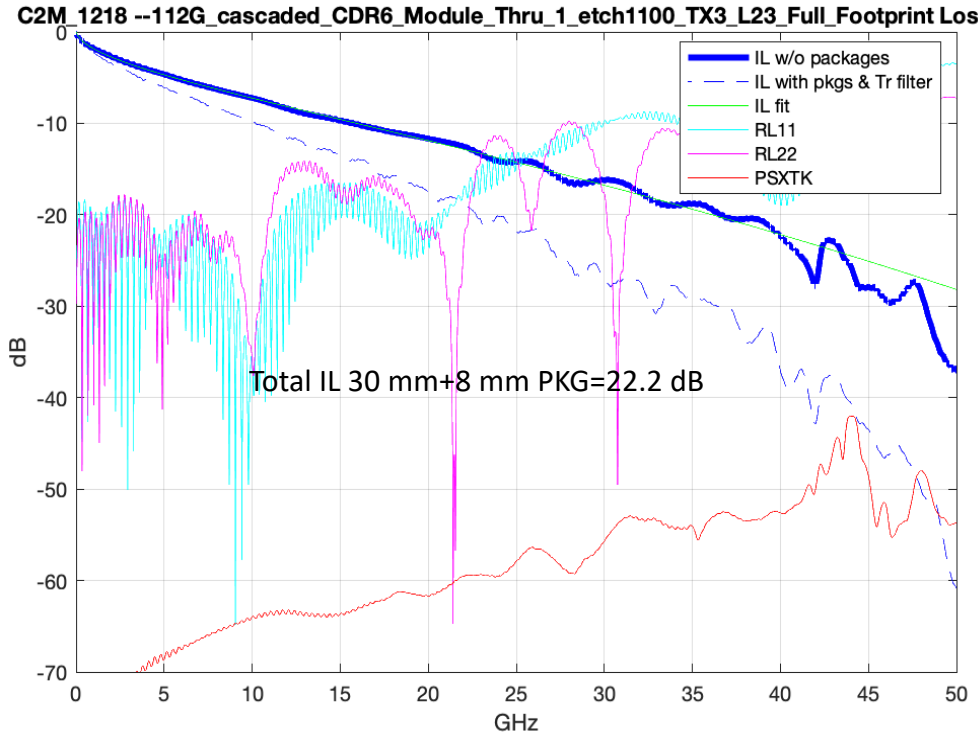
COM Analysis on Lim Channel 4 – ASIC to Module

- **Lim channel 4 (long via) Legacy QSFP-dd contact includes retimer foot print at TP1a and slicer input**

TP1a, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, , ERL11=15.2, ERL22=10.4
5T FFE(4 post): COM=5.9 (4.8) dB, EH=17.5 (12.7) mV, VEC=6.2 (7.4) dB
TX FIR[-0.02, -0.14, 0.82, 0.02] Optimum
5T FFE(4 post)+1DFE: COM=6.1 (5.4) dB, EH=18.6 (20.3) mV, VEC=5.9 (6.7) dB
TX FIR[-0.02, -0.14, 0.84, 0] Optimum
4DFE: COM=6.1 (5.3) dB, EH=20.3 (16.6) mV, VEC=6.9 (6.8) dB
TX FIR[-0.02, -0.14, 0.84, 0] Optimum

Slicer Input, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, , ERL11=15.2, ERL22=10.4
5T FFE(4 post): COM=4.3 (4.2) dB, EH=11.1 (10.3) mV, VEC=8.1 (8.2) dB
TX FIR[-0.04, -0.18, 0.72, -0.06] Optimum
5T FFE(4 post)+1DFE: COM=4.8 (5.1) dB, EH=19.6 (16.1) mV, VEC=7.4 (7.1) dB
TX FIR[-0.02, -0.16, 0.84, 0] Optimum
4DFE: COM=4.8 (4.9) dB, EH=13.3 (15.4) mV, VEC=7.3 (7.5) dB
TX FIR[-0.02, -0.14, 0.84, 0] Optimum



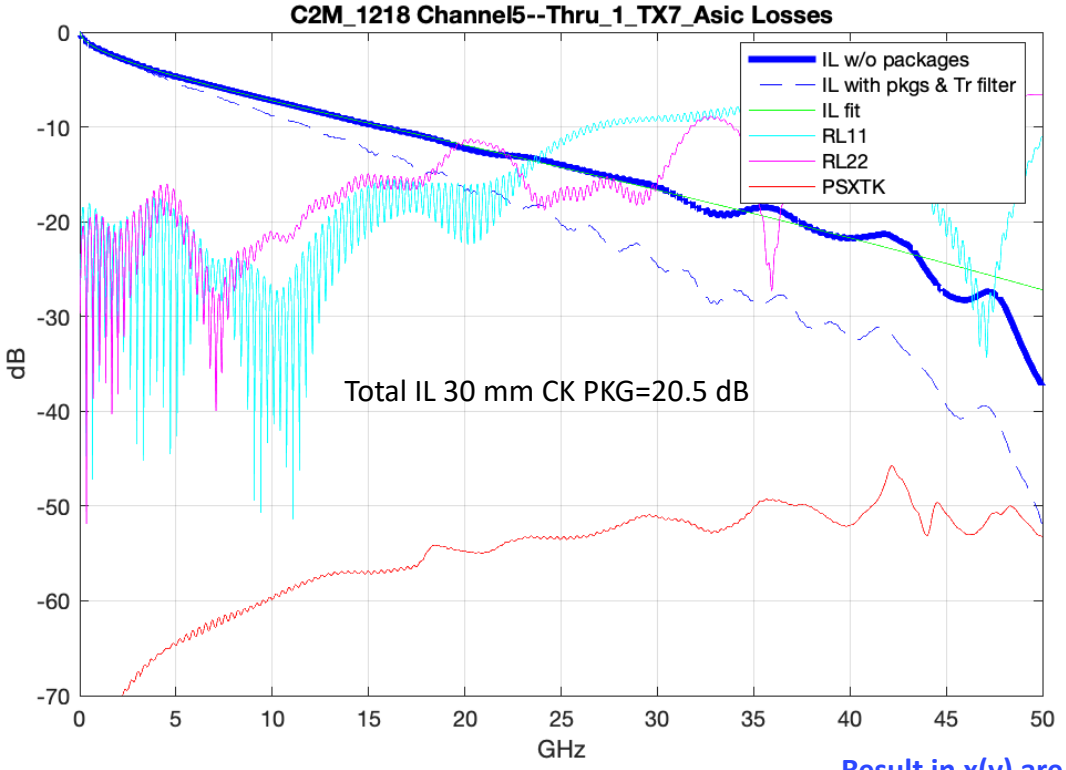


Result in x(y) are for 15(30) mm PKG.

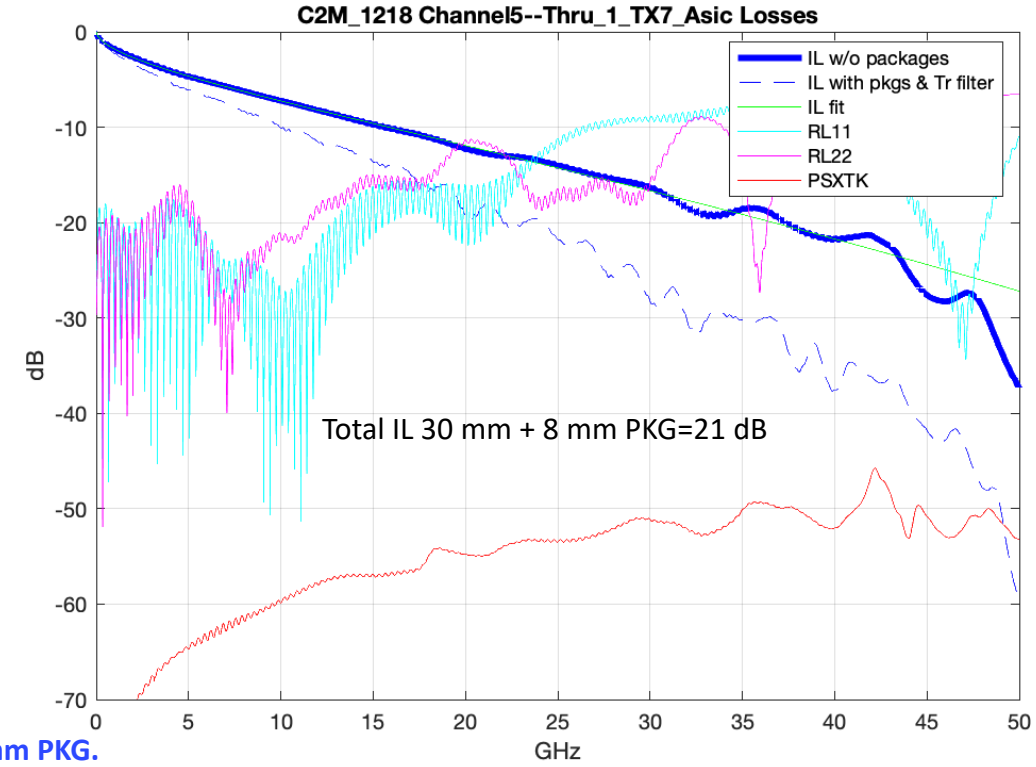
COM Analysis on Lim Channel 5 - ASIC-Module

- **Lim channel 6 both with Legacy QSFP-dd contacts includes ASIC foot print at TP1a and slicer input.**

TP1a, FOM_ILD=0.16, ICN=1.4 mV, ICR=38.2 dB, , ERL11=15.5, ERL22=9.9
5T FFE(4 post): COM=5.8 (4.3) dB, EH=17.9 (14.5) mV, VEC=6.2 (8.2) dB
Optimum TX FIR[0.04, -0.18, 0.78, 0]
5T FFE(4 post)+1DFE COM=6.2 (5.4) dB, EH=24.5 (20.3) mV, VEC=5.8 (6.6) dB
Optimum TX FIR[0.04, -0.2, 0.76, 0]
4DFE: COM=6.0 (5.1) dB, EH=14.1 (16.1) mV, VEC=7.9 (7.1) dB
Optimum TX FIR[0.04, -0.14, 0.84, 0]



Slicer input, FOM_ILD=0.16, ICN=1.4 mV, ICR=38.2 dB, , ERL11=15.5, ERL22=9.9
5T FFE(4 post): COM=5.5 (2.2) dB, EH=18.1 (6.5) mV, VEC=7.2 (13.0) dB
Optimum TX FIR[0.02, 0.18, 0.84, 0]
5T FFE(4 post)+1DFE: COM=3.7 (4.8) dB, EH=19.7 (14.4) mV, VEC=7.8 (7.5) dB
Optimum TX FIR[0.04, -0.2, 0.76, 0]
4DFE: COM=3.5 (4.5) dB, EH=12.0 (13.4) mV, VEC=9.5 (7.9) dB
Optimum TX FIR[0.04, -0.2, 0.76, 0]

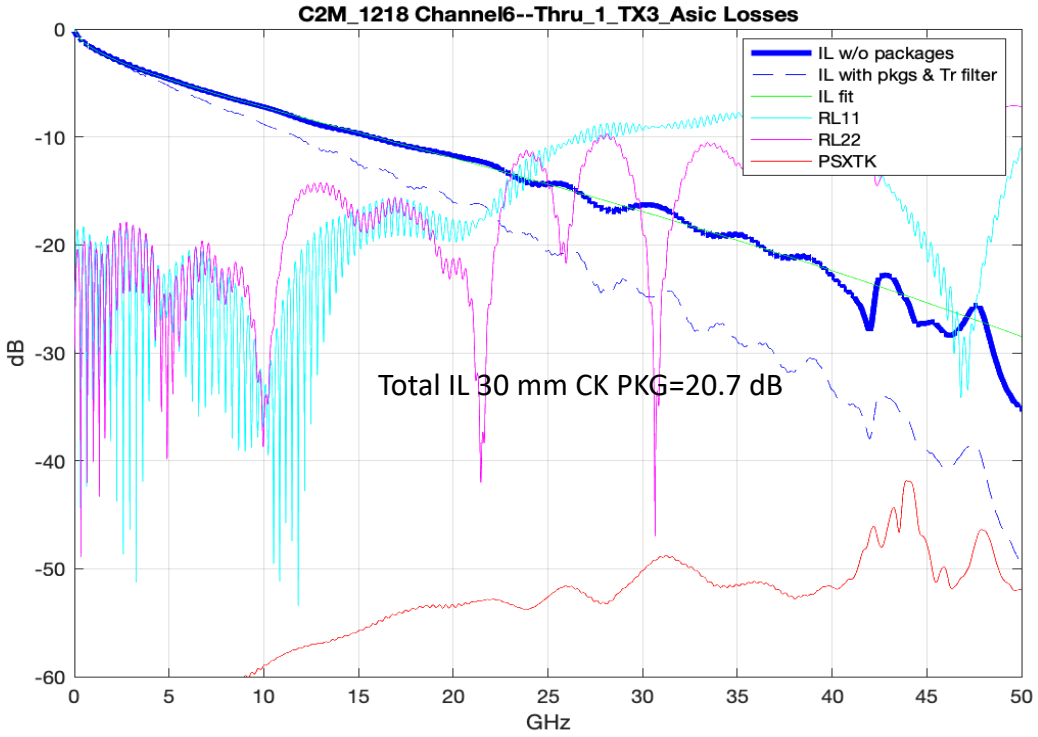


Result in x(y) are for 15(30) mm PKG.

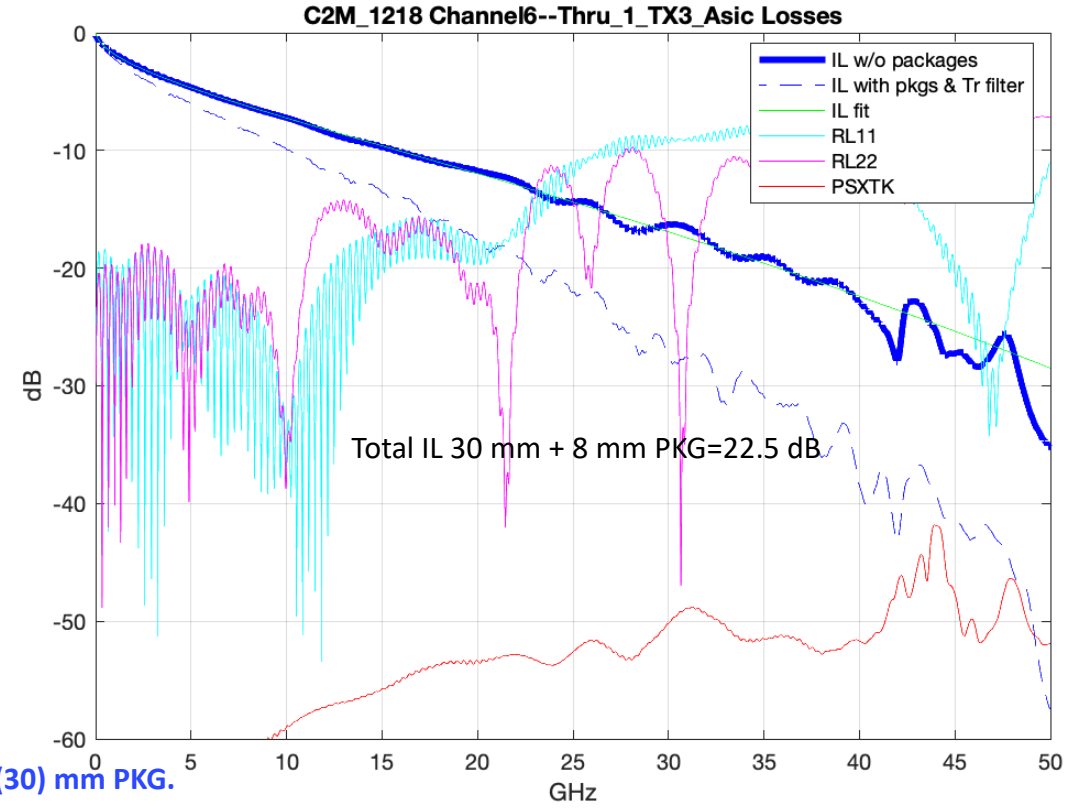
COM Analysis on Lim Channel 6 - ASIC-Module

- **Lim channel 5 QSFP-dd new contact with Legacy QSFP-dd contacts includes ASIC foot print at TP1a and slicer input.**

TP1a, FOM_ILD=0.17, ICN=1.6 mV, ICR=36.8 dB, , ERL11=15.8, ERL22=10.4
5T FFE(4 post): COM=4.8 (4.0) dB, EH=14.0 (10.6) mV, VEC=7.4 (8.7) dB
TX FIR[0.04, -0.18, 0.76, -0.02] Optimum
5T FFE(4 post)+1DFE: COM=5.6 (5.1) dB, EH=23.4 (19.2) mV, VEC=6.4 (7.0) dB
TX FIR[0.04, -0.2, 0.76, 0] Optimum
4DFE: COM=5.6 (4.9) dB, EH=18.3 (15.8) mV, VEC=6.4 (7.3) dB
TX FIR[0.02, -0.14, 0.84, 0] Optimum



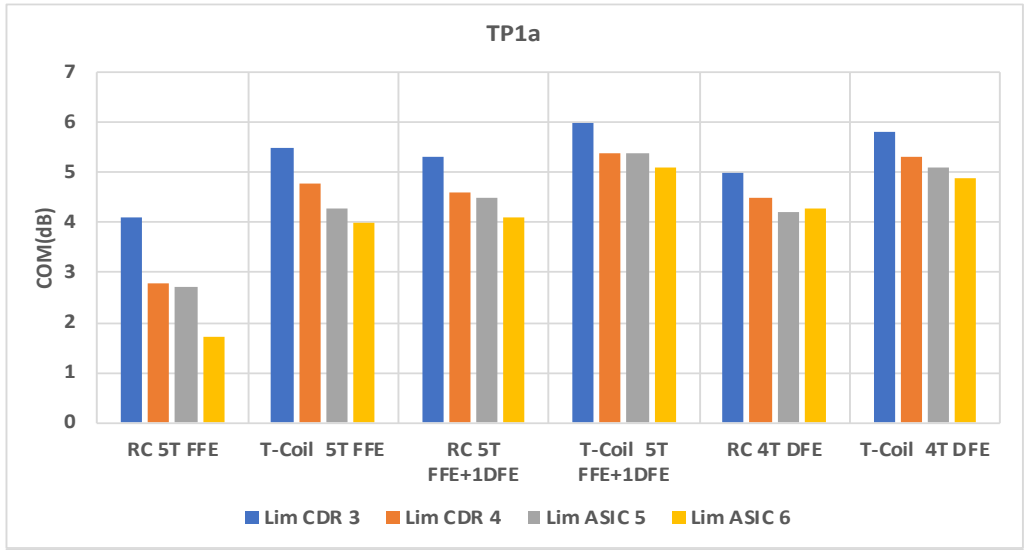
Slicer Input, FOM_ILD=0.17, ICN=1.6 mV, ICR=38.2 dB, , ERL11=15.8, ERL22=10.5
5T FFE(4 post): COM=3.5 (3.8) dB, EH=9.3 (8.6) mV, VEC=9.5 (9.9) dB
TX FIR [0.04, -0.18, 0.72, -0.06] Optimum
5T FFE(4 post)+1DFE: COM=4.6 (4.9) dB, EH=18.7 (15.1) mV, VEC=7.6 (7.3) dB
TX FIR[0.04, -0.20, 0.76, 0] Optimum
4DFE: COM=4.5 (4.6) dB, EH=14.5 (13.1) mV, VEC=7.9 (7.7) dB
TX FIR[0.04, -0.18, 0.78, 0] Optimum

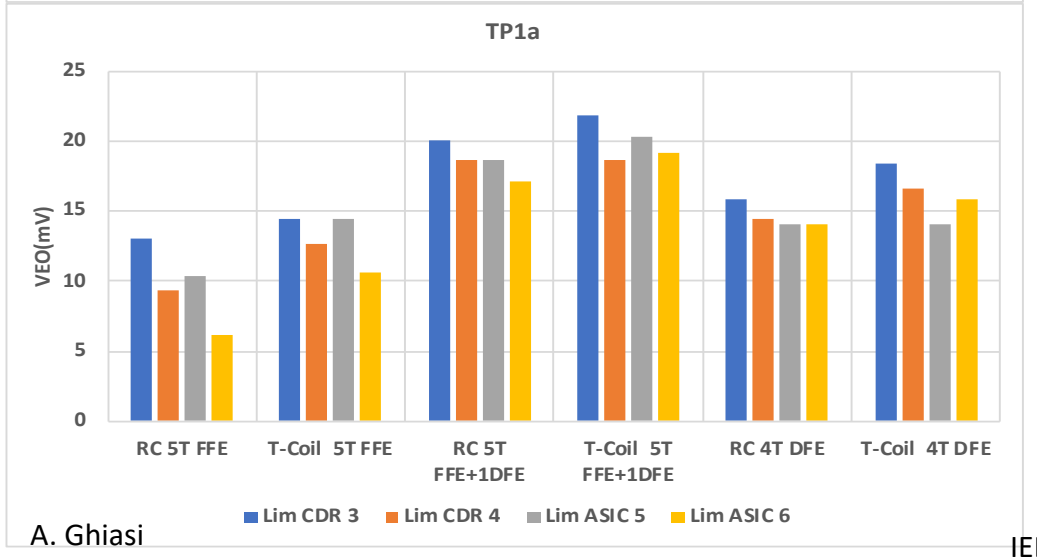


Result in x(y) are for 15(30) mm PKG.

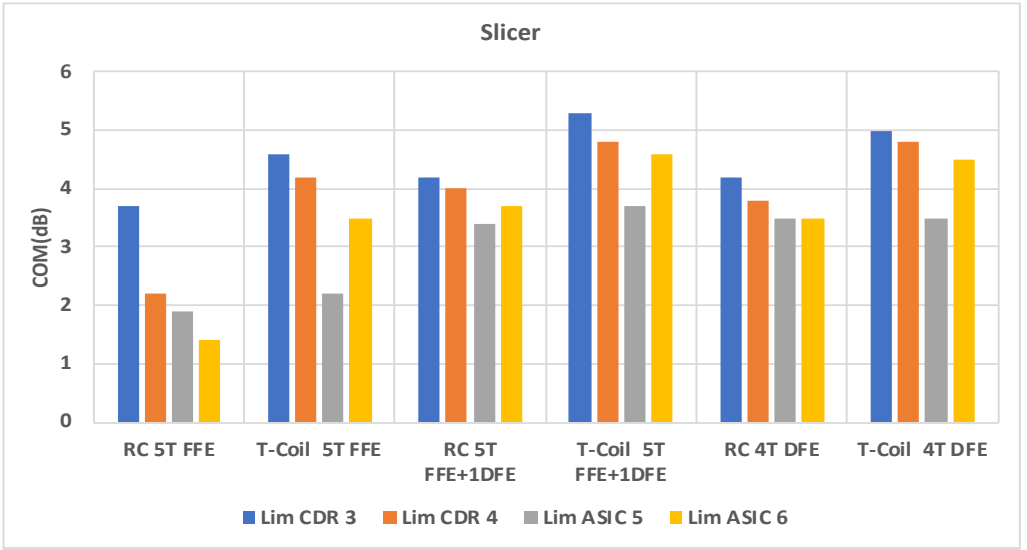
Comparisons of RC vs T-Coil Model for Lim Channels TP1a Direction

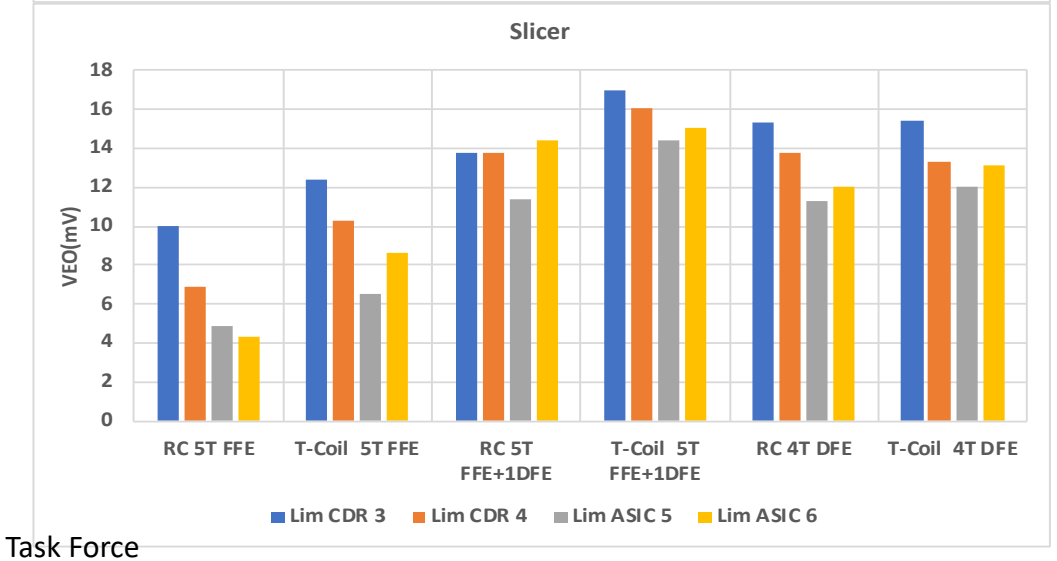
Slicer Results with RC and T-Coil TX (Ls=100 pH, Cb=30 ff, Cd=120 ff)





Slicer Results with RC and T-Coil TX (Ls=100 pH, Cb=30 ff, Cd=120 ff)





COM 2.70 Module to Host TP5 RC Model (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[0.85e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0 0]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	220	mm
z_p (RX)	[0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	220	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	220	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

COM 2.70 Module to Host TP5 T-Coil Model (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.1 0]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	220	mm
z_p (RX)	[0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	220	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	220	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

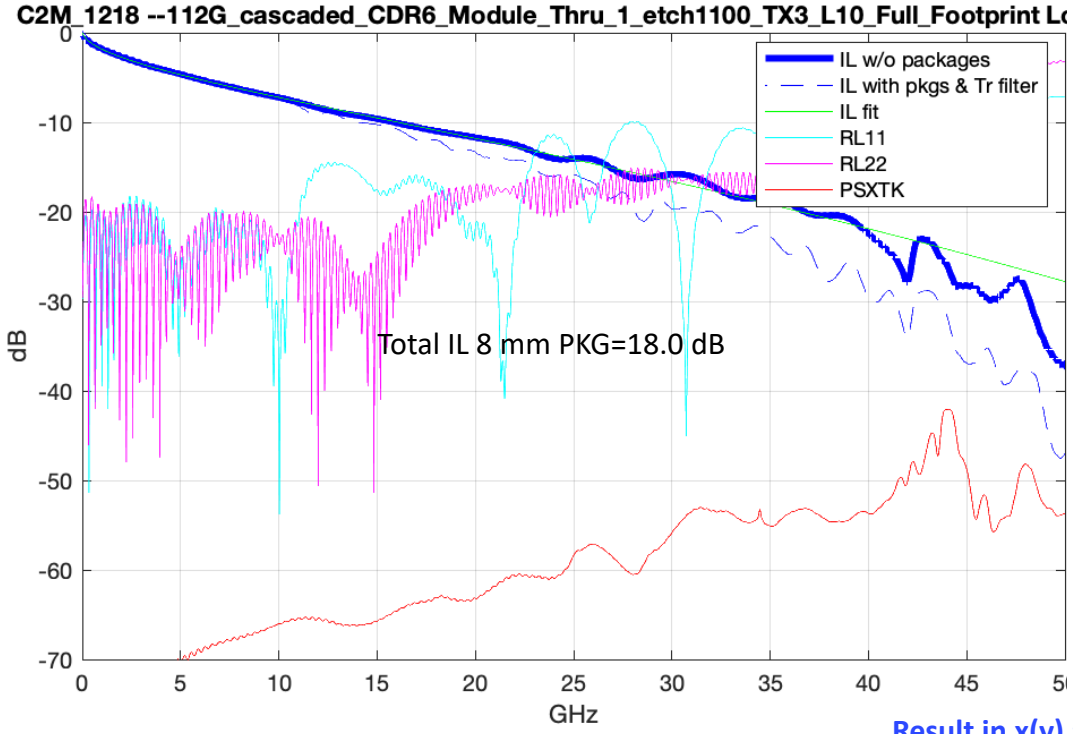
COM 2.70 Module to Host Slicer Input (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm
C_d	[0.85e-4 1.2e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0 0.12]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8; 0.01 0.01]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8; 0.01 0.01]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8; 0.01 0.01]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	50	mm
z_p (RX)	[15 30; 1.8 1.8]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	50	mm
C_p	[0.65e-4 0.87e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.8	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	1	UI			N_bx	4	UI				
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.2										
ffe_backoff	1										

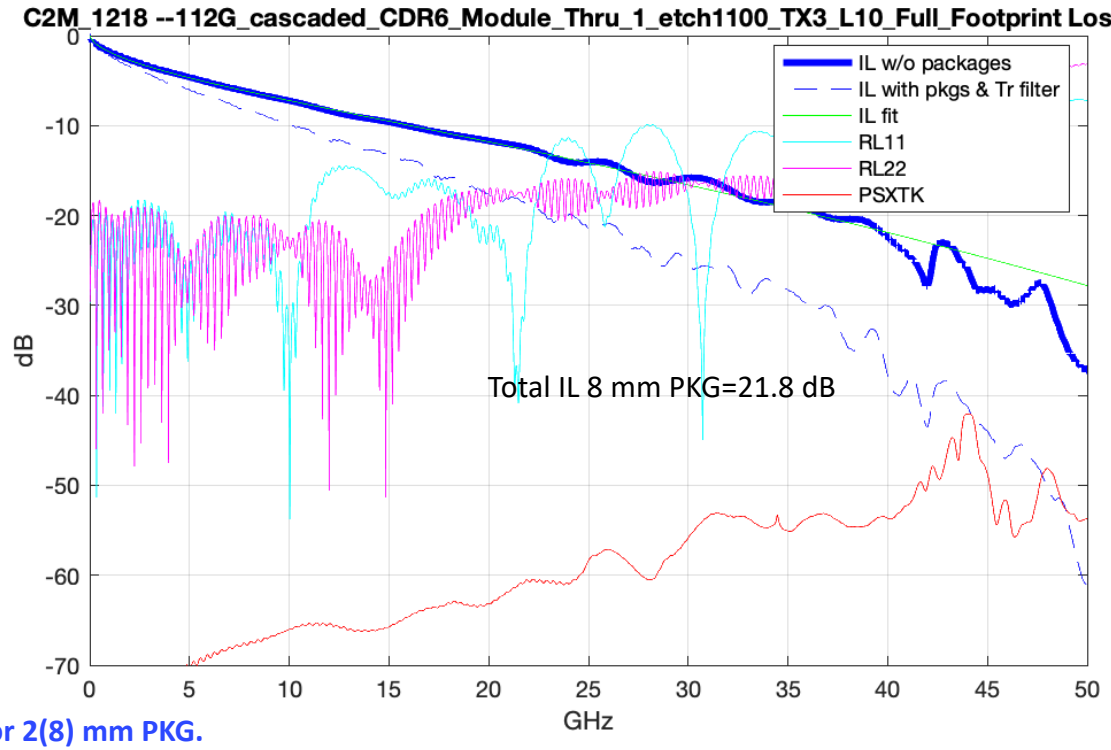
COM Analysis on Lim Channel3 – Module to ASIC TP5

- **Lim channel 3 (short via) Legacy QSFP-dd contacts include retimer foot print at TP5 and slicer input**

TP5, FOM_ILD=0.2, ICN=0.77 mV, ICR=43 dB, ERL11=10.8, ERL22=15.2
5T FFE: COM=6.2 (5.7) dB, EH=20.7 (18.9) mV, VEC=5.8 (6.4) dB
TX FFE [0.02, -0.14, 0.78, -0.06] Optimum
5T FFE+1DFE: COM=6.5 (6.0) dB, EH=30.7 (27.1) mV, VEC=5.5 (6.0) dB
TX FFE[0.04, -0.18, 0.78,0] Optimum
4T DFE: COM=6.4 (5.8) dB, EH=26.8 (23.2) mV, VEC=6.4 (6.2) dB
TX FFE[0.04, -0.18, 0.78, 0] Optimum



Slicer Input, FOM_ILD=0.2, ICN=0.77 mV, ICR=43 dB, ERL11=10.7, ERL22=15.2
5T FFE: COM=4.7 (4.6) dB, EH=12.3 (12.3) mV, VEC=7.6 (7.7) dB
TX FFE [0.02, -0.14, 0.74, -0.1] Optimum
5T FFE+1T DFE: COM=5.3 (5.4) dB, EH=21.4 (17.0) mV, VEC=6.8 (6.7) dB
TX FFE[0.04, -0.16, 0.82,0] Optimum
4T DFE: COM=5.1 (5.3) dB, EH=17.8 (15.0) mV, VEC=7.1 (6.8) dB
TX FFE[0.04, -0.18, 0.78,0] Optimum



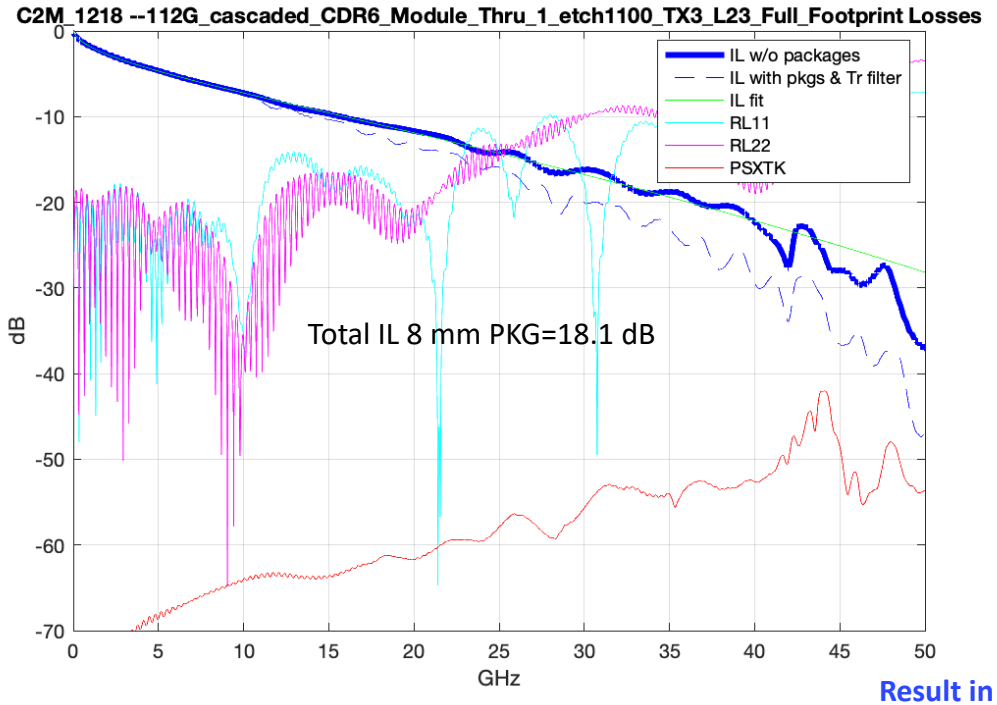
Result in x(y) are for 2(8) mm PKG.

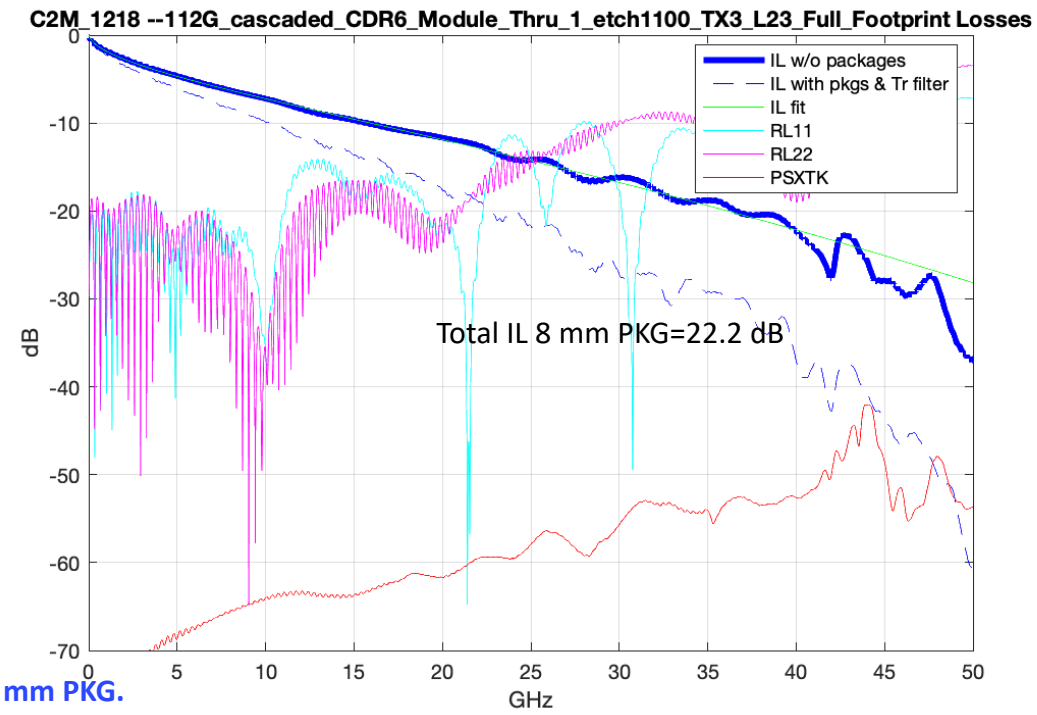
COM Analysis on Lim Channel 4 – Module to ASIC

- **Lim channel 4 (long via) Legacy QSFP-dd contact include retimer foot print at TP5 and slicer input**

TP5, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, ERL11=10.7, ERL22=14.5
5T FFE(4 post) TP5: COM=6.2 (5.7) dB, EH=21.1 (17.9) mV, VEC=5.9 (6.4) dB
TX FFE [0.02, -0.14, 0.8, -0.04] Optimum
5T FFE(4 post)+1T DFE : COM=6.4 (6.1) dB, EH=31.0(27.0) mV, VEC=5.7 (6.0) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum
4T DFE: COM=6.3 (5.9) dB, EH=25.8 (26.3) mV, VEC=5.7 (6.2) dB
TX FFE[0.04, -0.18, 0.78,0]

Slicer Input, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, ERL11=10.7, ERL22=14.2
5T FFE(4 post): COM=4.2 (4.2) dB, EH=10.9 (10.3) mV, VEC=8.3 (8.3) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum
5T FFE(4 post)+ 1T DFE : COM=4.8 (5.1) dB, EH=19.5 (16.0) mV, VEC=7.4 (7.1) dB
TX FFE[0.02, -0.16, 0.82,0] Optimum
4T DFE: COM=4.7 (4.9) dB, EH=15.3 (13.5) mV, VEC=7.5 (7.3) dB
TX FFE[0.04, -0.18, 0.78,0] Optimum



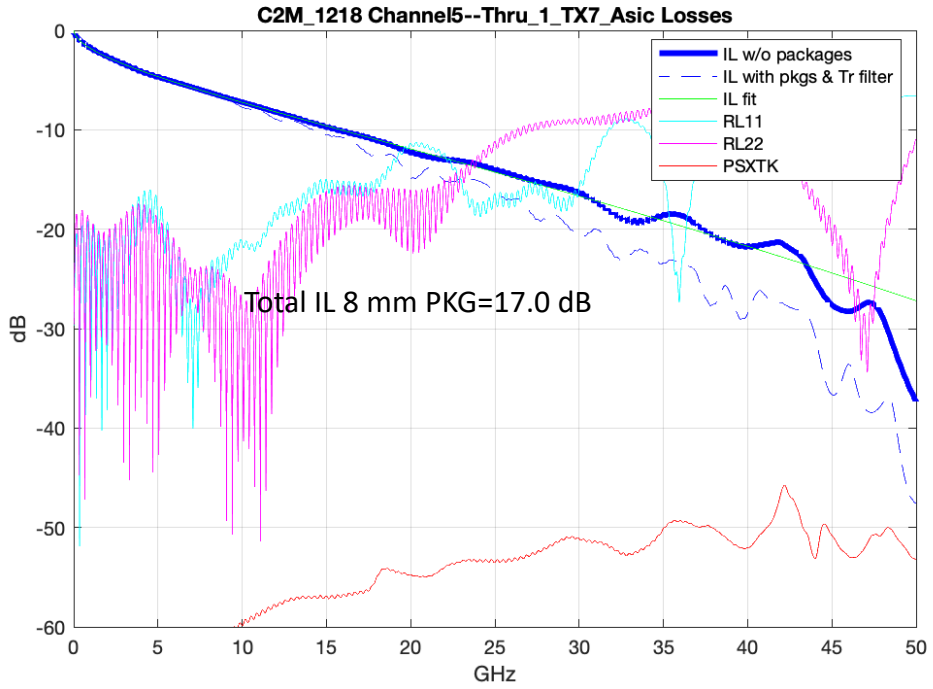


Result in x(y) are for 2(8) mm PKG.

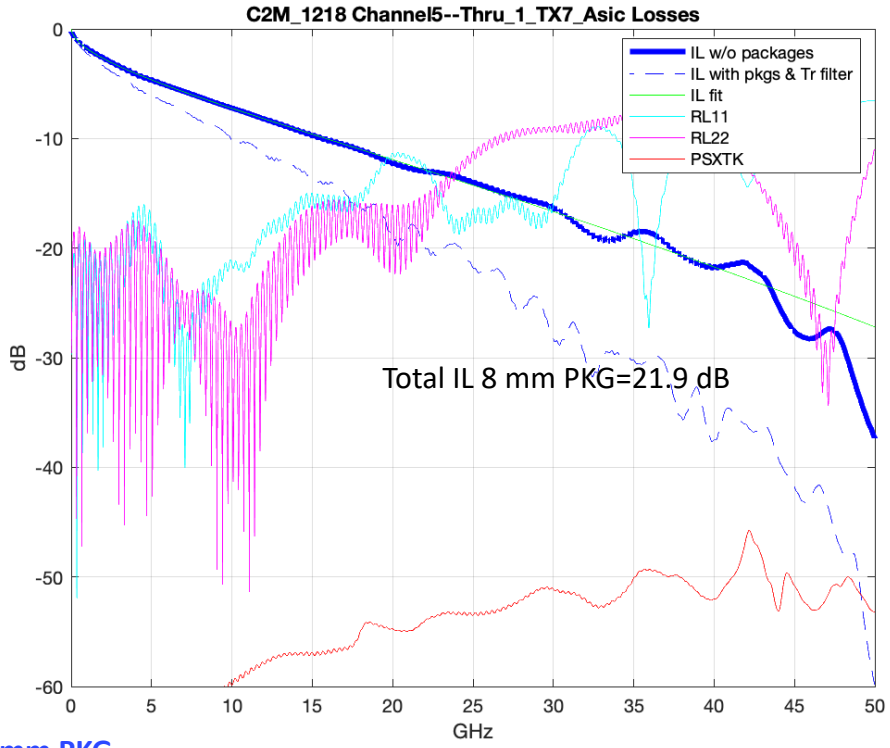
COM Analysis on Lim Channel 5 – Module to ASIC

- **Lim channel 5 QSFP-dd new contact includes ASIC foot print at TP5 and slicer input**

TP5, FOM_ILD=0.16, ICN=1.4 mV, ICR=38.2 dB, ERL11=10.1, ERL22=14.1
5T FFE: COM=5.0 (4.9) dB, EH=19.9 (17.9) mV, VEC=7.2 (7.4) dB
TX FFE [0.02, -0.14, 0.84, 0] Optimum
5T FFE+1T DFE: COM=5.8 (5.0) dB, EH=28.7 (26.8) mV, VEC=6.2 (6.5) dB
TX FFE[0.02, -0.14, 0.84,0] Optimum
4TDFE: COM=5.7 (5.5) dB, EH=27.6 (26.6) mV, VEC=6.4 (6.6) dB
TX FFE[0.02, -0.14, 0.84,0] Optimum



Slicer Input, FOM_ILD=0.16, ICN=1.4 mV, ICR=38.2 dB, ERL11=10.2, ERL22=14.2
5T FFE: COM=5.0 (2.2) dB, EH=16.0 (6.2) mV, VEC=7.2 (13) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum
5T FFE(4 post)+1T DFE: COM=5.5 (3.8) dB, EH=12 (20.6) mV, VEC=9.0(6.6) dB
TX FFE [0.04, -0.14, 0.78, 0] Optimum
4T DFE: COM=5.3 (3.9) dB, EH=16.4 (12.2) mV, VEC=6.8 (8.9) dB
TX FFE [0.02, -0.14, 0.84, 0] Optimum

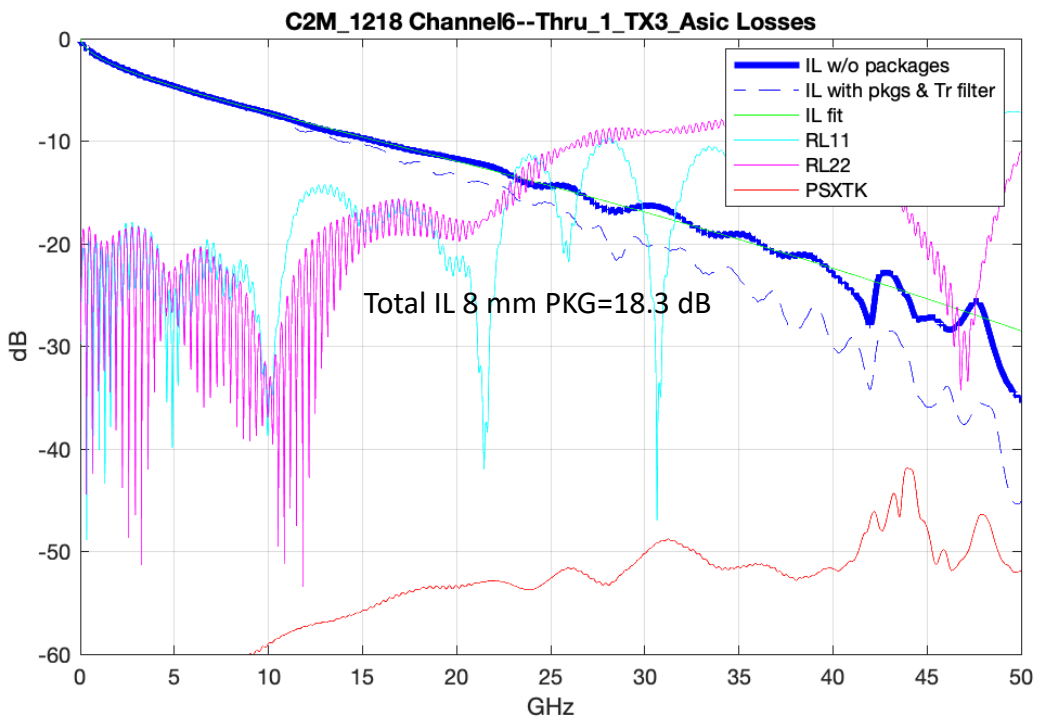


Result in x(y) are for 2(8) mm PKG.

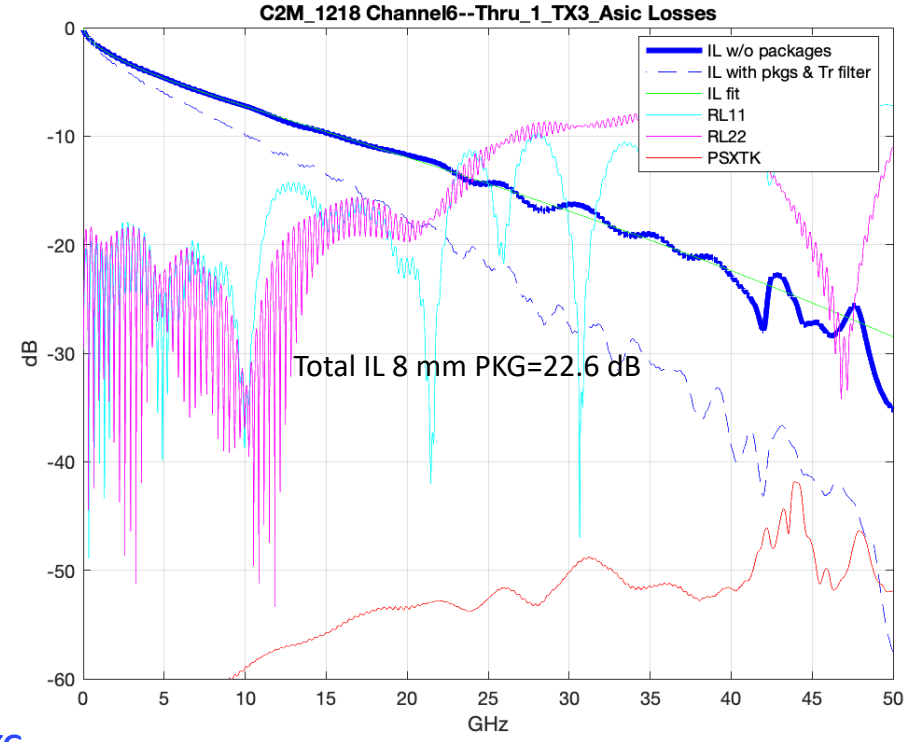
COM Analysis on Lim Channel6 - Module-ASIC

- **Lim channel 6 QSFP-dd Legacy contacts includes ASIC foot print at TP5 and slicer input**

TP5, FOM_ILD=0.17, ICN=1.56 mV, ICR=36.8 dB, ERL11=10.7, ERL22=14.8
5T FFE(4 post): COM=5.6 (5.1) dB, EH=18.9 (17.5) mV, VEC=6.5 (7.1) dB
TX FFE [0.02, -0.14, 0.78, -0.06] Optimum
5T FFE(4 post)+1T DFE: COM=5.9 (5.6) dB, EH=29.2 (25.4) mV, VEC=6.2 (6.5) dB
TX FFE[0.04, -0.18, 0.78,0] Optimum
4TDFE: COM=5.8 (5.4) dB, EH=24.1 (24.7) mV, VEC=6.2 (6.7) dB
TX FFE[0.04, -0.18, 0.78,0] Optimum



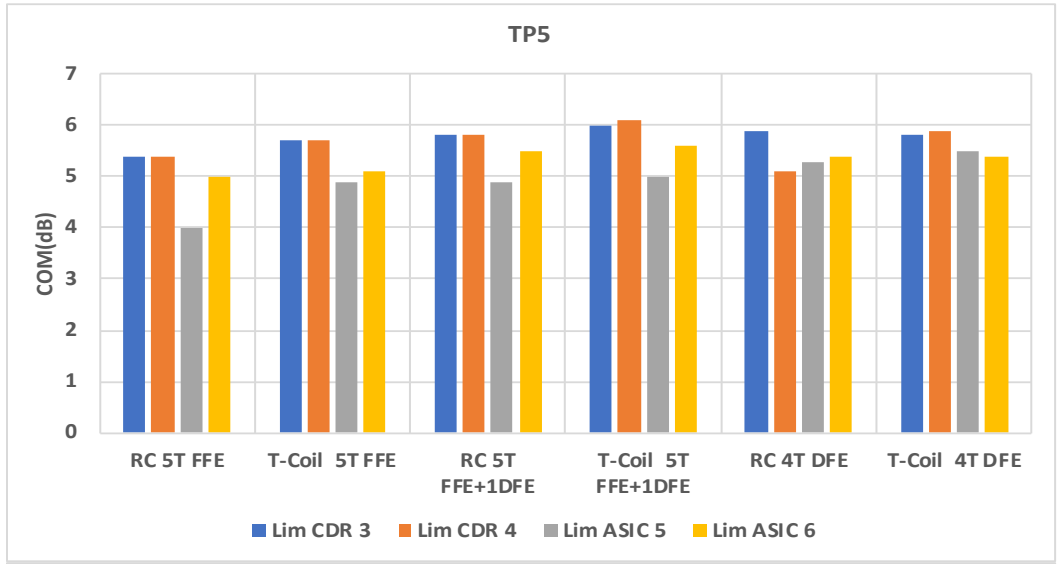
Slicer Input, FOM_ILD=0.17, ICN=1.56 mV, ICR=36.8 dB, ERL11=10.8, ERL22=15.2
5T FFE(4 post): COM=3.6 (3.8) dB, EH=9.4 (8.6) mV, VEC=9.5 (9.0) dB
TX FFE [0.02, -0.14, 0.74, -0.1 Optimum
5T FFE(4 post)+1T DFE: COM=4.7 (4.9) dB, EH=18.8 (15.3) mV, VEC=7.6 (7.4) dB
TX FFE [0.04, -0.2, 0.76, 0] Optimum
4T DFE: COM=4.5 (4.6) dB, EH=12.7 (14.7) mV, VEC=7.7(7.9) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum

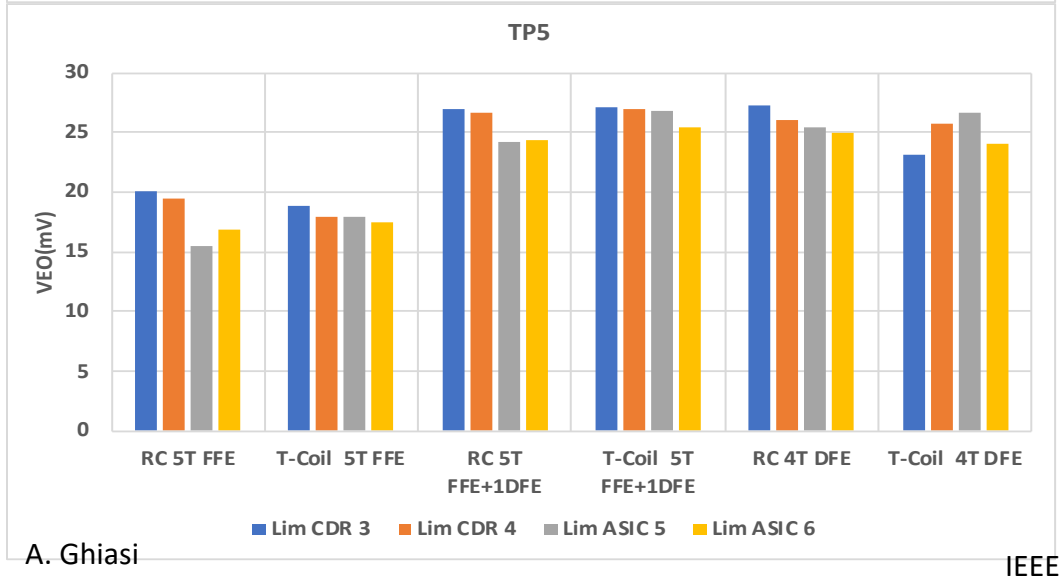


Result in x(y) are for 2(8) mm PKG.

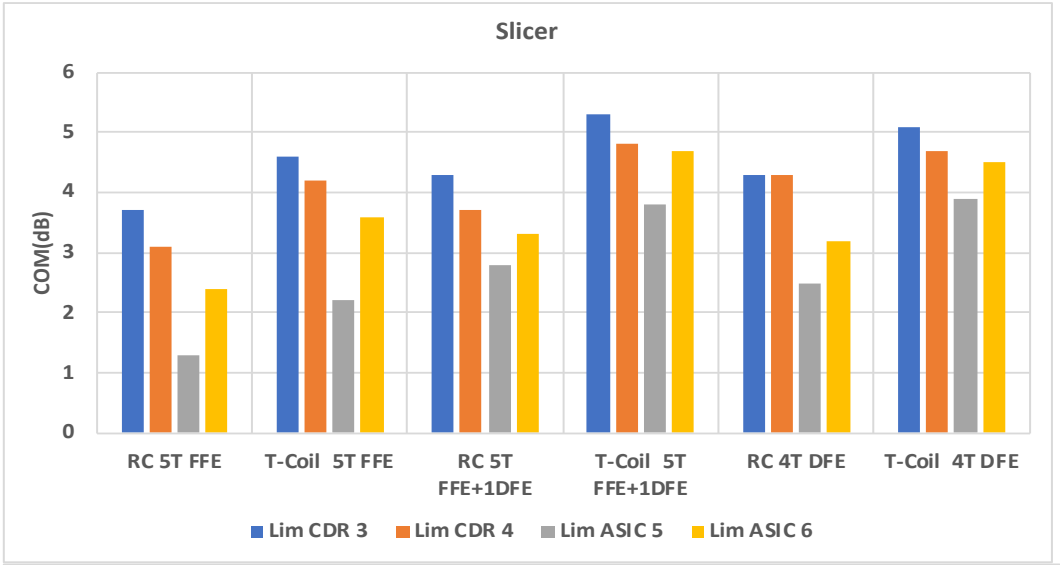
Comparisons of RC vs T-Coil Model for Lim Channels TP5 Direction

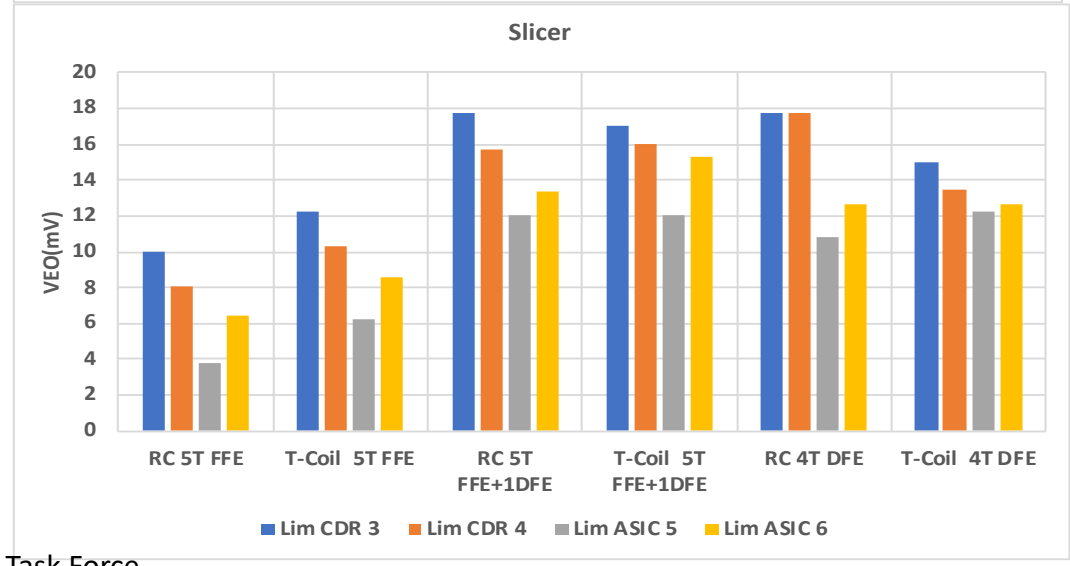
TP5 Results with RC and T-Coil
(Ls=100 pH, Cb=30 ff, Cd=120 ff)





Slicer Results with RC TX and RC/T-Coil RX
(Ls=100 pH, Cb=30 ff, Cd=120 ff)

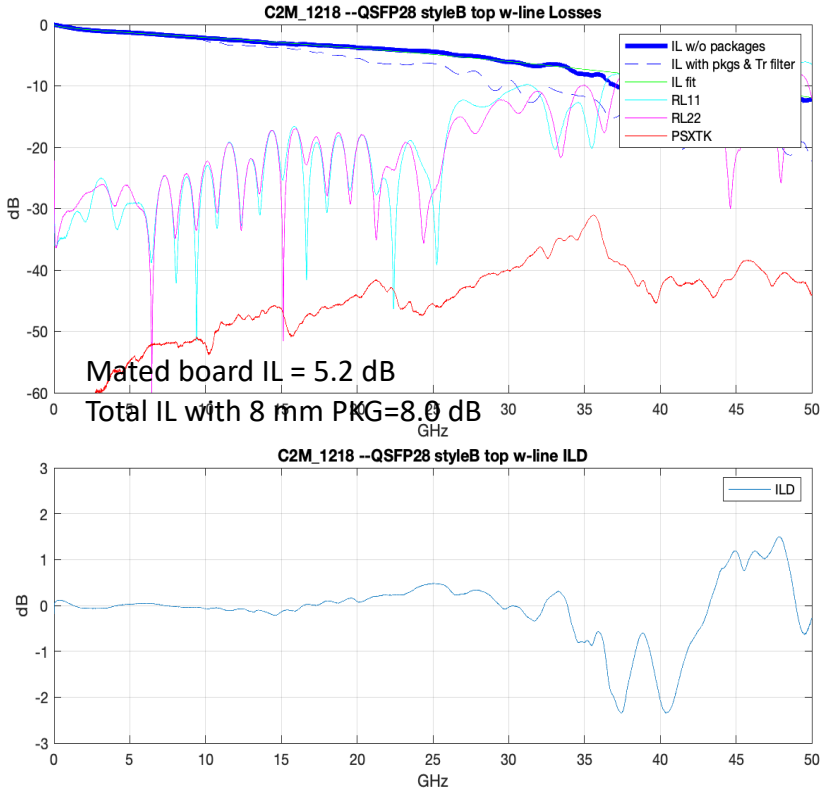




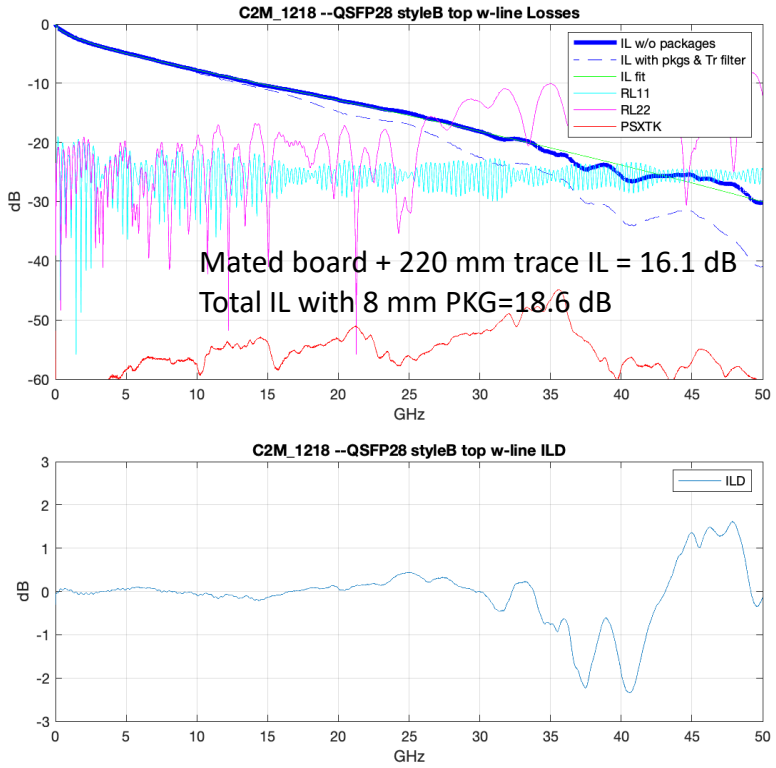
TP4/TP5 Analysis with Yamaichi QSFP-56 Mated Boards

- **COM improves by 1+ dB at TP5 compare to TP4!**
  - TP4 and TP5 results are with RC TX model.

TP4, ILD=0.18, ICN=5.2 mV, ICR=39.5 dB, ERL11=14.6, ERL22=10.7
5T FFE(4 post): COM=5.7 (4.9) dB, EH=51.5 (46.4) mV, VEC=6.3 (7.3) dB
5T FFE+1T DFE: COM=5.1 (4.5) dB, EH=54.2 (45.8) mV, VEC=7.2 (7.8) dB
4T DFE: COM=5.1 (4.5) dB, EH=53.1 (45.6) mV, VEC=7.1 (7.9) dB



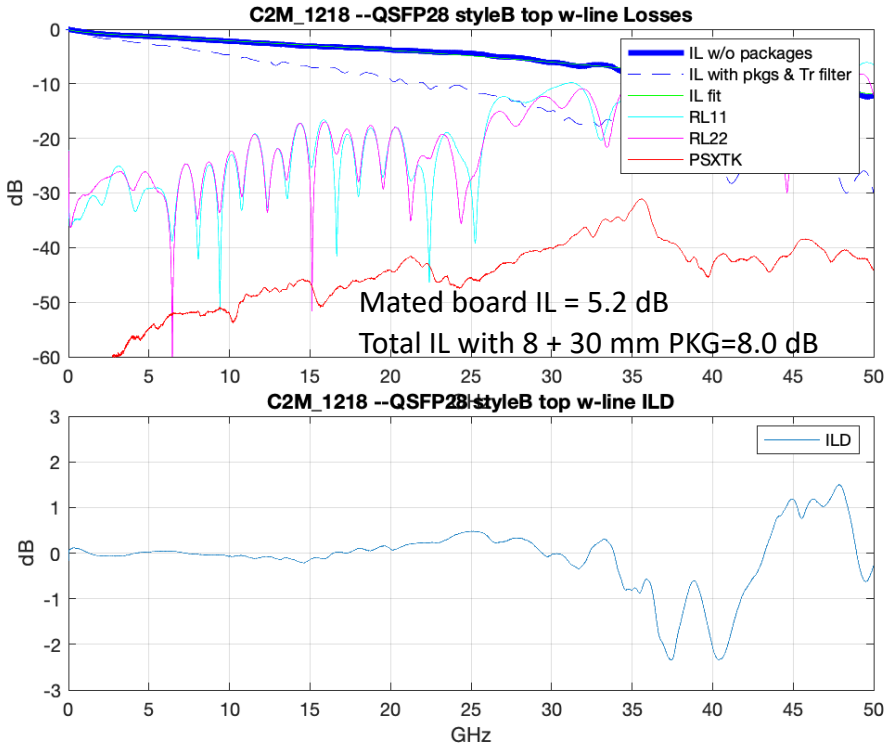
TP5, ILD=0.17, ICN=1.6 mV, ICR=39.1 dB, ERL11=14.6, ERL22=10.7
5T FFE(4 post): COM=6.6 (6.3) dB, EH=19.3 (20.9) mV, VEC=5.5 (5.8) dB
5T FFE+ 1T DFE : COM=6.7 (6.8) dB, EH=25.1 (26.0) mV, VEC=5.4 (5.3) dB
4T DFE: COM=6.7 (6.6) dB, EH=26.5 (24.0) mV, VEC=5.4 (5.5) dB



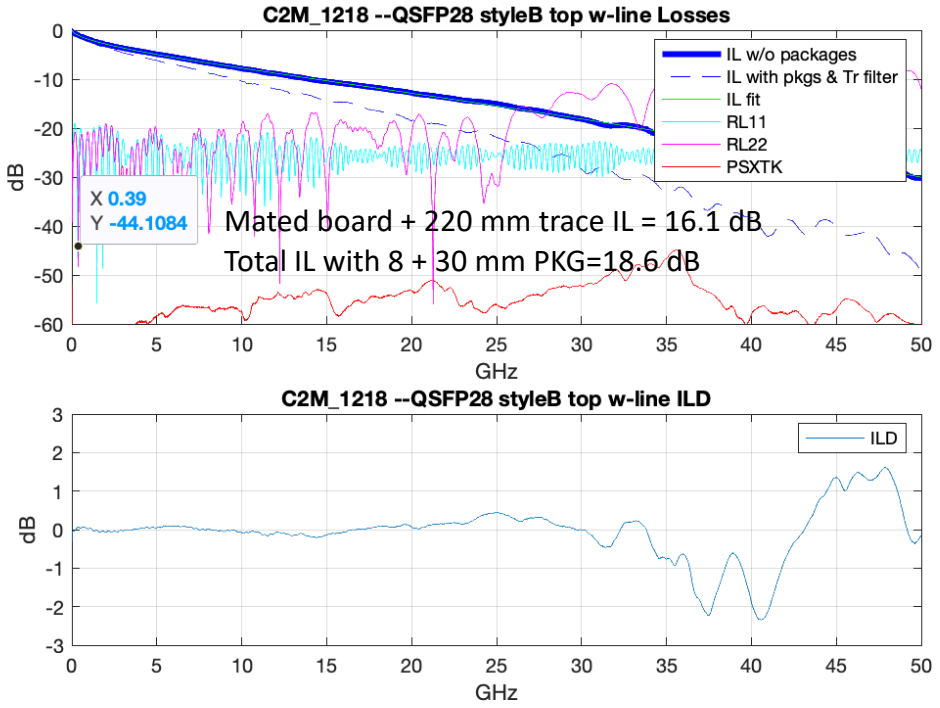
Min/Max Channel Loss at Slicer with Yamaichi QSFP-56 Mated Boards

- **COM at slicer for min loss 5.2 dB channel and max loss 16 dB channel are about the same!**
  - With RC TX and T-Coil RX model.

Min Loss, ILD=0.18, ICN=5.2 mV, ICR=39.5 dB, ERL11=14.6, ERL22=10.9
5T FFE(4 post): COM=5.1 (4.8) dB, EH=41.3 (31.3) mV, VEC=7.1 (7.5) dB
5T FFE+1T DFE: COM=4.9 (4.8) dB, EH=41.4 (33.4) mV, VEC=7.4 (7.4) dB
4T DFE: COM=5.1 (4.5) dB, EH=53.1 (45.6) mV, VEC=7.1 (7.9) dB



Max Loss, ILD=0.17, ICN=1.6 mV, ICR=39.1 dB, ERL11=14.6, ERL22=10.7
5T FFE(4 post): COM=5.2 (4.5) dB, EH=12.7 (11.1) mV, VEC=6.9 (7.9) dB
5T FFE+ 1T DFE : COM=5.8 (5.6) dB, EH=19.1 (15.9) mV, VEC=6.3 (6.4) dB
4T DFE: COM=5.6 (5.4) dB, EH=15.7 (13) mV, VEC=6.5 (6.7) dB



Why FFE Is Preferred Reference Equalizer

- **All 802.3bs and 802.3cd PAM4 PMDs require 5 tap T spaced FFE with up to 2 pre-cursor taps**
  - 4 tap DFE flatly fails as an optics receiver
  - Every optics CDR already has ≥ 5 tap FFE and possibly one tap DFE
  - Clause 121.8.5.4 defines TDECQ reference equalizer as a 5 tap, T spaced, feed-forward equalizer (FFE)
- **It has been raised that zero forcing DFE in COM is easier to adapt**
  - COM is not a normative requirement of C2M
  - The normative C2M test will be performed on scopes at TP1a and TP4/TP5 measuring EW and EH
  - Keysight and Tek both have developed TDECQ scope algorithm already based on 5 tap FFE
  - Reusing 5 tap FFE for electrical test is trivial
- **Why not duplicate the optics CDR core with 5 tap FFE (+ 1T DFE?) on the electrical side?**
- **Real use for 100G/lane AUI will be 800G modules where PD is critical 5 Tap FFE+1DFE offer more flexible architecture where 1T DFE is not turned on many channels**
  - Over time may find 1T DFE is not necessary
- **5T FFE or 5T FFE+1T DFE with bmax≤0.5 removes concern with burst error on segmented link**
- **TP1a and TP4/TP5 are observation point to estimate signal quality at slicer**
  - 5T FFE+1T DFE or 4T DFE EQ at TP4/TP5 may allow modules that should fail to pass such that host EQ based on 5T FFE+1T DFE or 4T DFE will fail
  - FFE inherently preserves the analog signal and will provide better direct correlation than a DFE clipped signal!

Summary

- **Summary of Lim 3/19 channels simulations at TP1a/TP5 and at slicer input**
  - Updated results with ASIC T-Coil and 5T FFE improves COM by 1-2 dB and in some cases VEO is doubled
  - Limited COM analysis at TP5 also shows general improvement if we use the T-Coil model for the CDR
  - Given the improved COM results with 5T FFE there is less reason to go with 5T FFE+1T DFE or 4T DFE
- **Reference EQ for TP4/TP5 should not be based on 5T FFE+1T DFE or 4T DFE otherwise channel that should fail may pass**
  - 5T FFE is best choice for TP1a and TP4/TP5 observation reference EQ
  - The actual equalizer likely will be something little more capable than just 5T FFE
- **C2M TP1, TP4, and TP5 recommended limits based on 5T FFE (4 post) scope reference equalizer**
  - TP1a EH=10 mV, VEC=9.5 dB, EW=TBD
  - TP4 EH=30 mV, VEC=9 dB, EW=TBD
  - TP5 EH=10 mV, VEC=9.5 dB, EW=TBD.