



# 100G C2M Channel Model Update (Module-to-Host)

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# Contributors

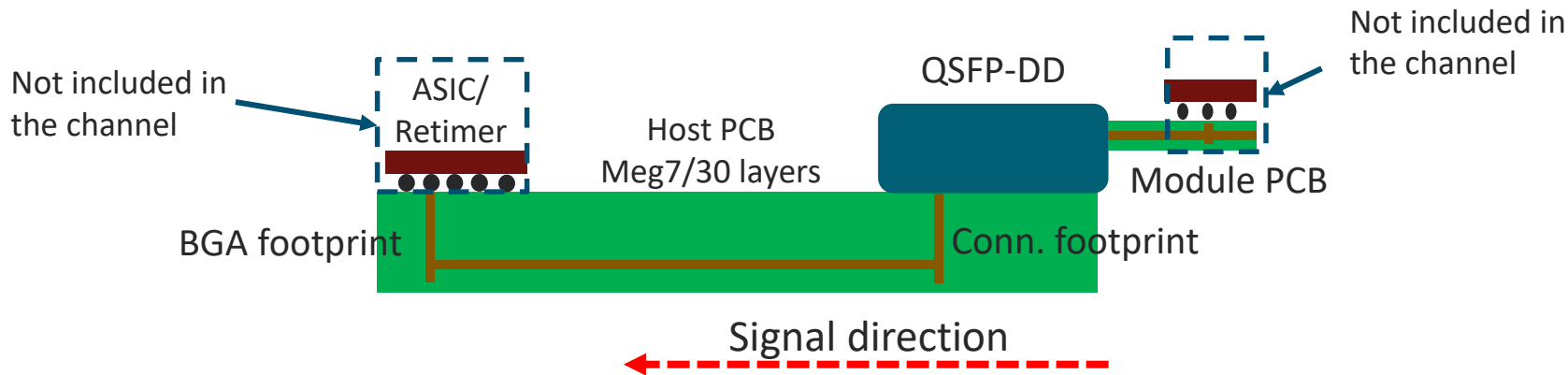
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- Alex Haser, Molex
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- Rockwell Hsu, Cisco
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# C2M Channel Model Update

- At March Vancouver meeting, lim\_3ck\_01a\_0319 analyzed 16 dB C2M Host to module channels at TP1a, using 112G QSFPDD SMT connector, 6 sets of channels are provided on March 3<sup>rd</sup>, 2019
- [http://www.ieee802.org/3/ck/public/tools/c2m/lim\\_3ck\\_01\\_0319\\_c2m.zip](http://www.ieee802.org/3/ck/public/tools/c2m/lim_3ck_01_0319_c2m.zip)
- This presentation provides Module-to-Host channels at TP4 and TP5, with optimized BGA & connector footprint
- Use COM scripts 2.60, to be consistent with what was used in March's presentation

# Model Overview

- 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector and host PCB footprint are solved as one piece in HFSS
- PCB stackup is 30 layers, 150mil thick, with Meg7 material
- PCB via stub length is modelled as 10mil
- Diff pair trace width/spacing is 4.5mil/8.5mil, 2 different trace lengths are used (2" & 9")
- ASIC/Retimer footprint are simulated with actual BGA ball-out using the same PCB stackup
- Module CDR footprint is not included in the channel



# Module Package Assumptions

- $C_d = 0.85e-4$  nF;  $C_p = 0.87e-4$  nF
- Package trace length = 2mm & 8mm; Package PTH = 0
- Use Reference receivers B & C currently in C2M consideration (see sun\_3ck\_01\_0519)
  - Rx B: 5-tap FFE with 1-tap DFE (FFE4post with DFE b1max=0.5)
  - Rx C: 5-tap FFE
- See backup slides for COM settings

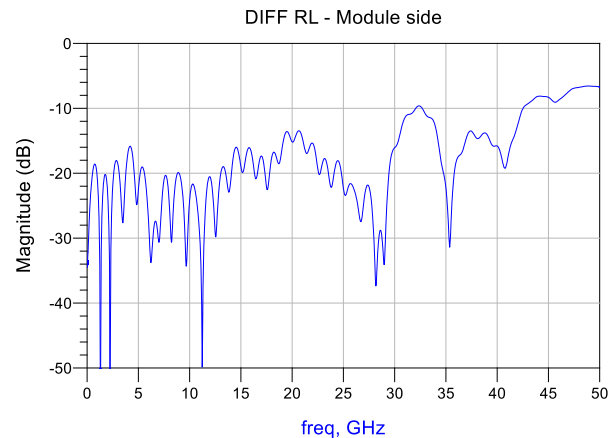
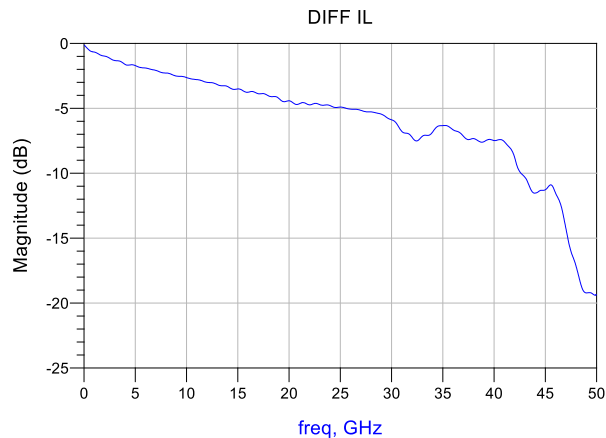
# Module-to-Host Channels

- Total 10 channels were built:
  - Channel 1a (TP4): Module PCB + QSFP-DD footprint & connector (new pair) + Host trace 2"; including 5 FEXT & 3 NEXT
  - Channel 1b (TP5): Module PCB + QSFP-DD footprint & connector (new pair) + Host trace 9" + Improved ASIC BGA footprint (long via) RX; including 5 FEXT & 3 NEXT
  - Channel 1c (TP5): Module PCB + QSFP-DD footprint & connector (new pair) + Host trace 2" + Improved ASIC BGA footprint (long via) RX; including 5 FEXT & 3 NEXT
  - Channel 1d (TP5): Module PCB + QSFP-DD footprint & connector (new pair) + Host trace 2" + Improved Retimer BGA footprint (short via) RX; including 2 FEXT & 2 NEXT
  - Channel 1e (TP5): Module PCB + QSFP-DD footprint & connector (new pair) + Host trace 2" + Improved Retimer BGA footprint (long via) RX; including 2 FEXT & 2 NEXT
  
  - Channel 2a (TP4): Module PCB + QSFP-DD footprint & connector (legacy pair) + Host trace 2"; including 5 FEXT & 3 NEXT
  - Channel 2b (TP5): Module PCB + QSFP-DD footprint & connector (legacy pair) + Host trace 9" + Improved ASIC BGA footprint (long via) RX; including 5 FEXT & 3 NEXT
  - Channel 2c (TP5): Module PCB + QSFP-DD footprint & connector (legacy pair) + Host trace 2" + Improved ASIC BGA footprint (long via) RX; including 5 FEXT & 3 NEXT
  - Channel 2d (TP5): Module PCB + QSFP-DD footprint & connector (legacy pair) + Host trace 2" + Improved Retimer BGA footprint (short via) RX; including 2 FEXT & 2 NEXT
  - Channel 2e (TP5): Module PCB + QSFP-DD footprint & connector (legacy pair) + Host trace 2" + Improved Retimer BGA footprint (long via) RX; including 2 FEXT & 2 NEXT

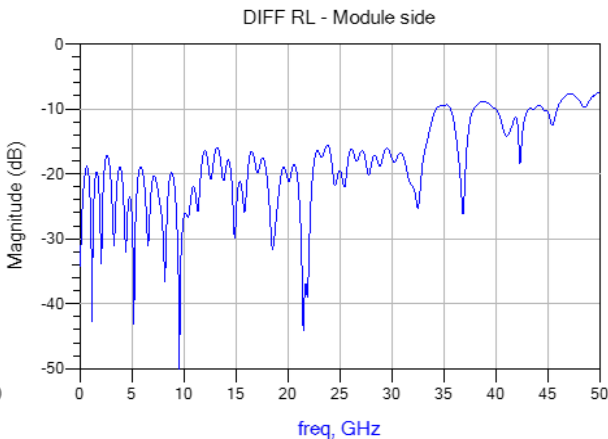
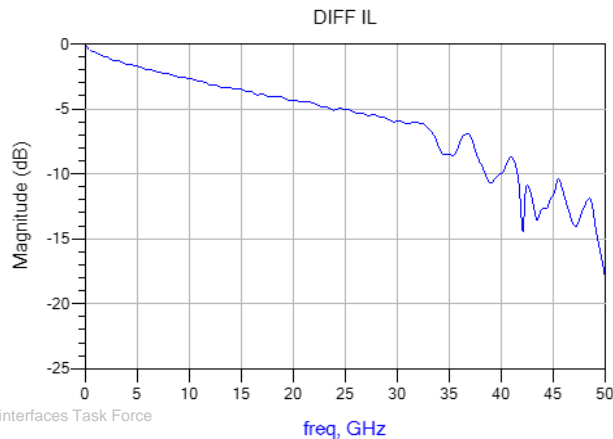
Channels s-param files have been contributed at [http://www.ieee802.org/3/ck/public/tools/c2m/lim\\_3ck\\_03\\_0719\\_m2c](http://www.ieee802.org/3/ck/public/tools/c2m/lim_3ck_03_0719_m2c)

# Channel 1a/2a: Insertion Loss, Return Loss

**Channel 1a, TP4  
(new pair)**

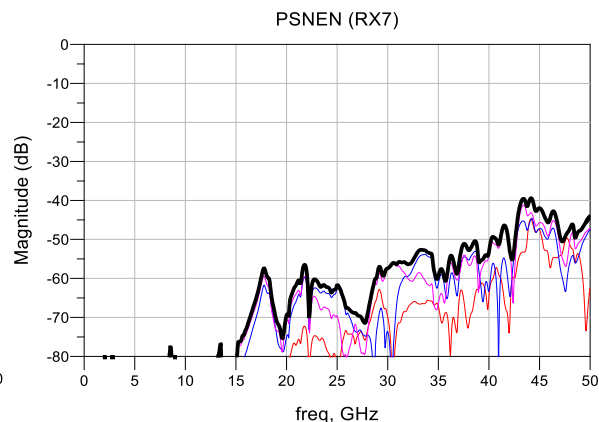
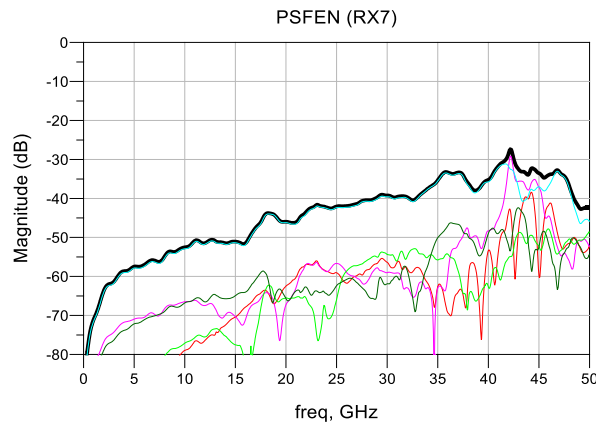


**Channel 2a, TP4  
(legacy pair)**

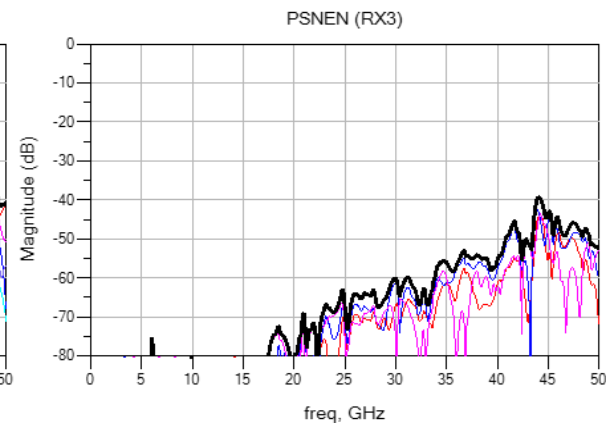
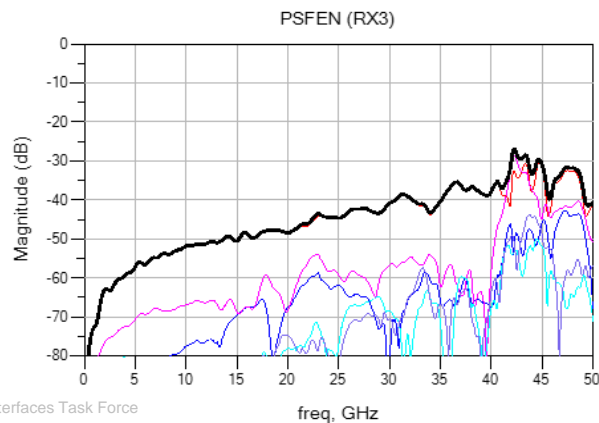


# Channel 1a/2a: Far-end and Near-end Crosstalk

Channel 1a, TP4  
(new pair)



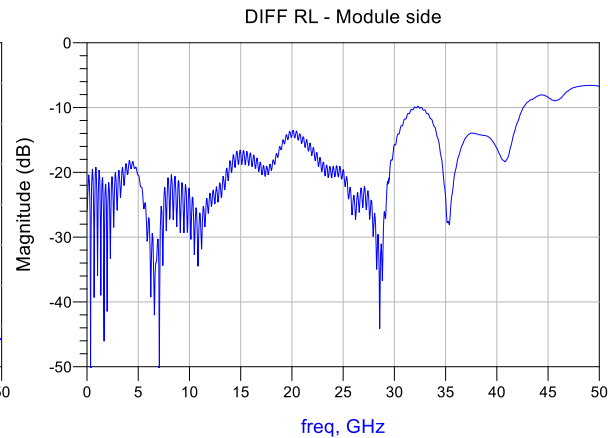
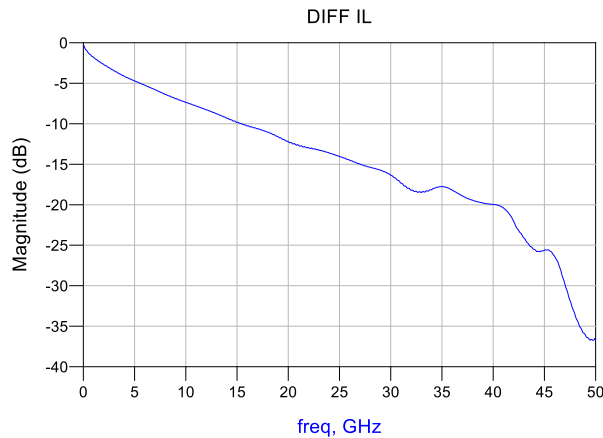
Channel 2a, TP4  
(legacy pair)



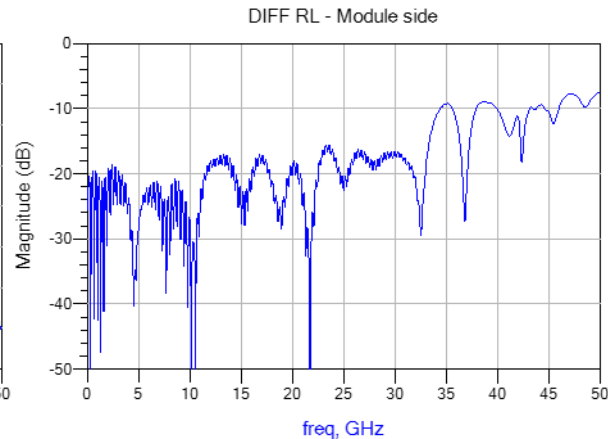
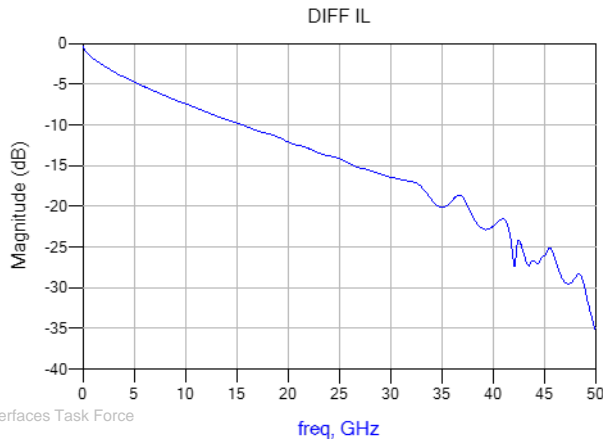


# Channel 1b/2b: Insertion Loss, Return Loss

**Channel 1b, TP5  
(new pair)**

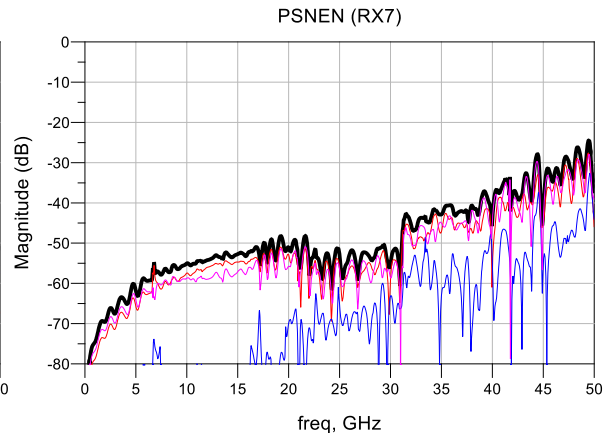
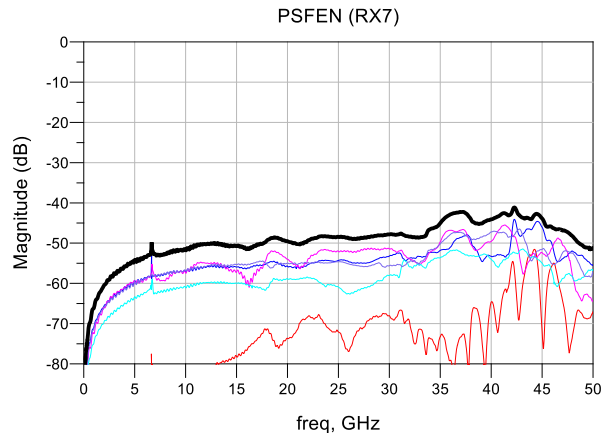


**Channel 2b, TP5  
(legacy pair)**

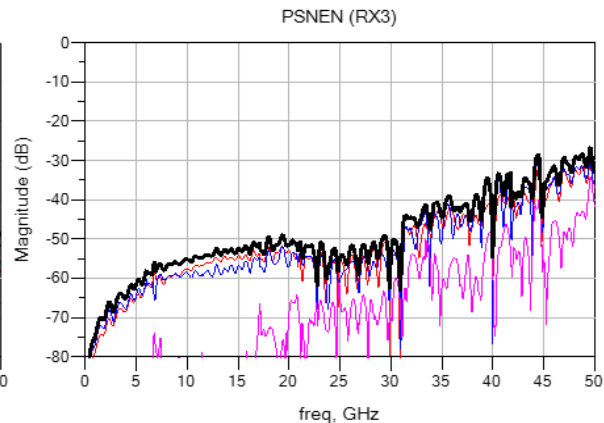
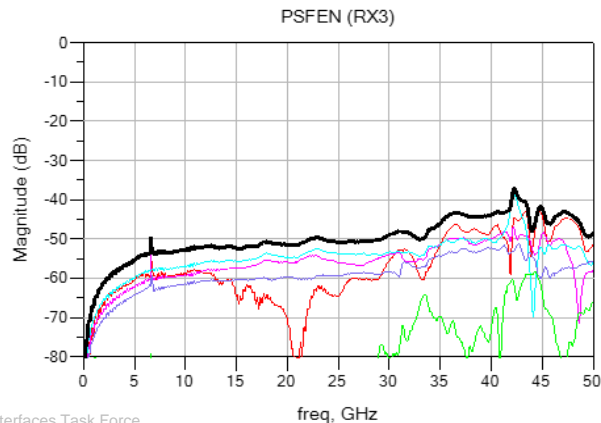


# Channel 1b/2b: Far-end and Near-end Crosstalk

Channel 1b, TP5  
(new pair)

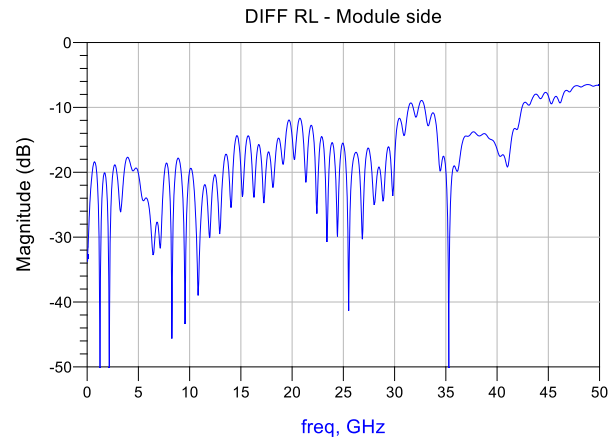
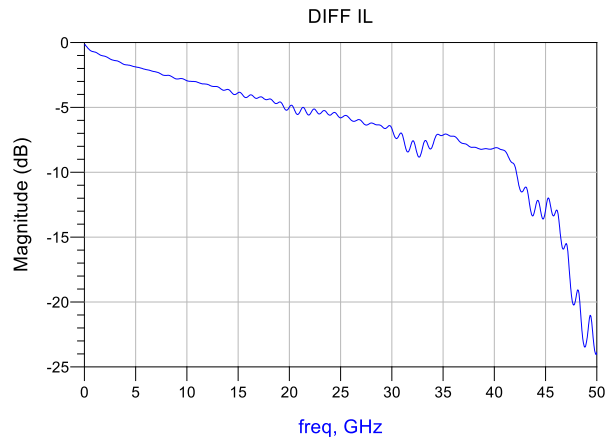


Channel 2b, TP5  
(legacy pair)

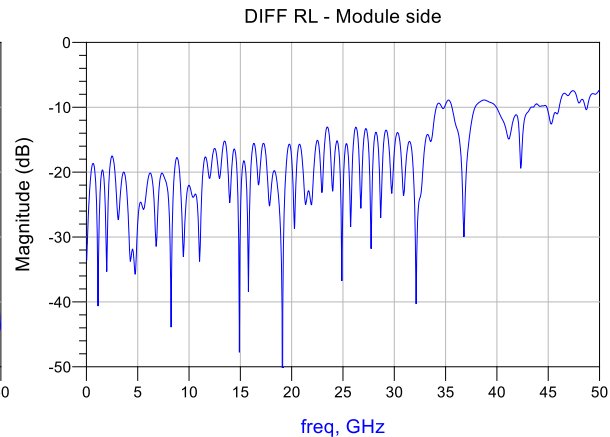
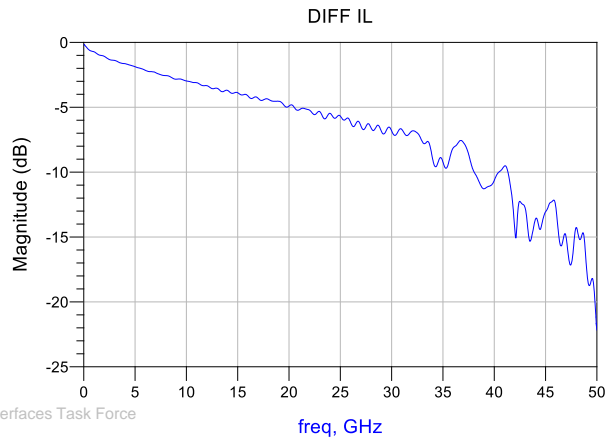


# Channel 1c/2c: Insertion Loss, Return Loss

**Channel 1c, TP5  
(new pair)**

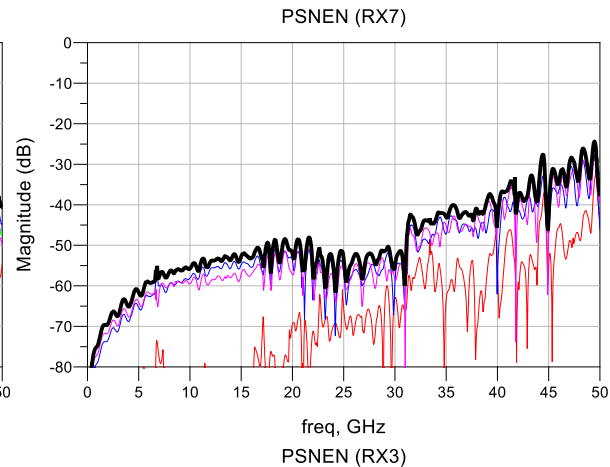
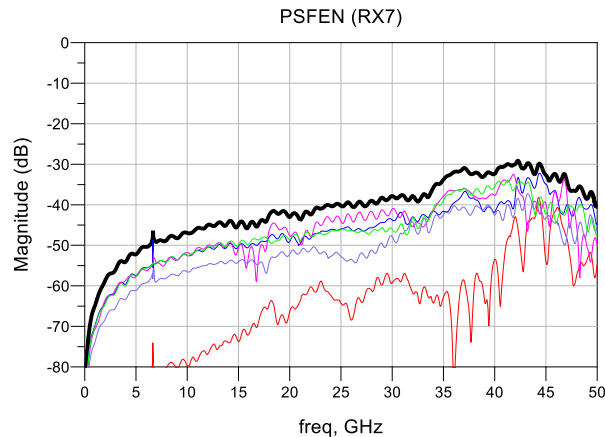


**Channel 2c, TP5  
(legacy pair)**

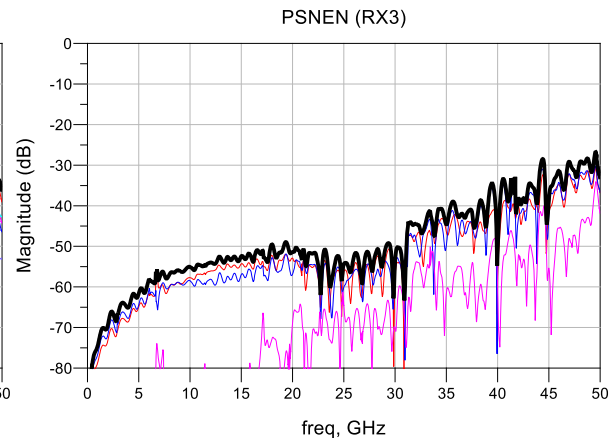
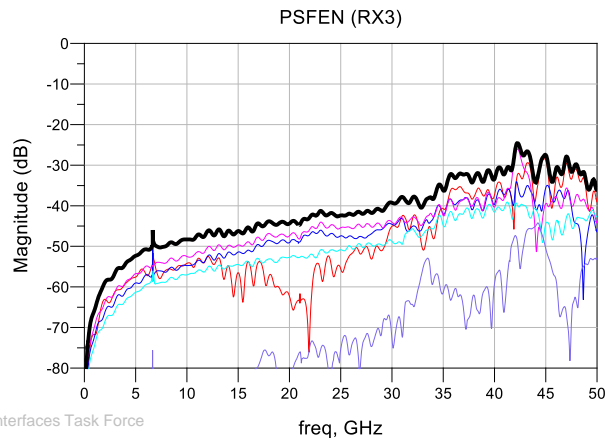


# Channel 1c/2c: Far-end and Near-end Crosstalk

Channel 1c, TP5  
(new pair)

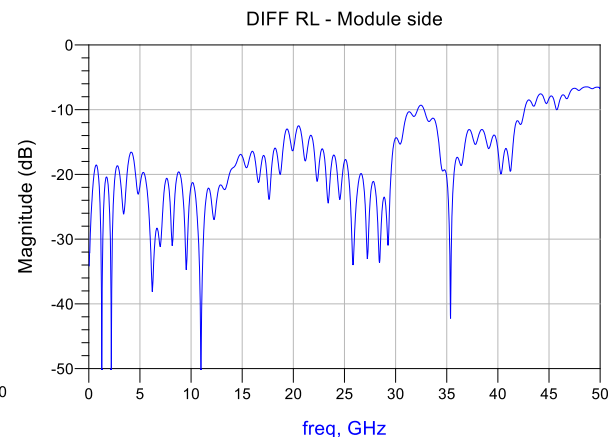
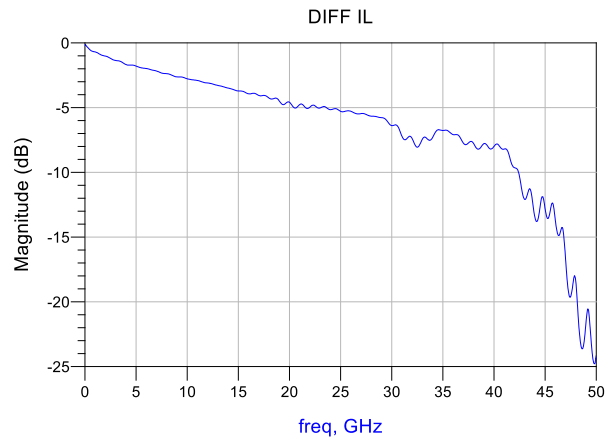


Channel 2c, TP5  
(legacy pair)

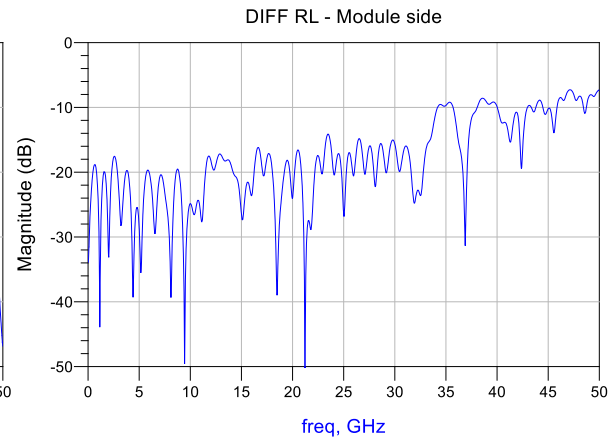
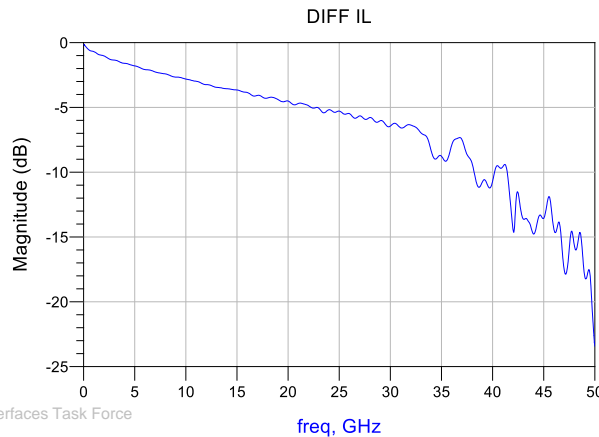


# Channel 1d/2d: Insertion Loss, Return Loss

**Channel 1d, TP5  
(new pair)**

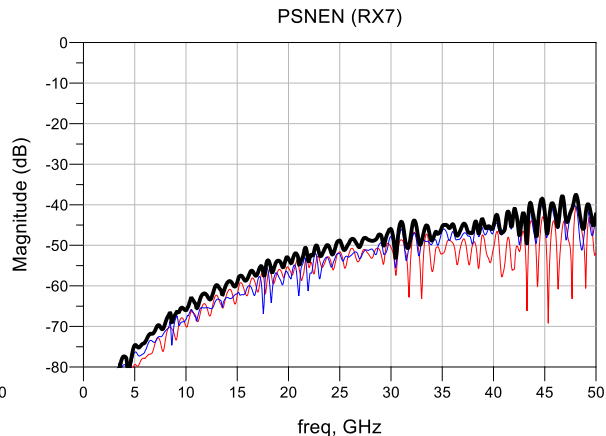
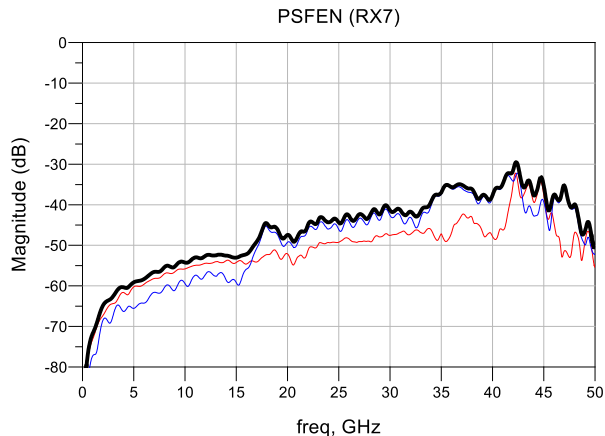


**Channel 2d, TP5  
(legacy pair)**

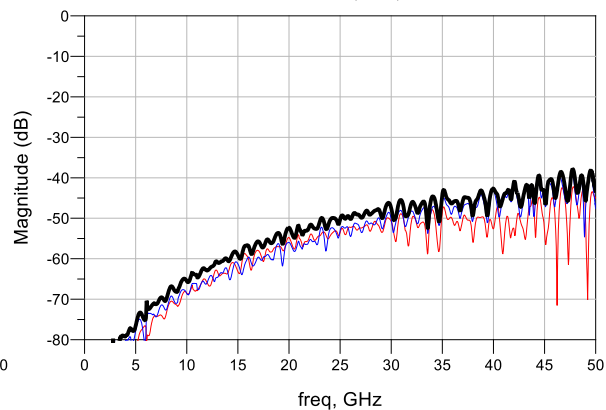
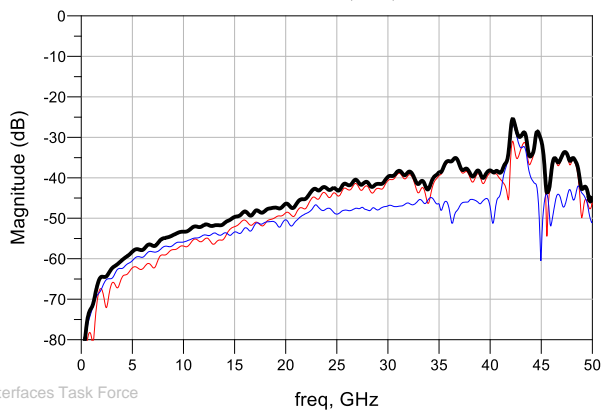


# Channel 1d/2d: Far-end and Near-end Crosstalk

Channel 1d, TP5  
(new pair)

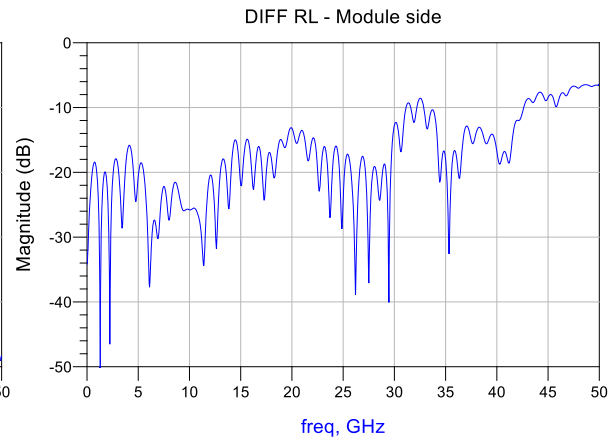
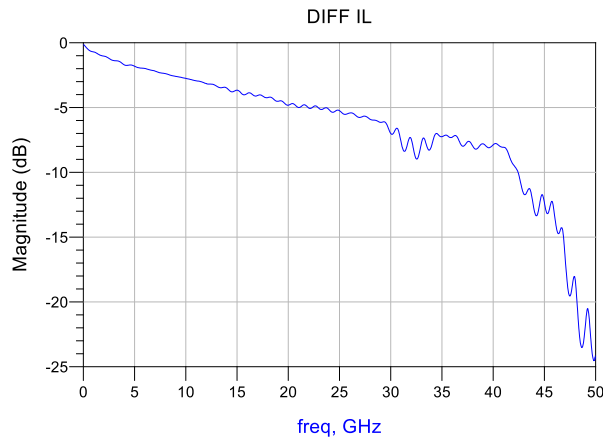


Channel 2d, TP5  
(legacy pair)

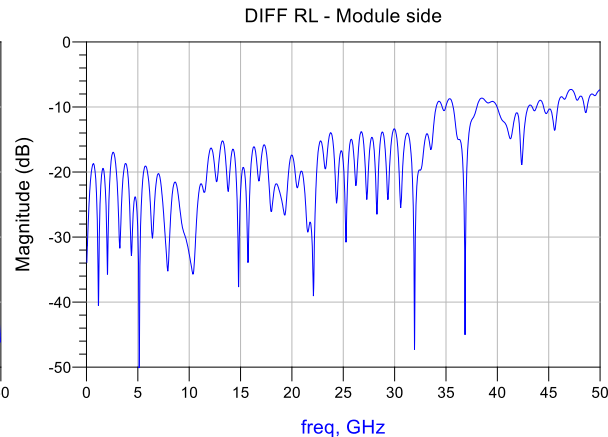
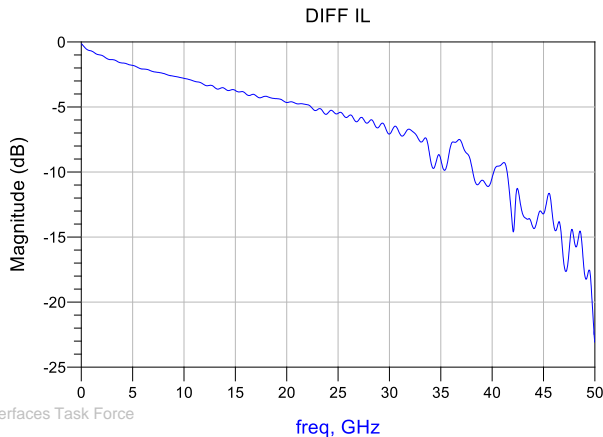


# Channel 1e/2e: Insertion Loss, Return Loss

**Channel 1e, TP5  
(new pair)**

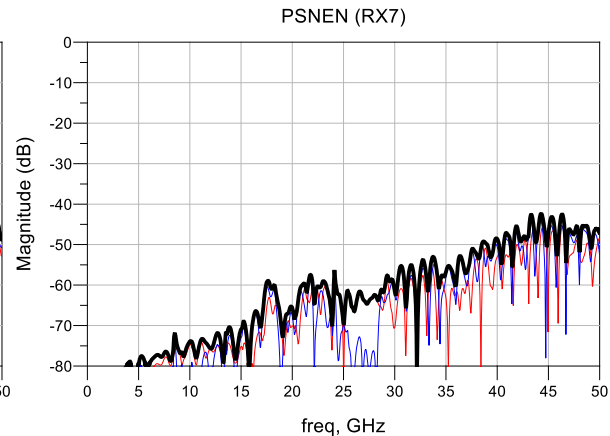
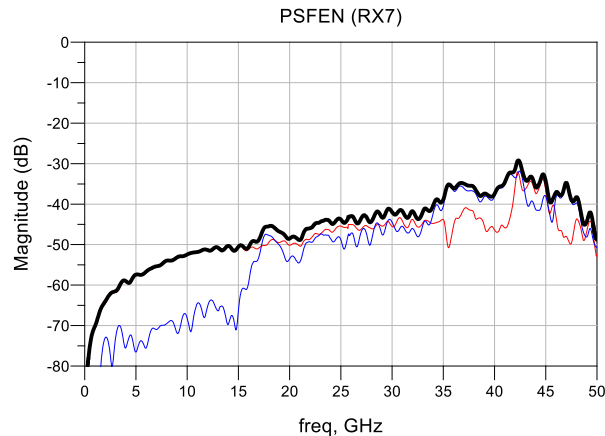


**Channel 2e, TP5  
(legacy pair)**

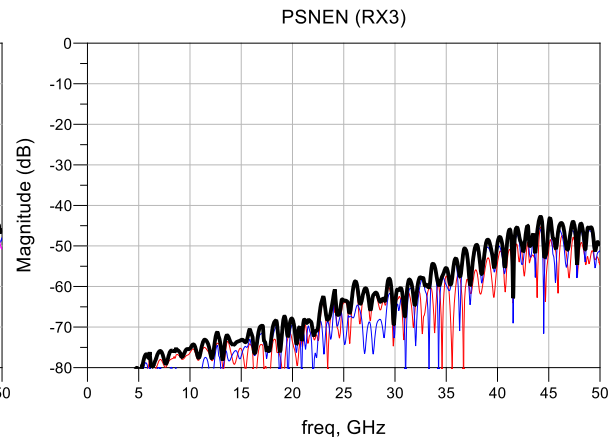
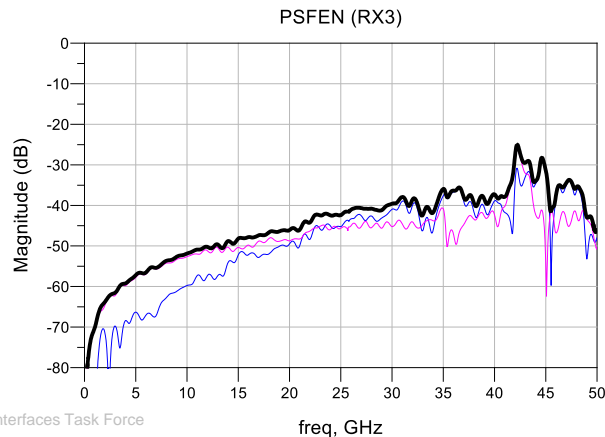


# Channel 1e/2e: Far-end and Near-end Crosstalk

Channel 1e, TP5  
(new pair)



Channel 2e, TP5  
(legacy pair)





# TP4/TP5 COM Results – 2 Ref. Rx (B & C)

DUT	COM Case1 (2mm) Rx B/Rx C (dB)	COM Case2 (8mm) Rx B/Rx C (dB)	ERL11 (dB)	ERL22 (dB)	ICN (mV)	FOM <sub>ILD</sub> (dBrms)	IL@26G ball- to-ball (dB)
Channel 1a	6.36/6.79	5.45/5.47	11.49	9.30	2.21	0.18	5.07
Channel 1b	5.91/5.56	5.30/4.43	12.10	9.79	1.92	0.17	14.76
Channel 1c	5.42/5.88	4.26/4.51	11.28	7.40	3.25	0.20	6.00
Channel 1d	6.19/6.60	5.18/5.25	11.54	8.67	2.12	0.19	5.47
Channel 1e	6.03/6.55	5.00/5.13	11.60	8.35	1.81	0.20	5.60
Channel 2a	6.40/6.76	6.17/6.34	12.54	9.77	1.83	0.17	5.34
Channel 2b	6.16/5.90	5.64/5.17	13.06	9.80	1.85	0.16	15.04
Channel 2c	6.10/6.39	5.48/5.65	12.10	7.88	2.99	0.18	6.18
Channel 2d	6.38/6.73	6.00/6.23	12.32	9.06	2.22	0.20	5.83
Channel 2e	6.45/6.79	5.72/5.90	12.35	8.83	2.08	0.17	5.97

Rx B = Ref. Rx with 5FFE + 1DFE; Rx C = Ref. Rx with 5FFE only, as listed in sun\_3ck\_01\_0519

# Summary

- C2M TP4 and TP5 channels are built with 112G QSFP-DD connector incl. realistic connector footprint; TP5 channels also include optimized host chip BGA footprint
- Both TP4 and TP5 channels can pass COM with margin using either ref. receiver B (5 tap FFE + 1 DFE tap) or ref. receiver C (5 tap FFE)
  - Ref. receiver C shows better COM values on all the short channels built with 2" trace
- Although TP4 channel 1a/2a has much less IL (~5dB) vs. TP5 channel 1b/2b (~15dB), COM is only ~0.3dB higher
  - TP4 and TP5 channels have similar ICN values (TP4 channel 1a/2a has higher FEXT, TP5 channel 1b/2b has higher NEXT)
- Channel 1c/2c has worst COM among the 10 channels due to more worse ILD & ICN with shorter trace and long via at the receiver end

*Backup Slides*

# Ref Receiver B

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.85e-4 0]	nF	[TX RX]
z_p select	[ 1 2]		[test cases to run]
z_p (TX)	[2 8 ; 0 0]	mm	[test cases]
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]
z_p (FEXT)	[2 8 ; 0 0]	mm	[test cases]
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[ 45 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.2:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(-3)	00:00.0		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:0.5:-4]	dB	[min:step:max]
f_z	18.5534	GHz	
f_p1	28.2	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-3:..0.5:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	4	UI	
Include PCB	0	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	1		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_(date)\	
SAVE_FIGURES	0	logical
Port Order	[ 1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.18	
fixture delay time	0	
TDR_W_TXPKG	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V <sup>2</sup> /GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	119	mm
z_bp (NEXT)	119	mm
z_bp (FEXT)	119	mm
z_bp (RX)	119	mm

# Ref Receiver C

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.85e-4 0]	nF	[TX RX]
z_p select	[ 1 2]		[test cases to run]
z_p (TX)	[2 8 ; 0 0]	mm	[test cases]
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]
z_p (FEXT)	[2 8 ; 0 0]	mm	[test cases]
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[ 45 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.2:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(-3)	00:00.0		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:0.5:-4]	dB	[min:step:max]
f_z	18.5534	GHz	
f_p1	28.2	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-3:..0.5:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	4	UI	
Include PCB	0	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	1		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_(date)\	
SAVE_FIGURES	0	logical
Port Order	[ 1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.18	
fixture delay time	0	
TDR_W_TXPKG	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V <sup>2</sup> /GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	119	mm
z_bp (NEXT)	119	mm
z_bp (FEXT)	119	mm
z_bp (RX)	119	mm