C2M Simulation Updates

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Introduction

- Studies such as sun_3ck_01_0519 and sun_3ck_01_0319 show reflection is the major impairment of 100G C2M interface. Recently higher-performance on-die termination has been suggested in kareti_3ck_01b_0519, and a termination model with inductor is proposed in healey_3ck_adhoc_01_061219.

- This contribution presents C2M simulation results with two higher-performance termination models that have been discussed for host side. With improved termination models, feasibility of lower-complexity reference equalizers are studied.

- Simulation is performed with COM tool v270.

Reference Receivers Review

Higher Performance

DFE-Based	**A** **4-tap DFE** **(tap 1-4, b1max=0.5)**	**D** **3-tap DFE** **(tap 2 - 4)**	**D2** **1-tap DFE** **(tap 2 only)**
FFE-Based	**B** **5 tap FFE + 1-tap DFE** **(post 1-4, b1max=0.5)**	**C** **5-tap FFE** **(post 1-4)**	**C2** **3-tap FFE** **(post 1-2)**

Less Complexity

- Receivers in the same column have similar performance. [sun_3ck_01_0519]

TP1a Results

Simulation Settings

- Simulations are set to study host on-die termination difference while keep all the other parameters the same.

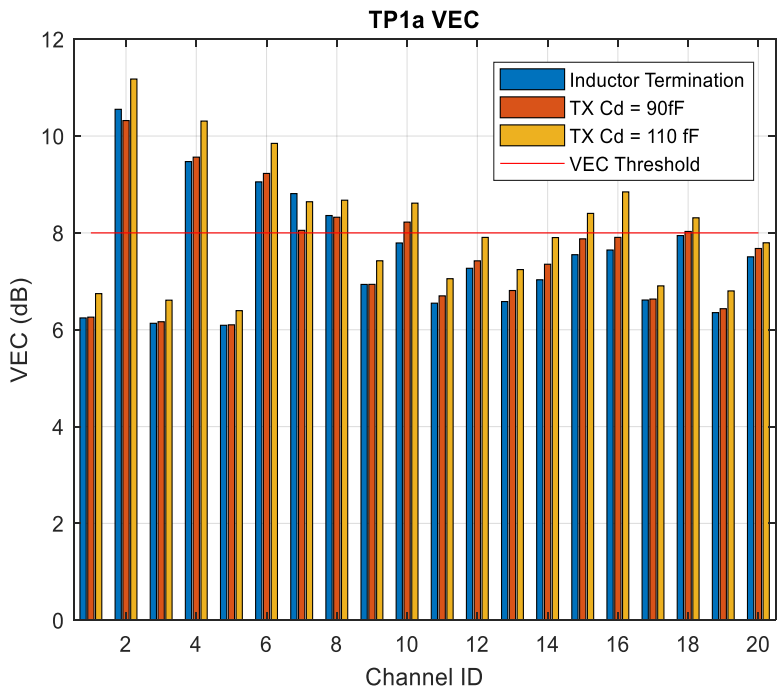
Termination Scheme for host	healey_3ck_adhoc_01_061219 (with inductor)	Cd 90 fF	Cd 110 fF
Ls	120 pH	0 pH	0 pH
Cb	30 fF	0 fF	0 fF
Cd	120 fF	90 fF	110 fF
Cp	87 fF	87 fF	87 fF
Package trace length	**Scan every 1 mm to find the worst VEC as worst package trace length is termination and channel dependent.**		

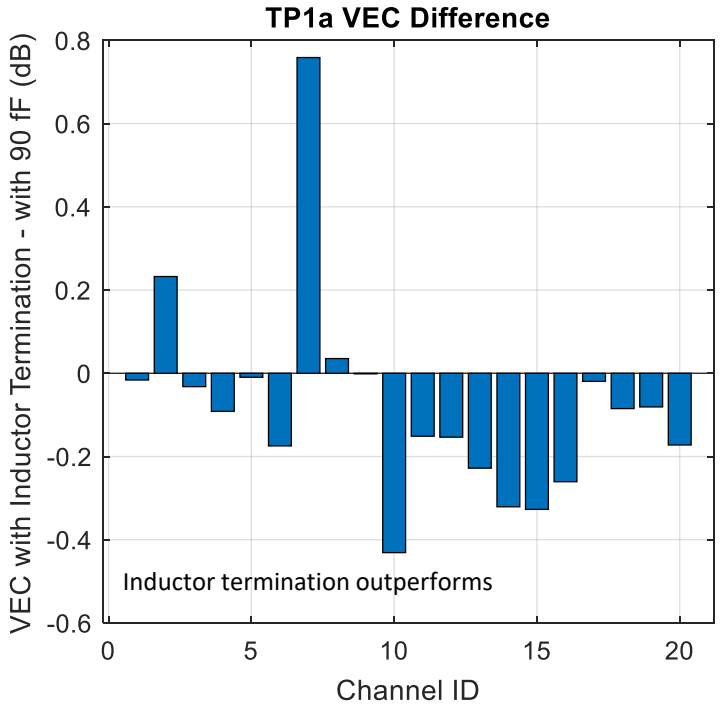
Channel Review with Inductor Termination

ID	Channel Description	Vote in May	IL (dB)	ERL11 (dB)	ERL22 (dB)	ICN (mV)	ILD (dB)	RX Required for TP1a		
								A	C	C2/D2
1	mellitz_3ck_01_0518_C2M\9dB	Pass	8.95	16.35	13.56	2.10	0.10	Pass	Pass	Pass
2	mellitz_3ck_01_0518_C2M\10dB	Fail	9.96	7.79	10.91	4.27	0.48	Fail	Fail	Fail
3	mellitz_3ck_01_0518_C2M\11dB	Pass	11.16	18.28	14.64	1.75	0.09	Pass	Pass	Pass
4	mellitz_3ck_01_0518_C2M\12dB	Fail	12.18	8.39	11.64	3.75	0.46	Fail	Fail	Fail
5	mellitz_3ck_01_0518_C2M\13dB	Pass	13.12	20.09	15.25	1.50	0.09	Pass	Pass	Pass
6	mellitz_3ck_01_0518_C2M\14dB	Fail	13.87	8.73	12.80	2.98	0.47	Fail	Fail	Fail
7	tracy_100GEL_02_0118\long_barrel_via\TX5	TBD	16.48	14.98	11.75	0.86	0.28	Fail	Fail	Fail
8	tracy_100GEL_02_0118\long_barrel_via\TX6	TBD	16.08	14.35	12.82	0.86	0.37	Fail	Fail	Pass
9	tracy_100GEL_06_0118\Microvia\RX6	Pass	14.59	15.71	12.74	0.79	0.21	Pass	Pass	Pass
10	tracy_100GEL_06_0118\Microvia\RX5	TBD	14.57	16.20	13.76	0.89	0.23	Pass	Pass	Pass
11	lim_3ck_01_0319_QDD_new_pad\ch1	Pass	14.40	15.83	21.66	0.73	0.20	Pass	Pass	Pass
12	lim_3ck_01_0319_QDD_new_pad\ch2	Pass	14.60	14.51	21.02	0.76	0.19	Pass	Pass	Pass
13	lim_3ck_01_0319_QDD_legacy_pad\ch3	Pass	14.69	16.04	16.42	0.72	0.20	Pass	Pass	Pass
14	llim_3ck_01_0319_QDD_legacy_pad\ch4	Pass	14.84	14.77	16.11	0.81	0.18	Pass	Pass	Pass
15	llim_3ck_01_0319_QDD_new_pad\ch5	TBD	14.77	14.70	21.42	1.34	0.16	Pass	Fail	Pass
16	llim_3ck_01_0319_QDD_legacy_pad\ch6	Pass	15.02	15.01	16.30	1.47	0.17	Pass	Pass	Pass
17	ito_3ck_01\QSFP \bottom normal\	Pass	15.10	12.79	10.92	1.14	0.18	Pass	Pass	Pass
18	ito_3ck_01\QSFP \bottom worst\	TBD	15.58	12.49	10.48	1.09	0.32	Pass	Pass	Pass
19	ito_3ck_01\QSFP \top normal\	Pass	14.53	12.76	11.03	1.19	0.18	Pass	Pass	Pass
20	ito_3ck_01\QSFP \top worst\	TBD	14.49	12.43	10.52	1.14	0.31	Pass	Pass	Pass

- Voting results can be found in lusted_3ck_02_0519.
- Parameters highlighted in red are worse than 10.5dB ERL, 2.5mV ICN, or 0.35dB ILD.
- ERL is reported with Nbx=4. ERL11 is for channel only. ERL22 is at TP1a including TX package.
- For receiver pass/fail results, worst package traces are considered.

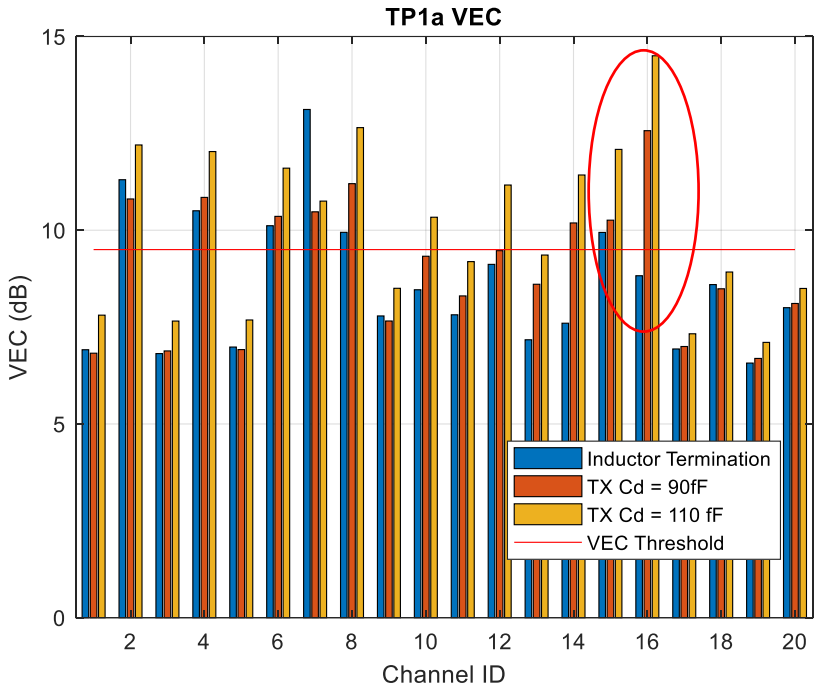
TP1a VEC with RX A

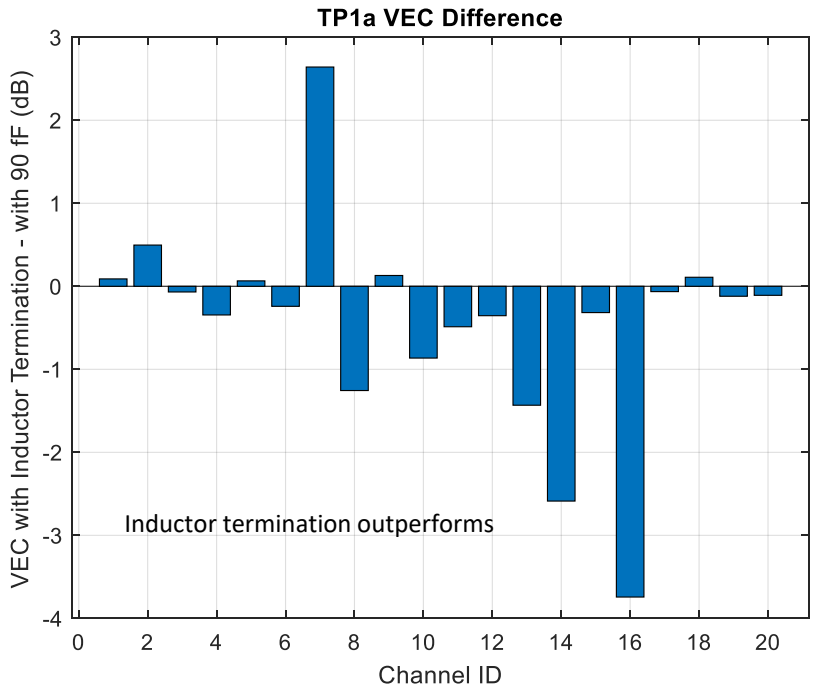




- With Reference receiver A (4-tap DFE, b1max=0.5)
- Termination with inductors outperforms Cd 90fF for most of the channels by up to 0.43dB.
  - Channel 7 is an exception.
- Receiver A is relatively insensitive to termination difference.
- If VEC threshold is set to 8dB with inductor termination, channels 2, 4, 6, 7, 8 fail.

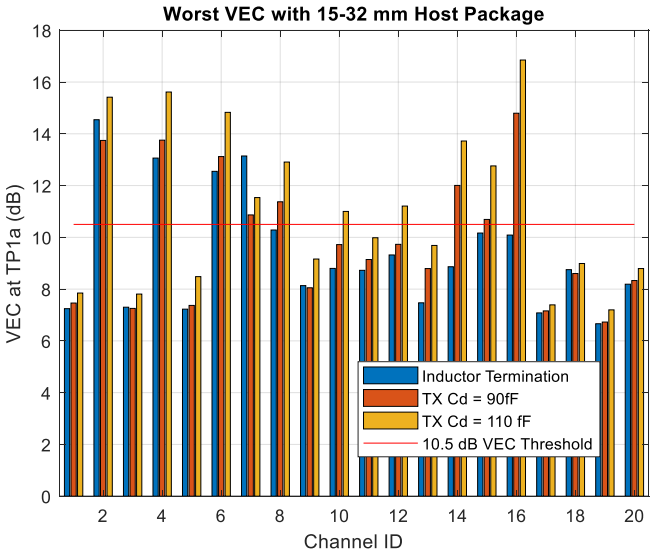
TP1a VEC with RX C

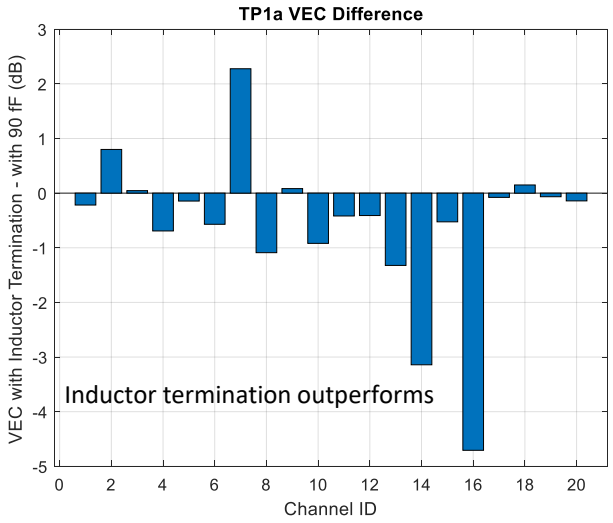




- With Reference receiver C – 4 post-tap FFE
- Inductor termination outperforms Cd=90 fF for most channels by up to 3.7dB.
- With receiver C, channels 2, 4, 6 and channels 8, 15 VEC are close to each other.
  - If VEC threshold is set to 9.5 dB with inductor termination, channels 2, 4, 6, 7, 8, and 15 will not be supported. 10dB VEC threshold has a risk to pass tough channels with bad whole-link COM.
- Channel 16 is voted to pass in May. It cannot pass TP1a with receiver C unless with inductor termination model.

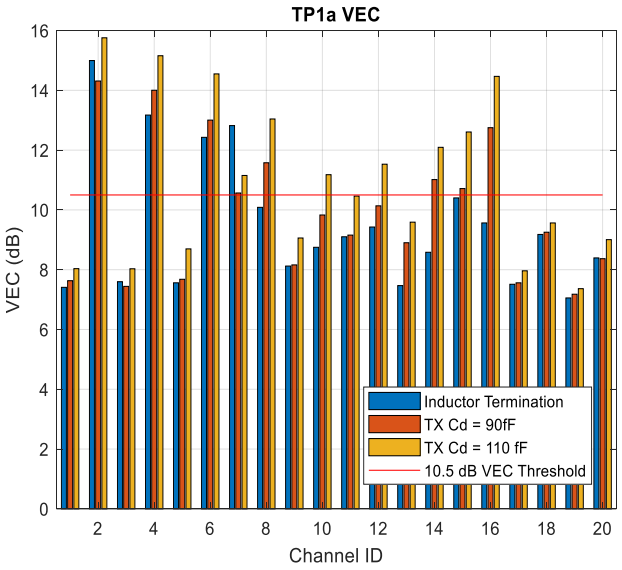
TP1a VEC with RX C2

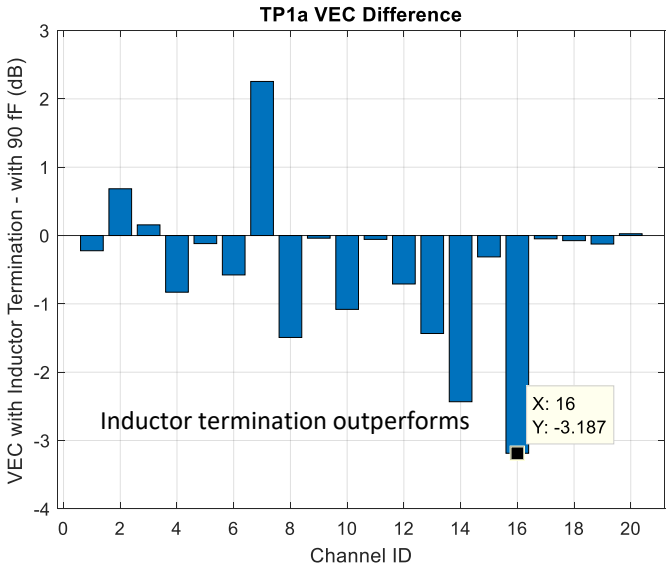




- With Reference receiver C2 (2 post-tap FFE).
- Inductor termination outperforms Cd=90 fF for most channels by up to 4.7dB.
- With inductor termination, VEC threshold can be set to ~10.5 dB to exclude channels 2, 4, 6, 7.

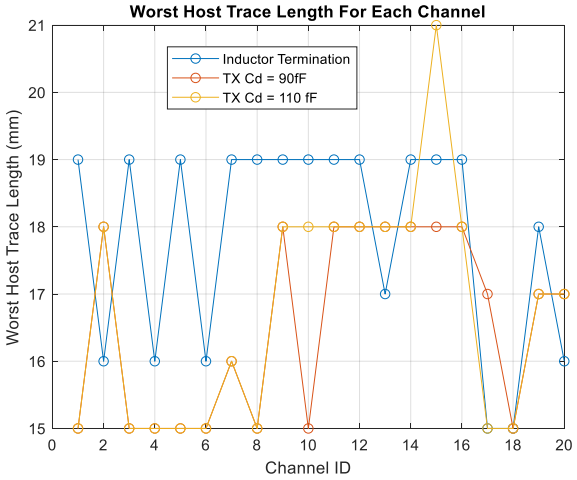
TP1a VEC with RX D2



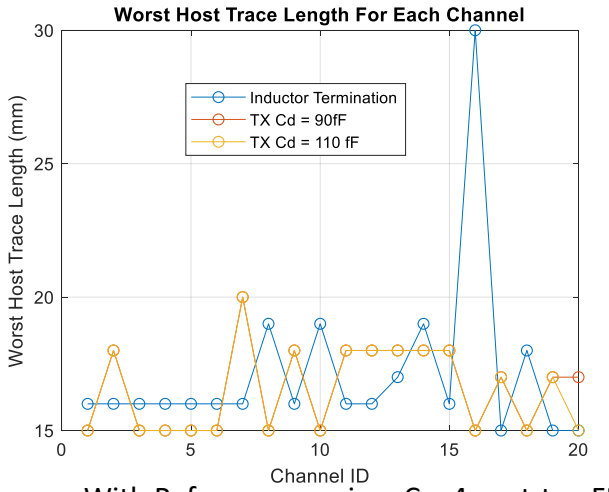


- With Reference receiver D2 – 1 tap DFE (post 2)
- Inductor termination outperforms Cd=90 fF for most channels by up to 3.2dB.
- With inductor termination, VEC threshold can be set to ~10.5 dB to exclude channels 2, 4, 6, 7.

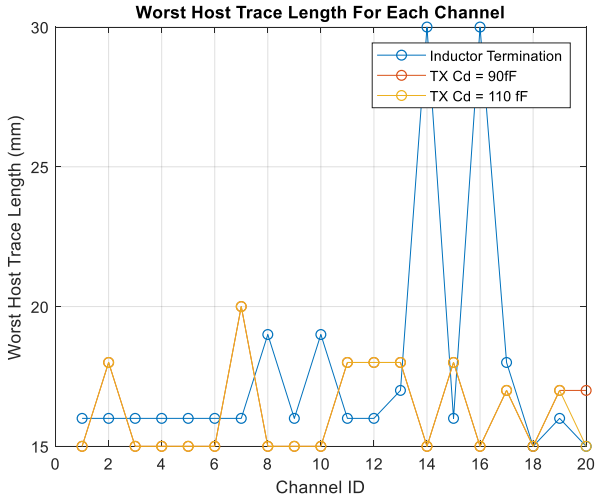
Worst Host Trace Length for TP1a VEC



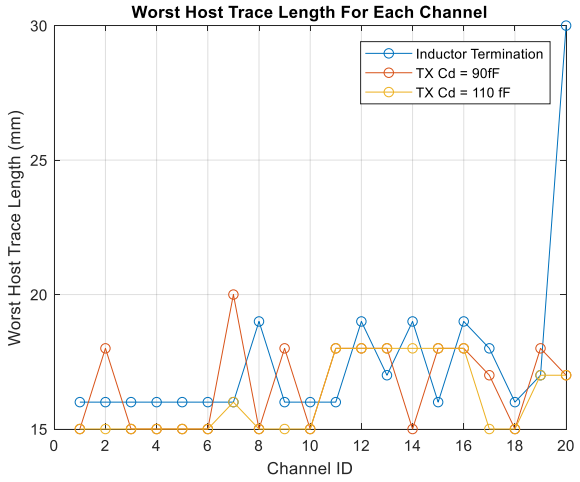
With Reference receiver A – 4 post-tap DFE



With Reference receiver C – 4 post-tap FFE



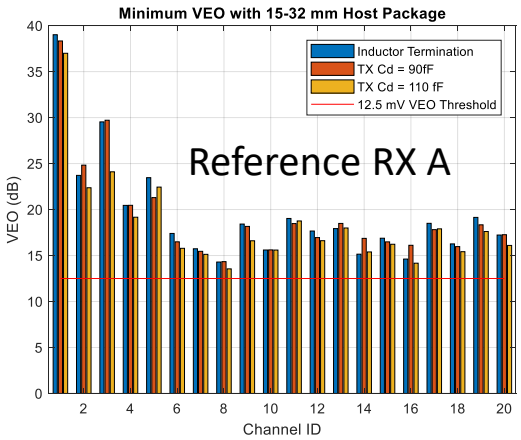
With Reference receiver C2 – 2 post-tap FFE

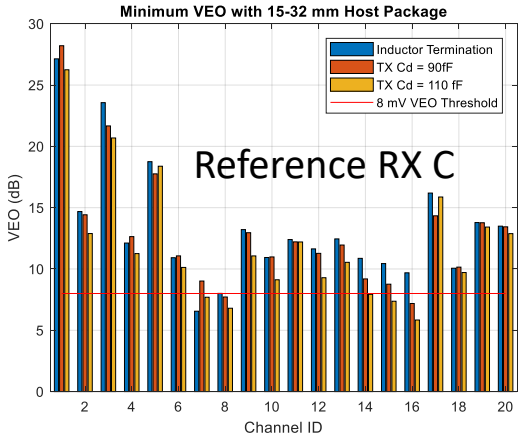


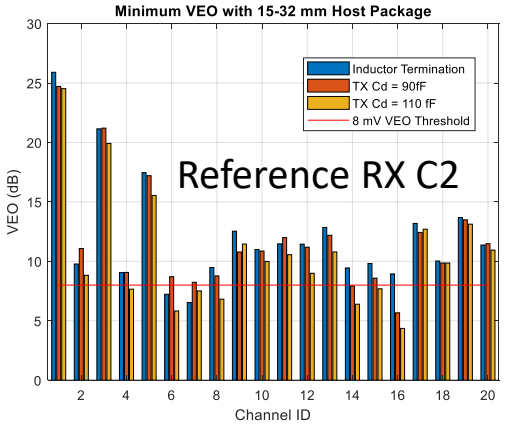
With Reference receiver D2 – 1-tap DFE on post 2

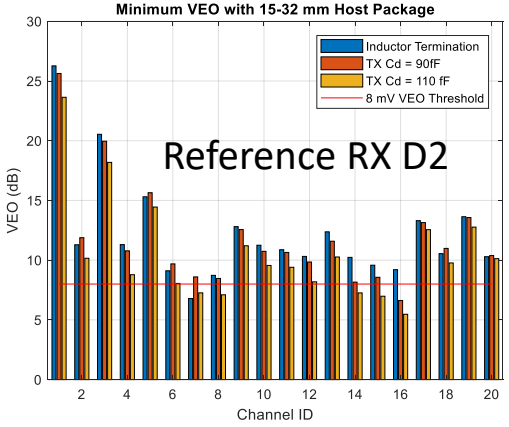
- Worst trace length is termination and channel dependent.

TP1a VEO









- Inductor termination model outperforms Rd 90 fF for VEO with some channels, e.g. channel 14, 15, and 16 with receivers C/C2/D2.

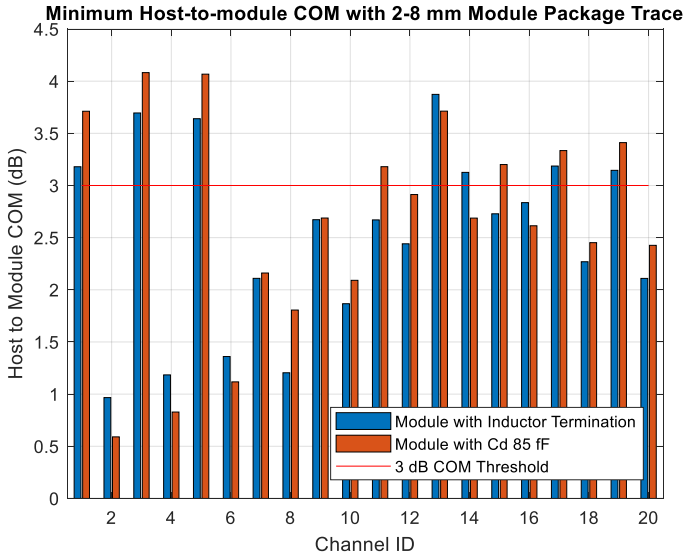
TP1a Summary

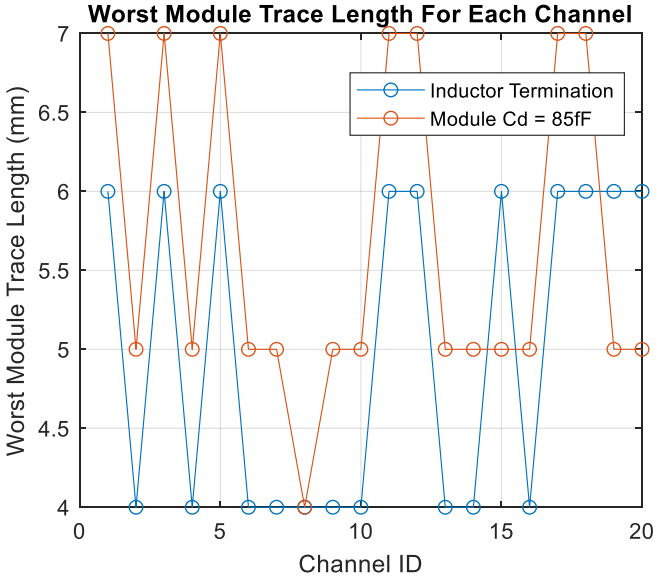
Reference Receiver	A 4-tap DFE	C 5-tap FFE	C2 2-tap FFE	D2 1-tap DFE
VEC Threshold (dB)	8	9.5	10.5	10.5
VEO Threshold (mV)	12.5	8	8	8
Channels not supported with inductor termination	2, 4, 6, 7, 8	2, 4, 6, 7, 8, 15	2, 4, 6, 7	2, 4, 6, 7
Channels not supported with Cd=90 fF	2, 4, 6, 7, 8, 10, 18	2, 4, 6, 7, 8, 14, 15, 16	2, 4, 6, 7, 8, 14, 15, 16	2, 4, 6, 7, 14, 15, 16

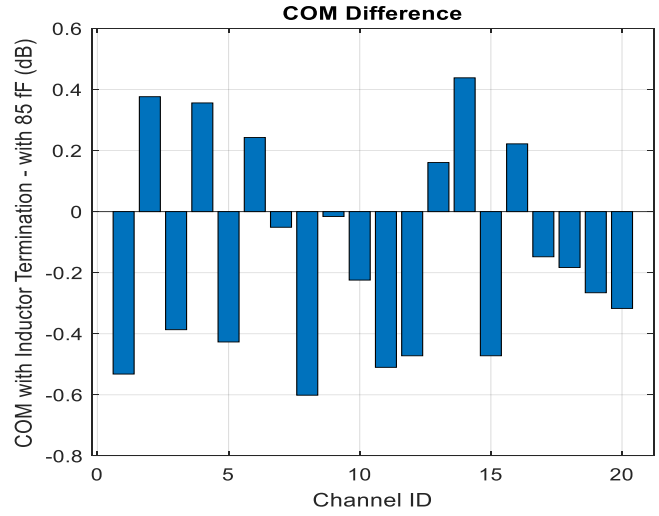
- With inductor termination model, receivers A, C, C2, D2 (and B, D) all can be used as reference receivers to qualify signal at TP1a.
- For different reference receivers, Pass/fail results may be different for some channels voted as TBD by the group (channel 8 and 15).
- Weaker reference receiver is more sensitive to detect channel impairments.
- Inductor termination outperforms 90 fF Cd for channels the group voted to support.

Host-to-module whole-Link Simulation

Whole-Link with TX Set by Receiver C

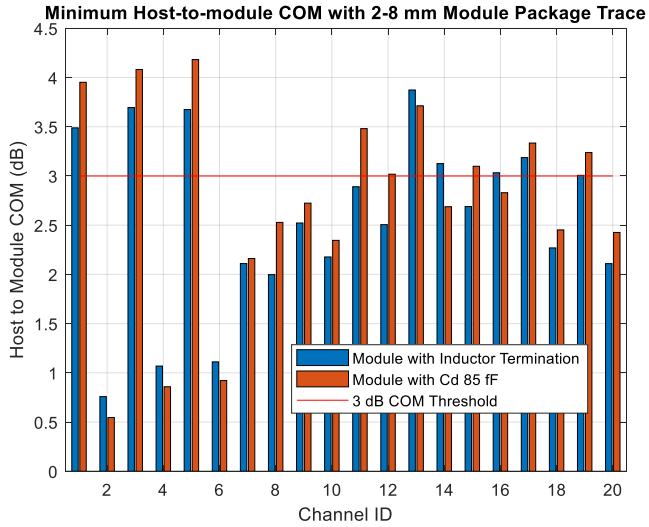


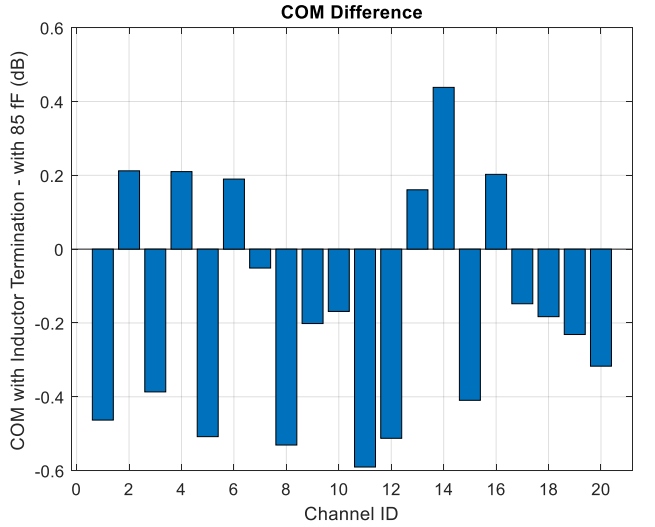


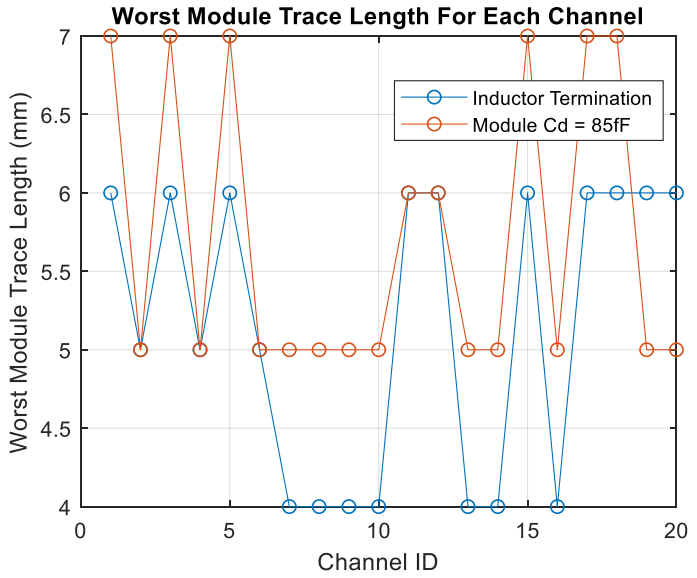


- Real receiver is receiver B (FFE4postDFEtap1).
- TX FIR is set by receiver C. Host trace is 19 mm with inductor model.
- COM value is reported with the worst performance module trace length.
- COM with inductor termination and Cd 85 fF is less than 0.6 dB.

Whole-Link with TX Set by Receiver C2

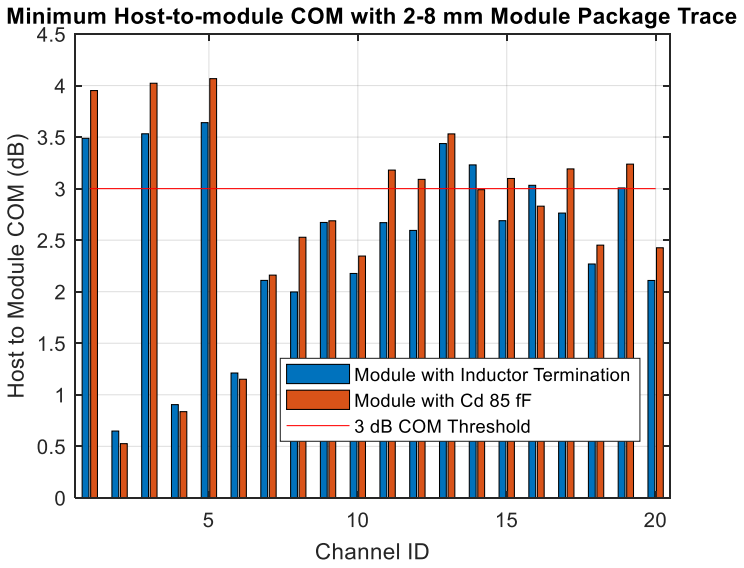


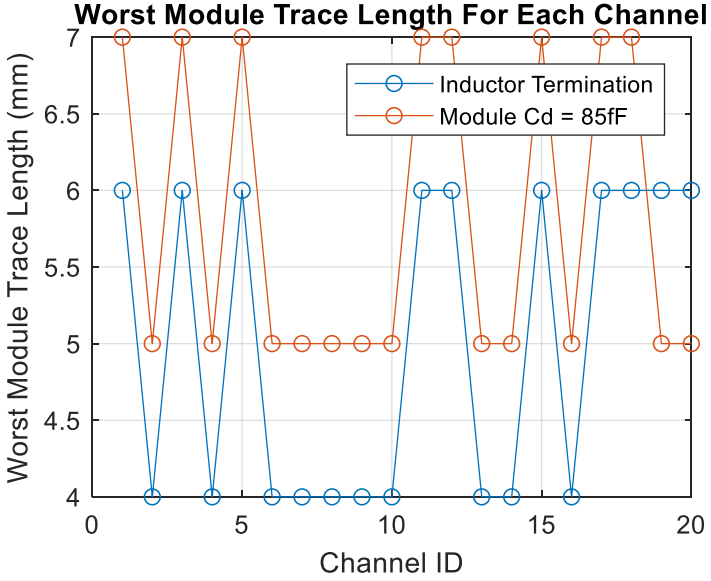


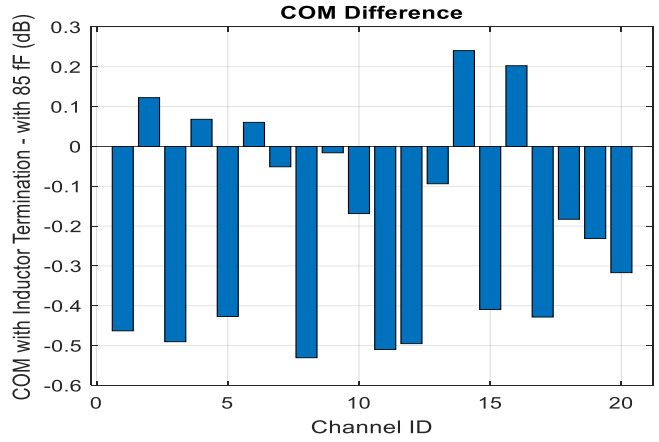


- Real receiver is receiver B (FFE4postDFEtap1).
- TX FIR is set by receiver C2. Host trace is 19 mm with inductor model.
- COM value is reported with the worst performance module trace length.
- COM with inductor termination and Cd 85 fF is less than 0.59 dB.

Whole-Link with TX Set by Receiver D2

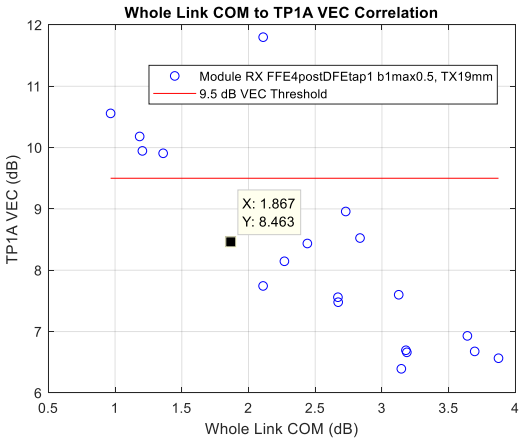




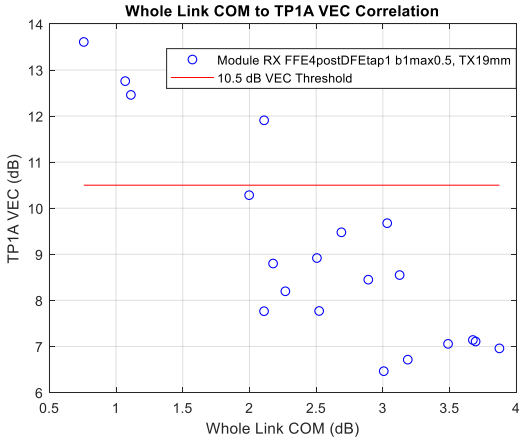


- Real receiver is receiver B (FFE4postDFEtap1).
- TX FIR is set by receiver D2. Host trace is 19 mm with inductor model.
- COM value is reported with the worst performance module trace length.
- COM with inductor termination and Cd 90 fF is less than 0.53 dB.

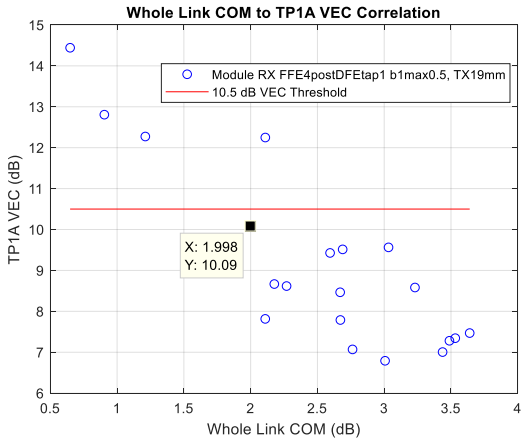
Whole-Link and TP1a Correlation



TX FIR is set by RX C. TP1a VEC threshold is 9.5 dB



TX FIR is set by RX C2. TP1a VEC threshold is 10.5 dB



TX FIR is set by RX D2. TP1a VEC threshold is 10.5 dB

- Real receiver is receiver B (FFE4postDFEtap1).
- Host trace is 19 mm with inductor model.
- Worst performance module trace length is selected for each channel. Module is with inductor termination model.
- VEC threshold is set to 9.5 dB for receiver C and 10.5 dB for receiver C2/D2.
- Correlation is observed between TP1a VEC and whole-link COM.

Host-to-module Whole-Link Summary

- Channels passed TP1a VEC threshold only achieves about 2 dB whole-link COM even with receiver B. DFE tap 1 is still needed for whole-link short equalizers. TP1a criteria needs to be tight enough to qualify module input signal.
- Compared to Cd 85 fF as module termination, the difference of using inductor termination is less than 0.6 dB.

Module-to-host

Module-to-Host Channels

ID	Naming in lim_3ck_02_0709	Description	IL (dB)
1	1a	Module PCB + Connector (new pair) + Host Trace 2”	5.08
2	1b	Module PCB + Connector (new pair) + Host Trace 9” + ASIC BGA footprint (long via)	14.76
3	2a	Module PCB + Connector (legacy pair) + Host Trace 2”)	5.34
4	2b	Module PCB + Connector (legacy pair) + Host Trace 9” + ASIC BGA footprint (long via)	15.05
5	1c	Module PCB + Connector (new pair) + Host Trace 2” + ASIC BGA footprint (long via)	6.00
6	1d	Module PCB + Connector (new pair) + Host Trace 2” + retimer BGA footprint (short via)	5.48
7	1e	Module PCB + Connector (new pair) + Host Trace 2” + retimer BGA footprint (long via)	5.60
8	2c	Module PCB + Connector (legacy pair) + Host Trace 2” + ASIC BGA footprint (long via)	6.19
9	2d	Module PCB + Connector (legacy pair) + Host Trace 2” + retimer BGA footprint (short via)	5.84
10	2e	Module PCB + Connector (legacy pair) + Host Trace 2” + retimer BGA footprint (long via)	5.98

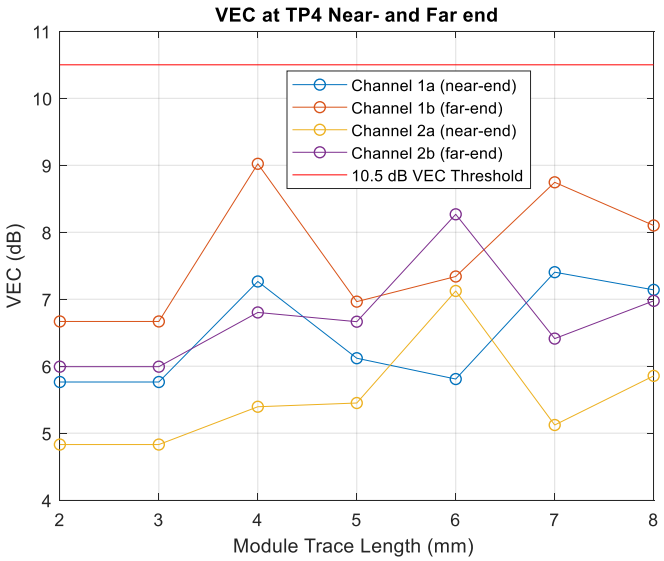
- Module-to-host channels are the same as in lim_3ck_02_0709.

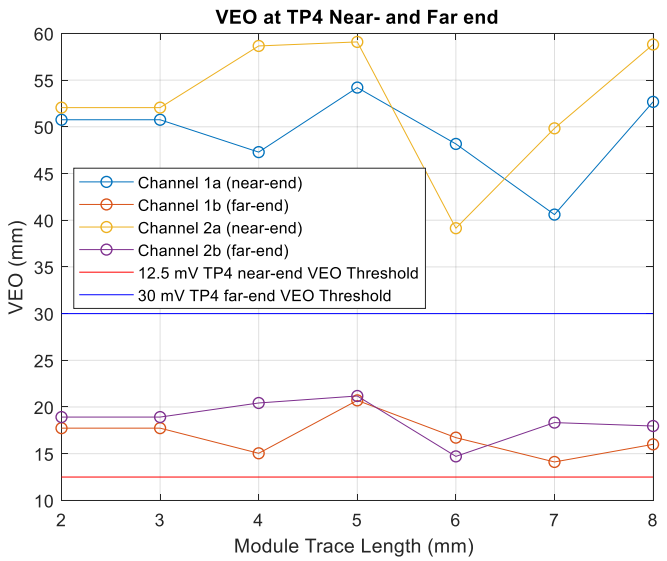
Package Assumptions

- The termination model with inductor is used for host side.
- The simple termination model w/o inductor is used for module per C2M small group discussion.

C_d	0.85e-4	nF
C_p	0.75e-4	nF
Package trace length Z_p	2-8	mm
Package PTH	0	mm

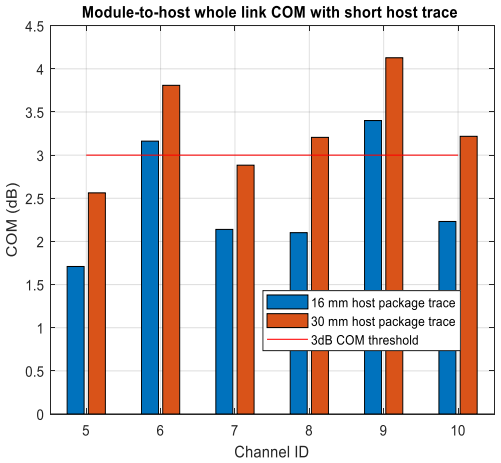
TP4 Simulation



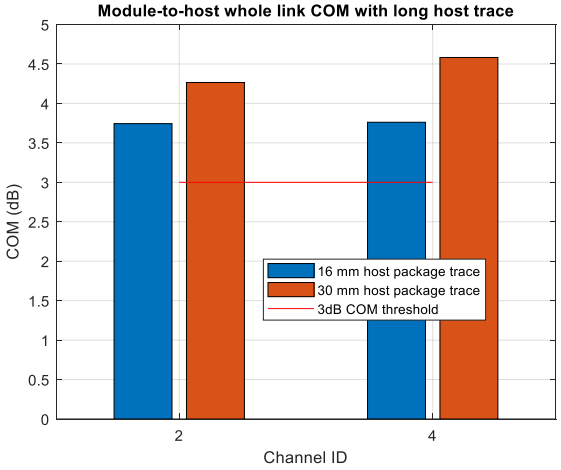


- Used channel 1b/2b to approximate TP4 far-end channel. VEC with TP4 far-end reference channel is likely to be better.
- VEC and VEO are simulated for 2-8 mm module traces.
- Receiver C2 is used here and appears to be sufficient for TP4 .
- TX FIR is optimized for each case. If near-end TX FIR is used for far-end channel, far-end VEC/VEO will be worse.

Module-to-host Whole-link Simulation



TX FIR optimized for channel 1
w/o host package.



TX FIR optimized for channel 2
w/o host package.

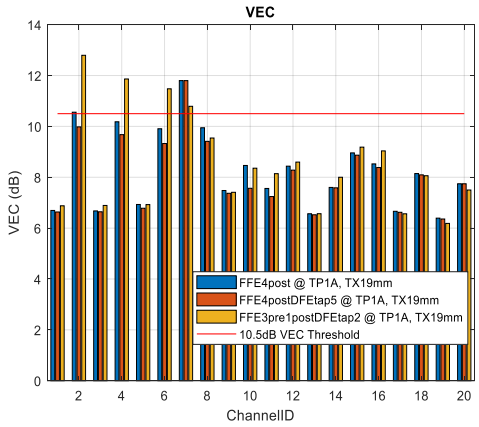
- Receiver B (FFE4postDFE1) is used for whole-link.
- TX FIR is set with receiver C2 (3-tap FFE).
- Module-to-host whole-link channels with short host traces are more challenging.

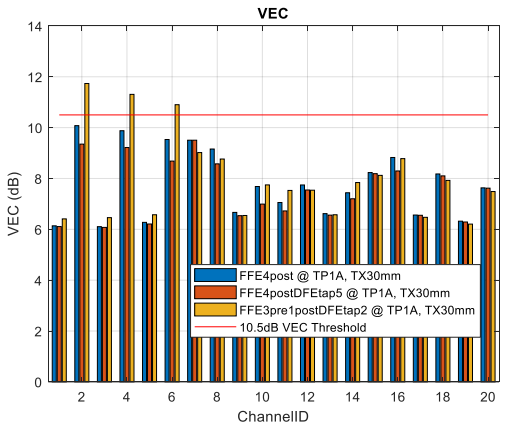
Conclusions

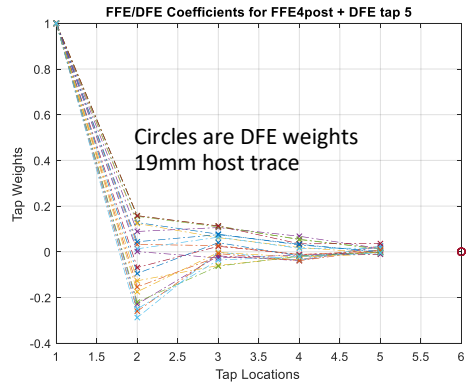
- Inductor termination model outperforms Cd = 90 fF for C2M TP1a signal.
- If the group agrees the performance of inductor on-die termination model is achievable, weaker reference receivers C/D/C2/D2 are sufficient for the simulated channels.
- Whole-link with packages are challenging for short equalizers. Appropriate TP1a/TP4 methodology is needed to ensure whole-link performance by filtering out bad channels and optimizing TX FIR as much as possible.

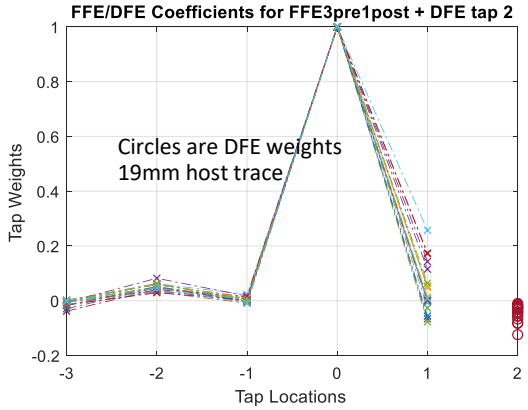
Backup Slides

TP1a- More Receivers









- Implemented two configurations in gopalakrishnan_3ck_01c_0519.
- FFE4post + DFE tap 5 has similar performance as reference RX C.
- FFE3pre1post + DFE tap 2 has similar performance as reference RX C for majority of the channels and weaker than C for some channels.

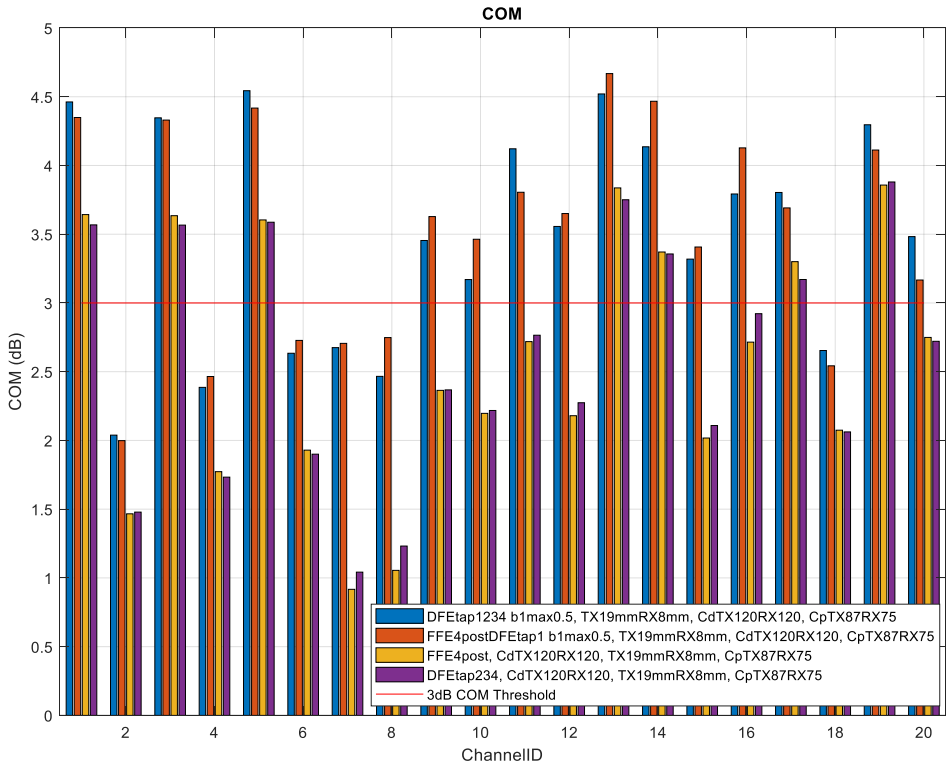
COM Spread Sheet – TP1a With Ref RX C

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\TestCaseFloatingBank\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 , 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	testPkg			Parameter	Setting	
z_p select	[1]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[16 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[16 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	119	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.391	V	vp/vf=.694		TDR and ERL options						
A_fe	0.391	V	vp/vf=.694		TDR	1	logical				
A_ne	0.489	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	400					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.6		min		beta_x	0.00E+00					
c(-1)	[-0.3:0.02:0]		[min:step:max]		rho_x	0.32					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0	enter sec				
c(-3)	[-0.04:.02:0.0]		[min:step:max]		TDR_W_TXPKG	1					
c(1)	[-0.1:0.05:0]		[min:step:max]		N_bx	4	UI				
N_b	0	UI			Receiver testing						
b_max(1)	0				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter						
f_z	12.58	GHz			sigma_RJ	0.01	UI				
f_p1	20	GHz			A_DD	0.02	UI				
f_p2	28	GHz			eta_0	8.20E-09	V^2/GHz				
g_DC_HP	[-3:1:0]		[min:step:max]		SNR_TX	33	dB				
f_HP_PZ	1.328125	GHz			R_LM	0.95					
ffe_pre_tap_len	0	UI									
ffe_post_tap_len	4	UI									
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	0										

COM Spread Sheet – TP1a With Ref RX D2

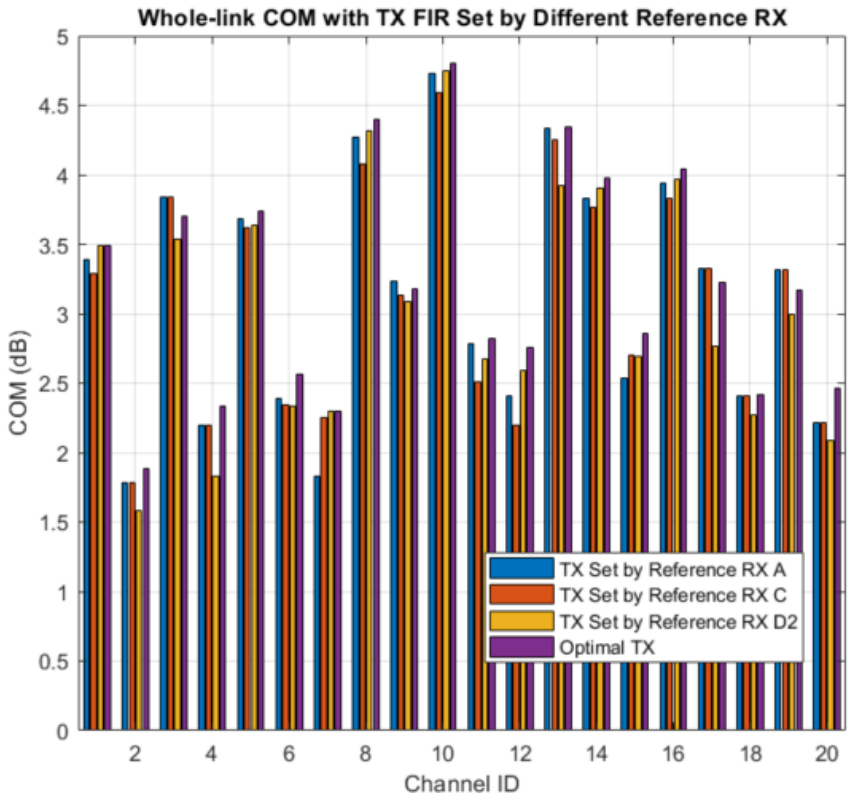
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\TestCaseFloatingBank\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 , 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	testPkg			Parameter	Setting	
z_p select	[1]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[16 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[16 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	119	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.391	V	vp/vf=.694		TDR and ERL options						
A_fe	0.391	V	vp/vf=.694		TDR	1	logical				
A_ne	0.489	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	400					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.6		min		beta_x	0.00E+00					
c(-1)	[-0.3:0.02:0]		[min:step:max]		rho_x	0.32					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0	enter sec				
c(-3)	[-0.04:.02:0.0]		[min:step:max]		TDR_W_TXPKG	1					
c(1)	[-0.1:0.05:0]		[min:step:max]		N_bx	4	UI				
N_b	2	UI			Receiver testing						
b_max(1)	0				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter						
f_z	12.58	GHz			sigma_RJ	0.01	UI				
f_p1	20	GHz			A_DD	0.02	UI				
f_p2	28	GHz			eta_0	8.20E-09	V^2/GHz				
g_DC_HP	[-3:1:0]		[min:step:max]		SNR_TX	33	dB				
f_HP_PZ	1.328125	GHz			R_LM	0.95					
ffe_pre_tap_len	0	UI									
ffe_post_tap_len	0	UI									
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	0										

Whole Link



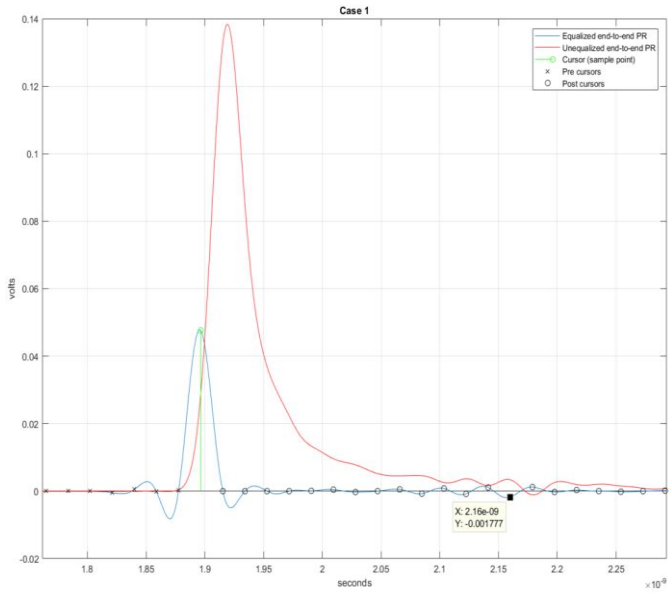
- Both host and module are with inductor termination models
- TX is set by reference RX D2.
- Short equalizers need b1max =0.5 to cover whole link.

Reference RX Impact on TX Settings

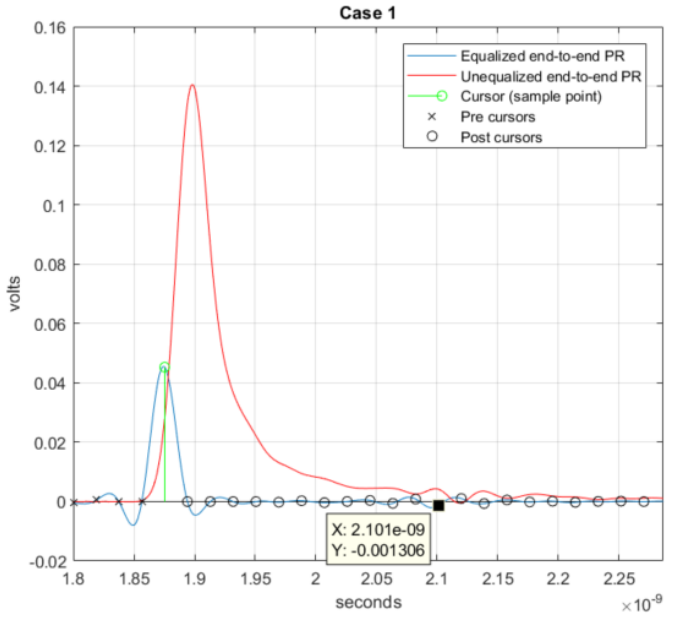


Performance penalty by setting TX FIR using reference receivers is within 0.5 dB.
Similar behavior/penalty is observed for all reference receivers.

Channel 7 Pulse Response



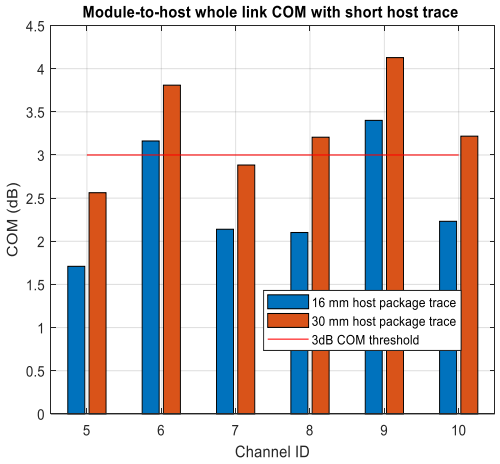
With inductor termination



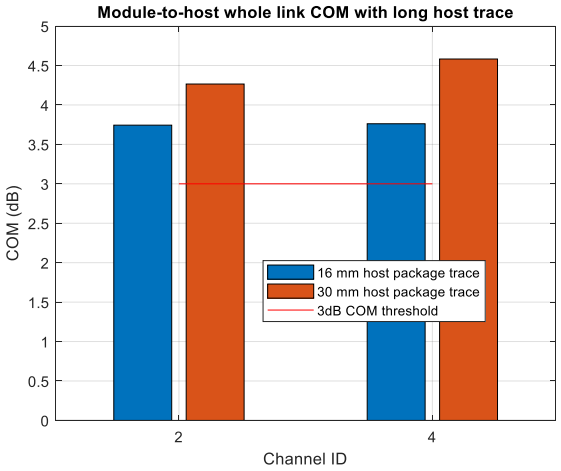
With Cd 90 fF

- Host package reflection is the major contributor of VEC difference.

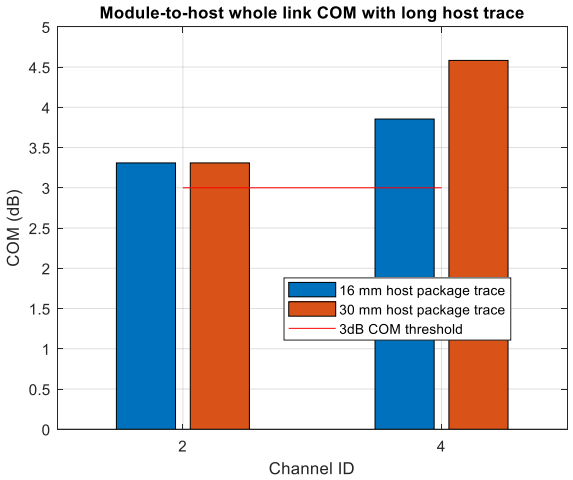
Module-to-host Whole-link Simulation



TX FIR optimized for channel 1 w/o host package.



TX FIR optimized for channel 2 w/o host package.



TX FIR optimized for channel 1 w/o host package.

- Receiver B (FFE4postDFE1) is used for whole-link.
- TX FIR is set with receiver C2 (3-tap FFE).
- Module-to-host whole-link with short host traces is more challenging.