CR Baseline Proposal Considerations at Compliance Points

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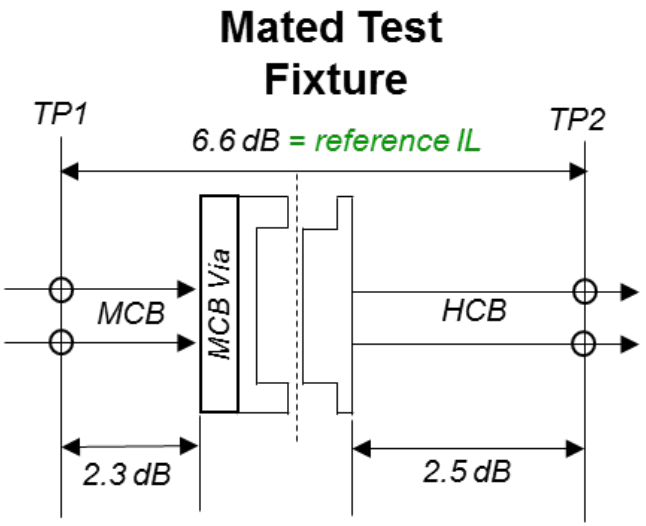
Review – CR baselines

- 162.9 PMD electrical characteristics
  - Tx requirements - compliance at TP2
  - Rx requirements - compliance at TP3
- 162.11 Cable assembly characteristics
  - requirements - compliance at TP0-TP4
- 162.10 Channel characteristics - Channel information TP0-TP5 – Annex 162A
- Annex 162A (informative) – **TP0 and TP5 test point parameters and channel characteristics**
- **Annex 162B (normative)– Test fixtures (adopted)**
- **Annex 162C (normative)– MDIs (adopted)**
- Annex 162D – (informative) Host and cable assembly form factors

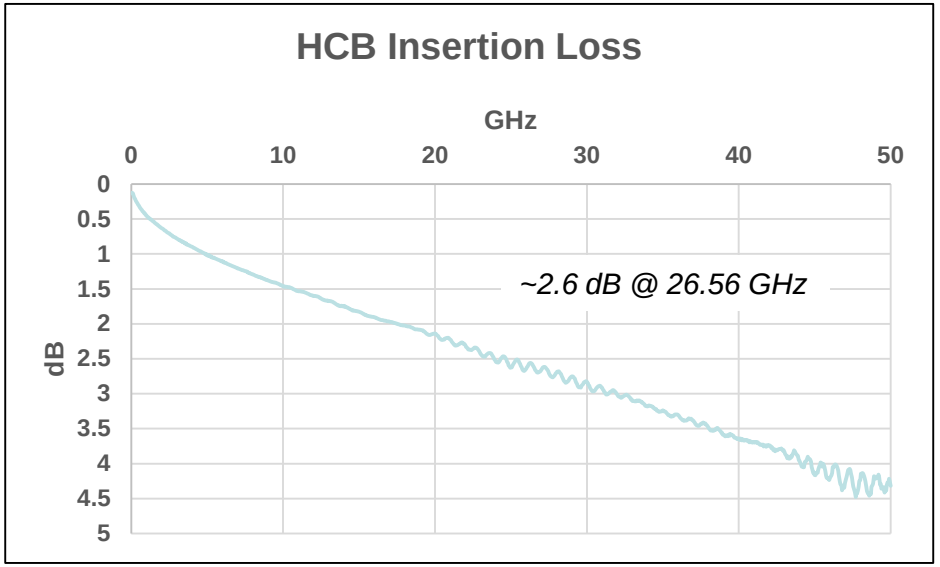
Table 136–7—Test points

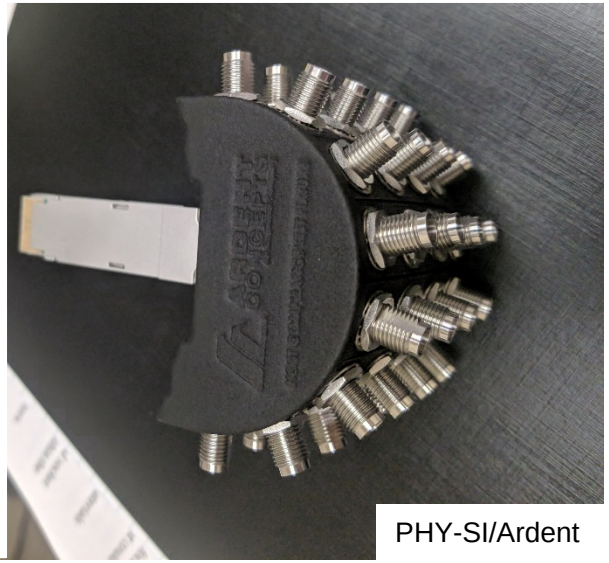
Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of Annex 136B, or its equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 136.9.3.2.
TP2	Unless specified otherwise, all transmitter measurements defined in 136.9.3 are made at TP2 utilizing the test fixture specified in Annex 136B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are made at TP3 utilizing the test fixture specified in Annex 136B.

Test Fixtures – adopted - update



Note: 2.3 dB MCB PCB includes test point IL and MCB Via allowance is 0.2 dB





PHY-SI/Ardent

Channel – informative channel

- Cable assembly and Host IL tied to channel IL

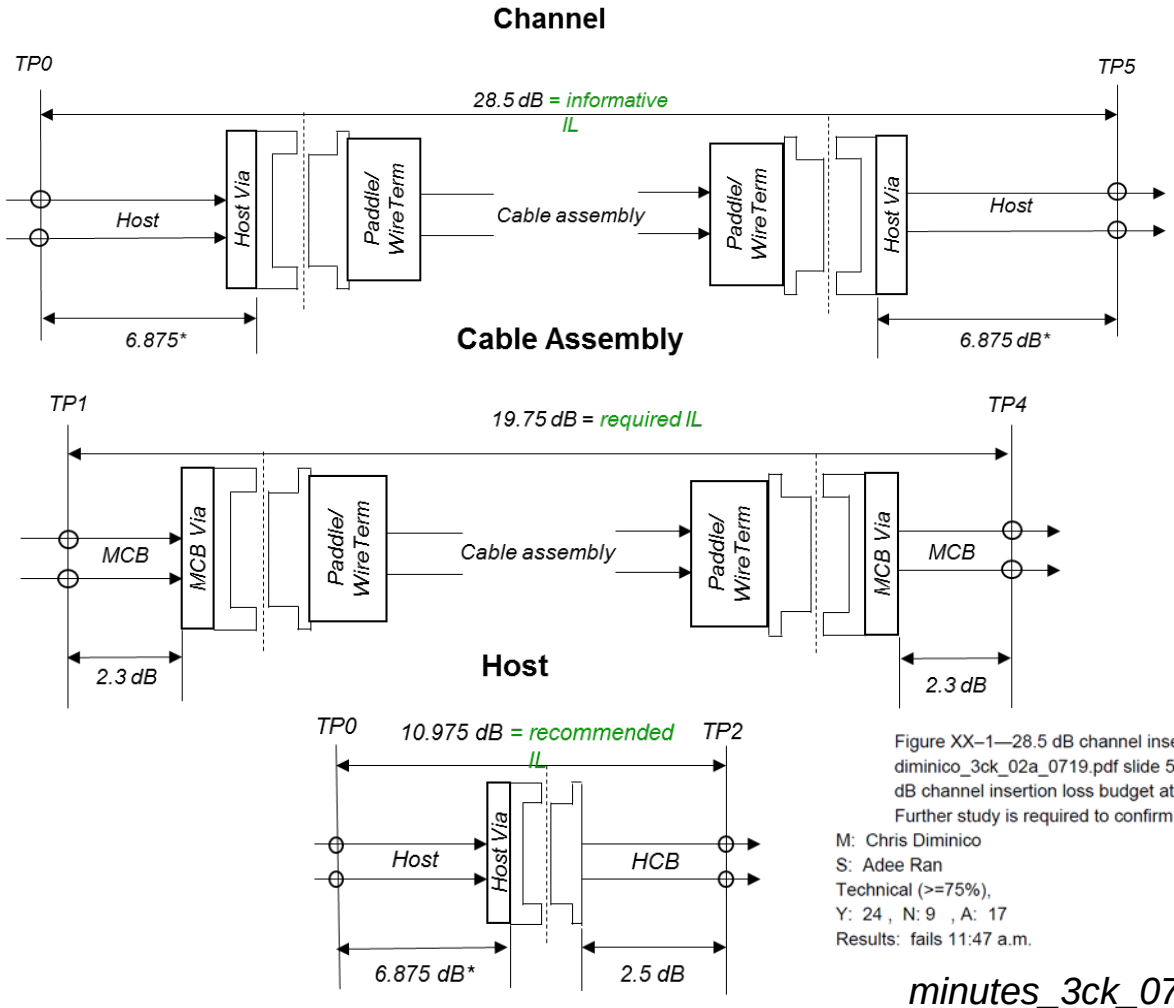


Figure XX–1—28.5 dB channel insertion loss budget at 26.56 GHz in diminico_3ck_02a_0719.pdf slide 5 and slide 6 for Annex 162A - Figure 162A–1—28.5 dB channel insertion loss budget at 26.56 GHz with the addition of an editors note: Further study is required to confirm 28.5 dB. With editorial license

M: Chris Diminico
S: Adee Ran
Technical (>=75%),
Y: 24 , N: 9 , A: 17
Results: fails 11:47 a.m.

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Note: The 6.875 dB includes via allowances for BGA and connector footprint

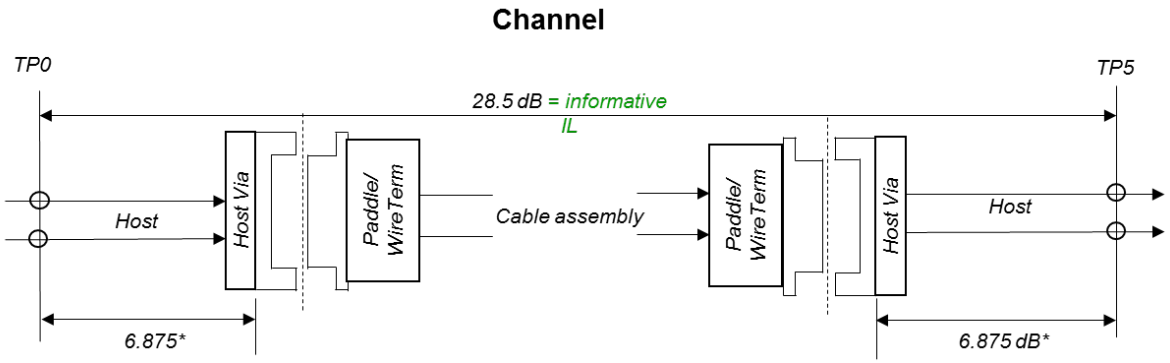
Review – Channel loss budget

- **Backplane objective:**
  - **Define single-lane, two-lane, and four-lane 100 Gb/s PHY(s) for operation over electrical backplanes supporting an insertion loss ≤28 dB at 26.56 GHz.**

Twin-axial objective(s):

- **Define single-lane, two-lane, and four-lane 100 Gb/s PHY(s) for operation over twin-axial copper cables with lengths up to at least 2 m.**
  - **Channel loss budget in informative Annex to provide information on parameters associated with test points TP0 and TP5 that might not be testable in an implemented system.**

Channel – informative channel



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Summary

- The updated 2m CR channels with cable assemblies manufacturing variation have IL close to 28.5 dB
  - Data shows ~0.8 – 1.0 dB COM improvement compared to previously generated 29 dB channels
  - QSFP-DD legacy pair can now pass 3 dB COM target, the DD new pair is missing 0.1dB (under development by Molex)
  - ICN has been improved from ~1.5mV to ~1.2mV, mainly coming from ASIC RX footprint NEXT reduction
- 28.5dB loss budget (informative) looks promising for 2m Cu cable assembly baseline consideration

Tx compliance at TP2

Table 162–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Differential pk-pk output voltage (max.) with Tx disabled[1]	93.8.1.3	30	mV
DC common-mode voltage (max.)[a]	93.8.1.3	1.9	V
AC common-mode RMS output voltage, v_{cmi} (max.)[a]	93.8.1.3	30	mV
Differential pk-pk voltage, v_{di} (max.)[a]	93.8.1.3	1200	mV
Effective return loss (ERL) (min.)	162.9.3.4	See Equation (162–6)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92–3)	dB
Transmitter steady-state voltage, v_f (min.) Transmitter steady-state voltage, v_f (max.)	162.9.3.1.2	0.354 0.6	V
Linear fit pulse peak (min.)	162.9.3.1.2	$0.49 \times v_f$	V
Level separation mismatch ratio R_{LM} (min.)	120D.3.1.2	0.95	—

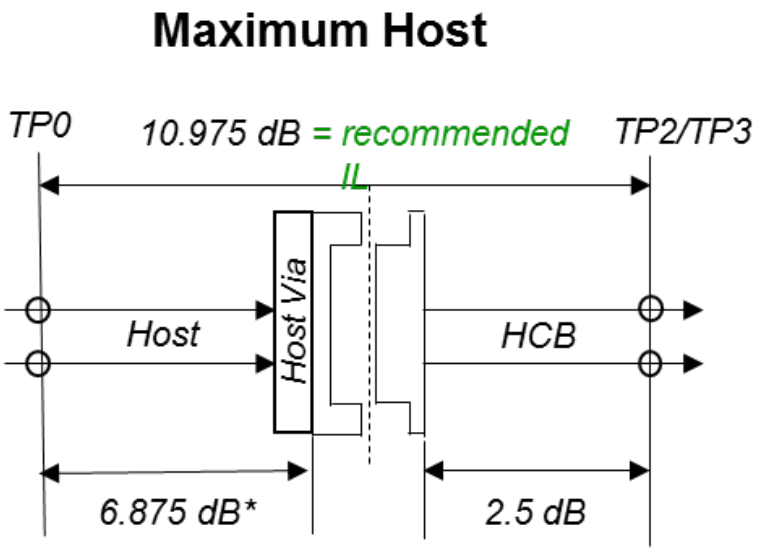
Tx compliance at TP2

Table 162–11—Summary of transmitter specifications at TP2 *(continued)*

Parameter	Subclause reference	Value	Units
Transmitter output waveform			
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (min.)	162.9.3.1.4	0.005	—
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (max.)	162.9.3.1.4	0.05	—
abs step size for $c(-2)$ (min.)	162.9.3.1.4	0.005	—
abs step size for $c(-2)$ (max.)	162.9.3.1.4	0.025	—
value at minimum state for $c(-1)$ and $c(1)$ (max.)	162.9.3.1.5	−0.25	—
value at maximum state for $c(-2)$ (min.)	162.9.3.1.5	0.1	—
Signal-to-noise-and-distortion ratio SNDR (min.)	120D.3.1.6	32.2	dB
Output jitter (max.)[2]			
J_{RMS}	120D.3.1.8	0.023	UI
J3u	162.9.3.3	0.115	UI
Even-odd jitter, pk-pk[3]	120D.3.1.8	0.019	UI
Signaling rate		53.125 ± 100 ppm	GBd
Unit interval nominal		18.82353	ps

[1]Measurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.
[2]J3u, J_{RMS}, and even-odd jitter measurements are made with a single transmit equalizer setting selected to compensate for the loss of the host channel
[3]If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed.

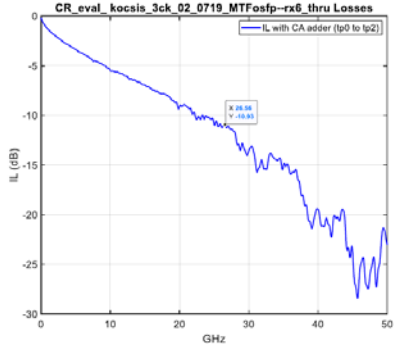
Tx/Rx compliance at TP2/TP3

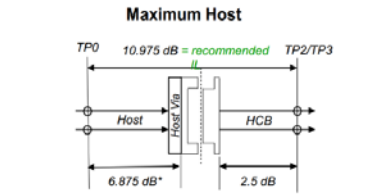


Note: The 6.875 dB includes via allowances for BGA and connector footprint

Tx requirements - compliance at TP2

MTF and COM CA Host Adder Insertion Loss is ~ 10.97 dB

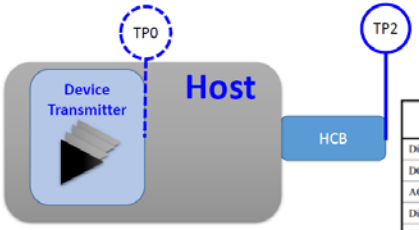




*Note: The 6.875 dB includes via allowances for BGA and connector footprint

diminico_3ck_cu cable 8-12-19

Review: Parameters we are looking to specify



We going after V_f and the ratio of P_{max}/V_f

Table 136–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Differential pk-pk output voltage (max.) with Tx disabled[a]	93.8.1.3	30	mV
DC common-mode voltage (max.)[a]	93.8.1.3	1.9	V
AC common-mode RMS output voltage, v_{ccm} (max.)[a]	93.8.1.3	30	mV
Differential pk-pk voltage, v_{df} (max.)[a]	93.8.1.3	1200	mV
Effective return loss (ERL) (min.)	136.9.3.4	See Equation (136–6)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92–3)	dB
Transmitter steady-state voltage, v_f (min.) Transmitter steady-state voltage, v_f (max.)	136.9.3.1.2	0.354 0.6	V
Linear fit pulse peak (min.)	136.9.3.1.2	$0.49 \times v_f$	V
Level separation mismatch ratio R_{LM} (min.)	120D.3.1.2	0.95	—

Choices

- Choice c might be suggested from the doubled baud rate used for 50 G PAM4
- Choice e might be suggested since the fit is using N_v=200. The longer time range of the step response would have better sensitivity to loss.
- Recommend the choice be used for all 100 Gb/s PMDs which use the fitted pulse parameters

	N_v (UI)	N_b (UI)	V_f (mV)	P_max/V_f
a	13	9	350	0.446
b	16	12	359	0.436
c	26	22	371	0.411
d	44	40	385	0.397
e	200	-	387	0.397

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Rx compliance at TP3

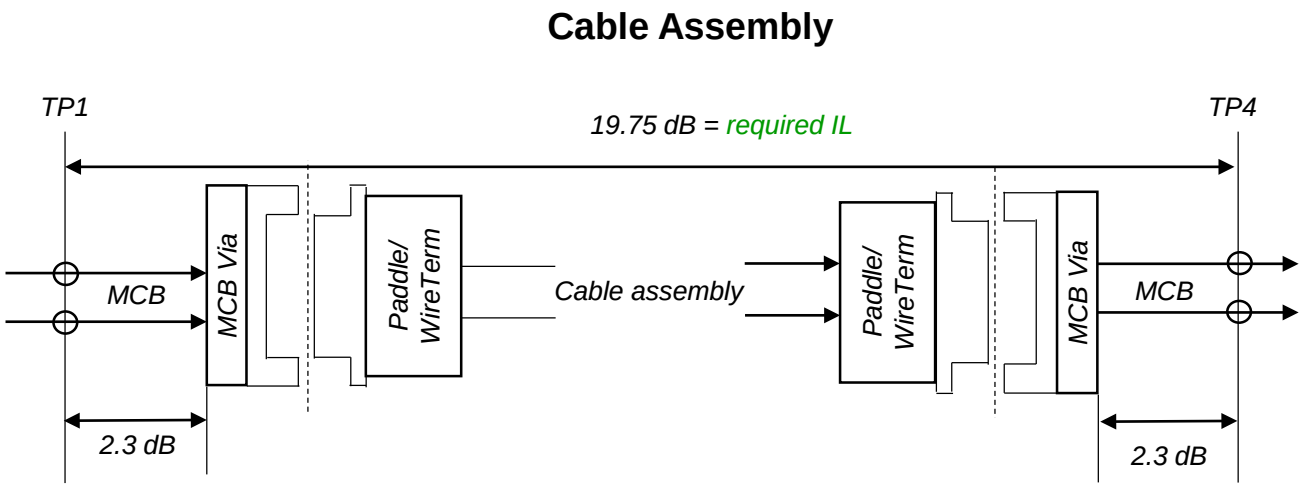
Table 162–14—Summary of receiver specifications at TP3

Parameter	Subclause reference	Value	Units
Input amplitude tolerance	162.9.4.1	1200[1]	mV
Interference tolerance	162.9.4.2	Table 136–15	—
Jitter tolerance	162.9.4.3	Table 120D–7	—
Signaling rate	162.9.4.4	53.125 ± 100 ppm	GBd
ERL (min.)	162.9.4.5	10	dB
Differential to common-mode input return loss	92.8.4.3	Equation (92–21)	dB

[1]Amplitude is measured at TP2.

Cable assembly compliance TP0-TP4

- Cable assembly IL tied to channel IL
  - Cable assembly baseline has been contingent on channel IL resolution



Cable assembly – baseline

- Cable assembly specifications – Adopt CL136 – referenced parameters @ 26.56 GHz, f=0.01≤f≤38 (signaling rate 53.125 GBd).

Cable assembly characteristics summary

Parameter description	Value	Unit
Maximum insertion Loss	19.75	dB
Minimum Insertion Loss	11.15	dB
Minimum ERL	TBD	dB
Differential to Common-mode return loss	Equation(TBD)	dB
Differential to Common-mode conversion loss	Equation(TBD)	dB
Common-mode to common–mode return loss	Equation(TBD)	dB
Minimum COM	TBD	dB

http://www.ieee802.org/3/ck/public/19_03/diminico_3ck_01_0319.pdf

Cable Assembly COM- Baseline

- COM - consistent with methodology CL136 – signaling rate 53.125 GBd
- COM parameter values TBD

Table 136–18—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step[a]	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface Package transmission line characteristic impedance	 C_d z_p z_p C_p Z_c	 1.8×10^{-4} 12 30 1.1×10^{-4} 95	 nF mm mm nF Ω
Single-ended reference resistance	R_0	50	Ω

TBD

Table 136–18—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.25 0 0.05	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.1 0.025	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b / 2.5$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 2.5$ $2 \times f_b$	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	$f_b / 40$	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.415 0.415 0.604	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit for $n = 1$ for $n = 2$ to N_b	$b_{max}(n)$	 0.7 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI

TBD

http://www.ieee802.org/3/ck/public/19_03/diminico_3ck_01_0319.pdf

Proposals for parameters- contributions required

- **TX – Parameters Table 162–8 transmitter specifications at TP2**
  - **Suggest host loss budget – slide 9**
- **RX – Parameters Table 162–11 receiver specifications at TP3**
  - **Suggest host loss budget – slide 9**
- **Cable assembly - Table 162–13—Cable assembly characteristics**
  - **Cable assembly baseline has been contingent on channel IL resolution**
  - **Suggest cable assembly loss budget – slide 12**
- **Channel - 162.10 - Annex 162A - Channel information TP0-TP5**
  - **Consider *differences* in 28 dB channels that pass COM and 28.5 dB channels that fail COM.**

Recommendation

- **Motion:**
  - **Move to give editorial license to revise Annex 162D – (informative) Host and cable assembly form factors based on adopted MDIs in Annex 162C (normative).**

Supporting slides

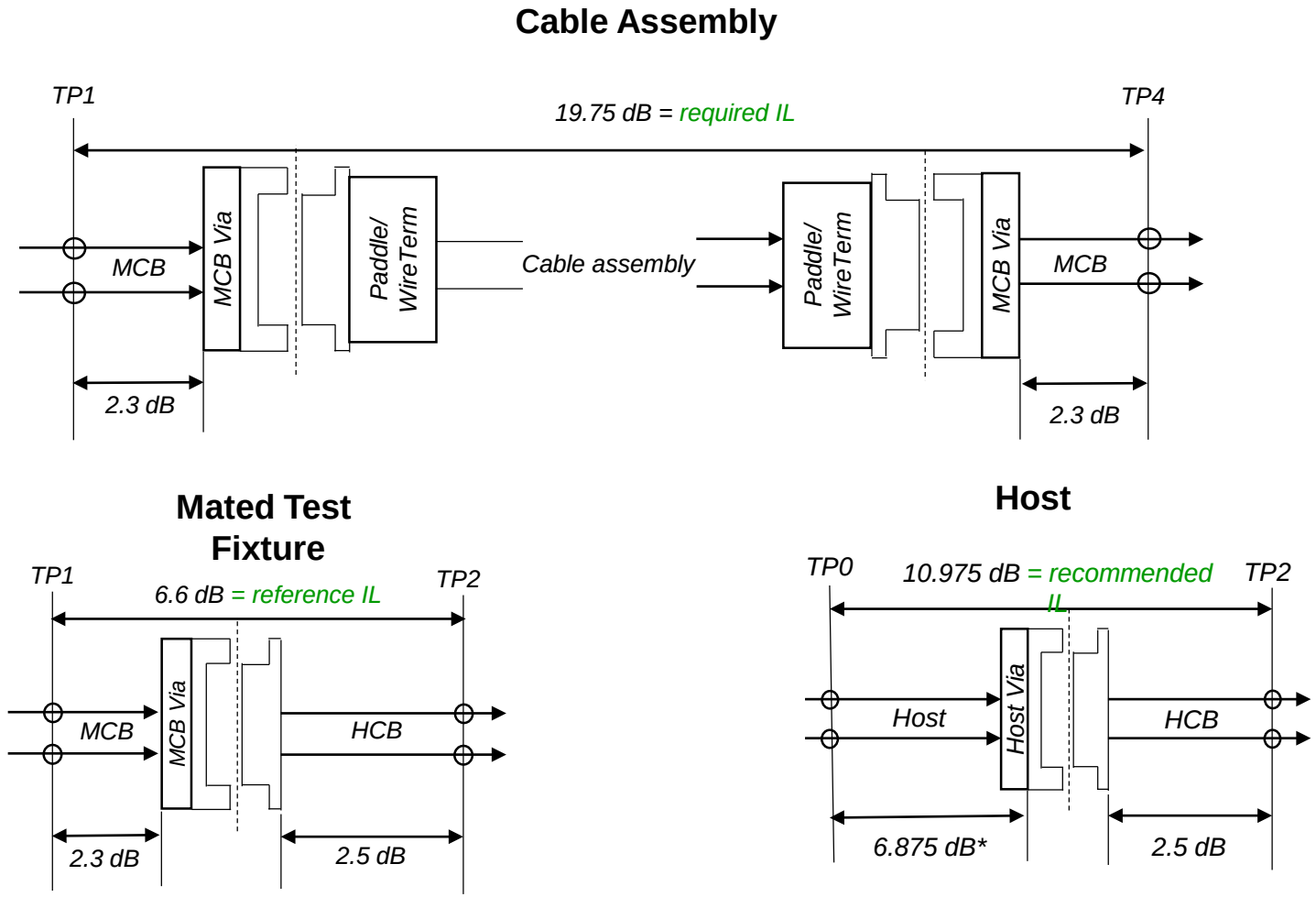
Overview

Component	802.3cd Insertion Loss dB @ 13.28 GHz	802.3ck Insertion Loss dB @ 26.56 GHz (proposed)	Comment
Module Compliance Board (MCB) PCB	1.2	2.3	
Host Compliance Board (HCB) PCB	1.38	2.5	
Host	7	6.875	cd-The 7 dB did not include explicit allowances for BGA and connector footprint ck-The 7 dB includes allowance of 1.34 dB for BGA (0.73) via and connector footprint via (0.61)
Host Connector	1.07+0.62	1.6	cd-The host connector is allocated 0.62 dB of additional margin ck- The host connector mating interface is allocated 0.3 dB variation allowance (not including via)
Mated Test Fixture (MTF)	3.65	6.6	
MTF connector	1.07	1.6	ck-includes 0.2 dB via allowance
Bulk cable and wire attachment	12.62	11.55	cd(3m), ck(2m)
Channel	30	28.5	

- Host and Mated test fixture connector mating interfaces are the same >>1.3 dB + variation 0.3 dB = 1.6 dB.
- Variation is to account for multiple MDIs and other factors other than implementation or margin.

MTF IL = 2.3(MCB PCB)+1.6(conn)+0.2(via)+2.5(HCB PCB) =6.6 dB
Host Channel IL =6.875(Host PCB and via's)+1.6(conn)+2.5(HCB PCB) = 10.975 dB
Channel IL =2*6.875(Host PCB and via's)+2*1.6(conn)+11.55(cable and wire termination) = 28.5 dB

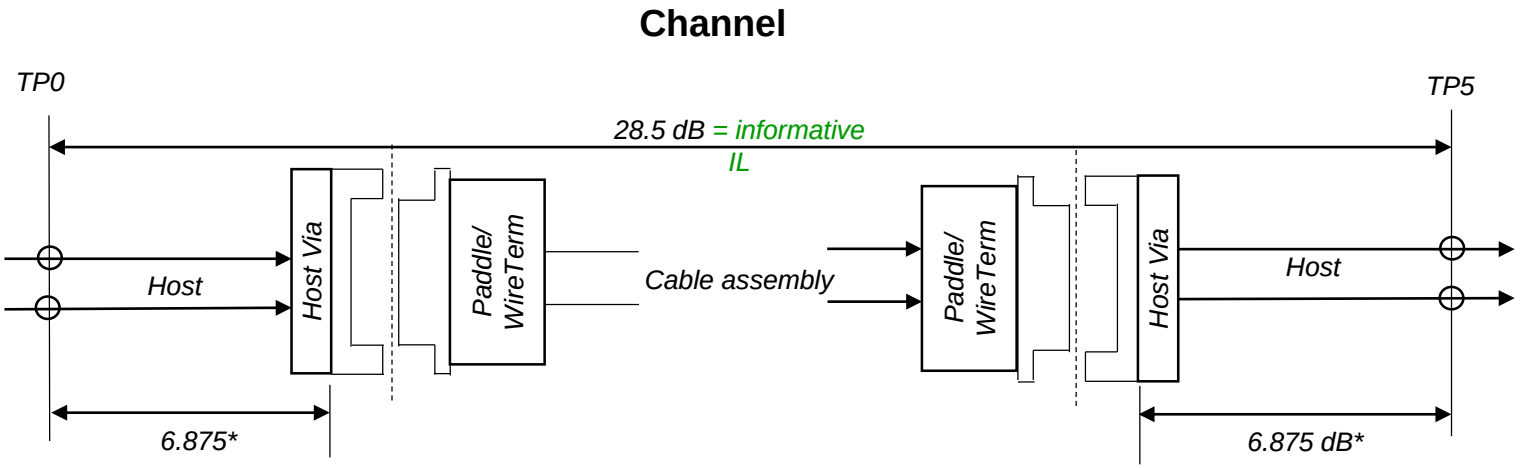
802.3ck Figure XX–1—28.5 dB channel insertion loss budget at 26.56 GHz



Note: 2.3 dB MCB PCB includes test point IL and MCB Via allowance is 0.2 dB

Note: The 6.875 dB includes via allowances for BGA and connector footprint

802.3ck Figure XX–1—28.5 dB channel insertion loss budget at 26.56 GHz



Channel IL = 28.5 dB @26.56 GHz =2*(6.875+1.6)+11.55

Note: Channel IL derived from cable assembly host, and mated test fixture IL=28.5 dB @26.56 GHz =2*(6.875+1.6)+11.55