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Comparison of C2M performance at TP1a with whole channel performance.

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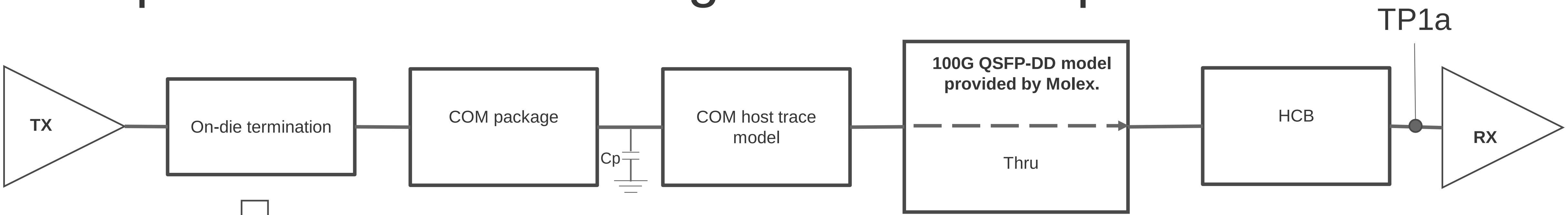
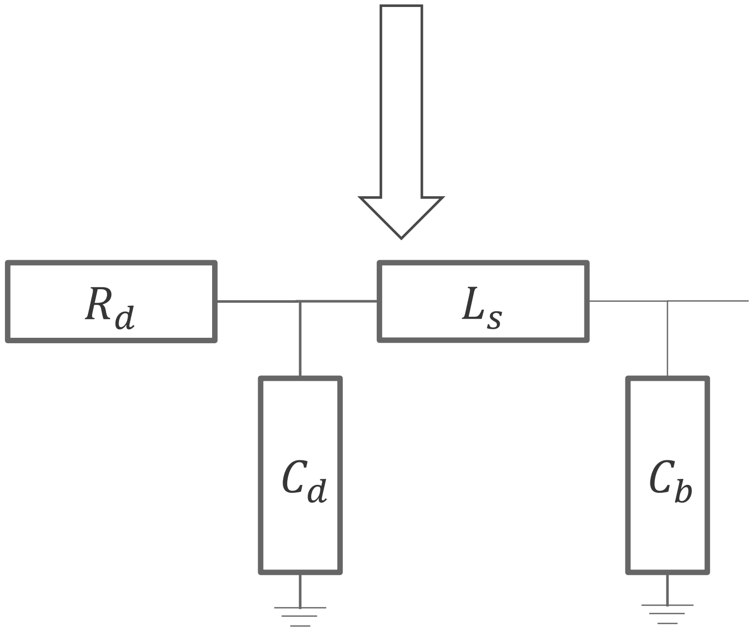
Introduction

- Dudek_3ck_01_0719 explored the effect of host trace length on C2M TP1a performance with different die models, package lengths and some host impairments. It showed significant degradations and resonances at shorter host trace lengths. Unfortunately the "good host trace lengths" became "bad host trace lengths" if the connector lane or details of the die model etc. were changed. I.e. It is not possible to choose "good" lengths. The system needs to be designed to cope with the bad resonances.
- Since then the inductor model has been adopted for the host ASIC die model.
- This presentation provides more TP1a simulations with this host ASIC die model and presents simulations of the whole channel performance.
- It shows that a significantly stronger equalizer than the 5 tap FFE equalizer is required for adequate whole channel performance.
- The presentation also provides correlation between the VEC performance at TP1a and the whole channel performance and discusses the problem of setting a specification at TP1a.

Chip to module block diagram for TP1a performance





On-die inductor termination

- HCB trace: 100ohm 63.8mm (2.5dB loss) (from COM model)
- TX/RX termination Rd: 50ohm
- Package trace length: 11.5mm unless stated otherwise
- Host die model Ls=120pH, Cd=120fF, Cb=30fF
- Sweep host trace length
- Host trace impedance: 80/90/100/110ohm
- Av: 0.415V A_ne: 0.608V A_fe: 0.415V
- Crosstalk is not included.
- Lane 3 Is used for the simulations if not stated otherwise.
- 4 tap DFE is used unless stated otherwise
- Eta0=8.2e-9 and TxSNR= 33dB unless stated otherwise.
- Performance is simulated using COM 2.70
- The complete COM table is in the back-up

	filter and Eq		
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	4	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
Include PCB	1	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

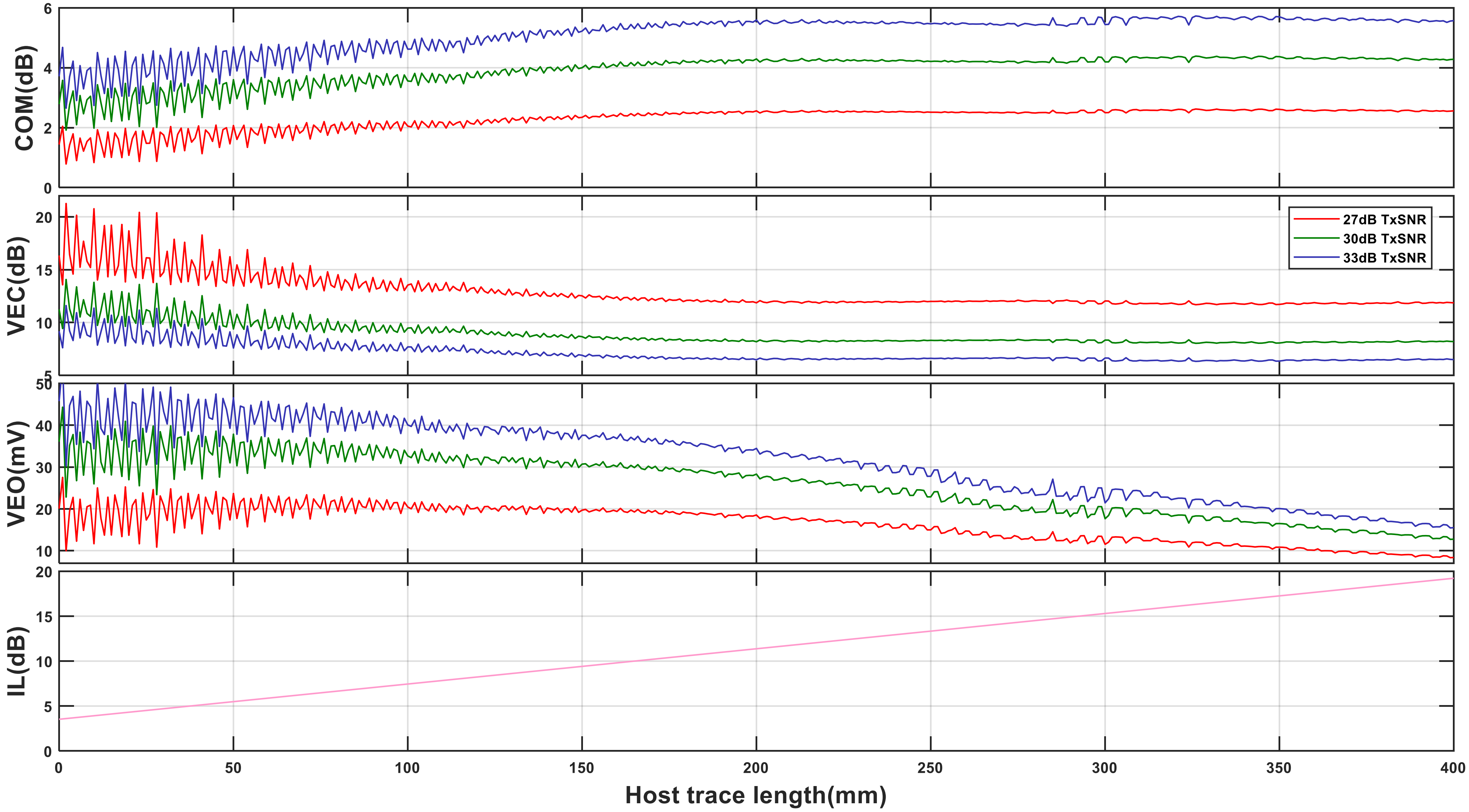
4-tap DFE RX

COM PCB and package loss information

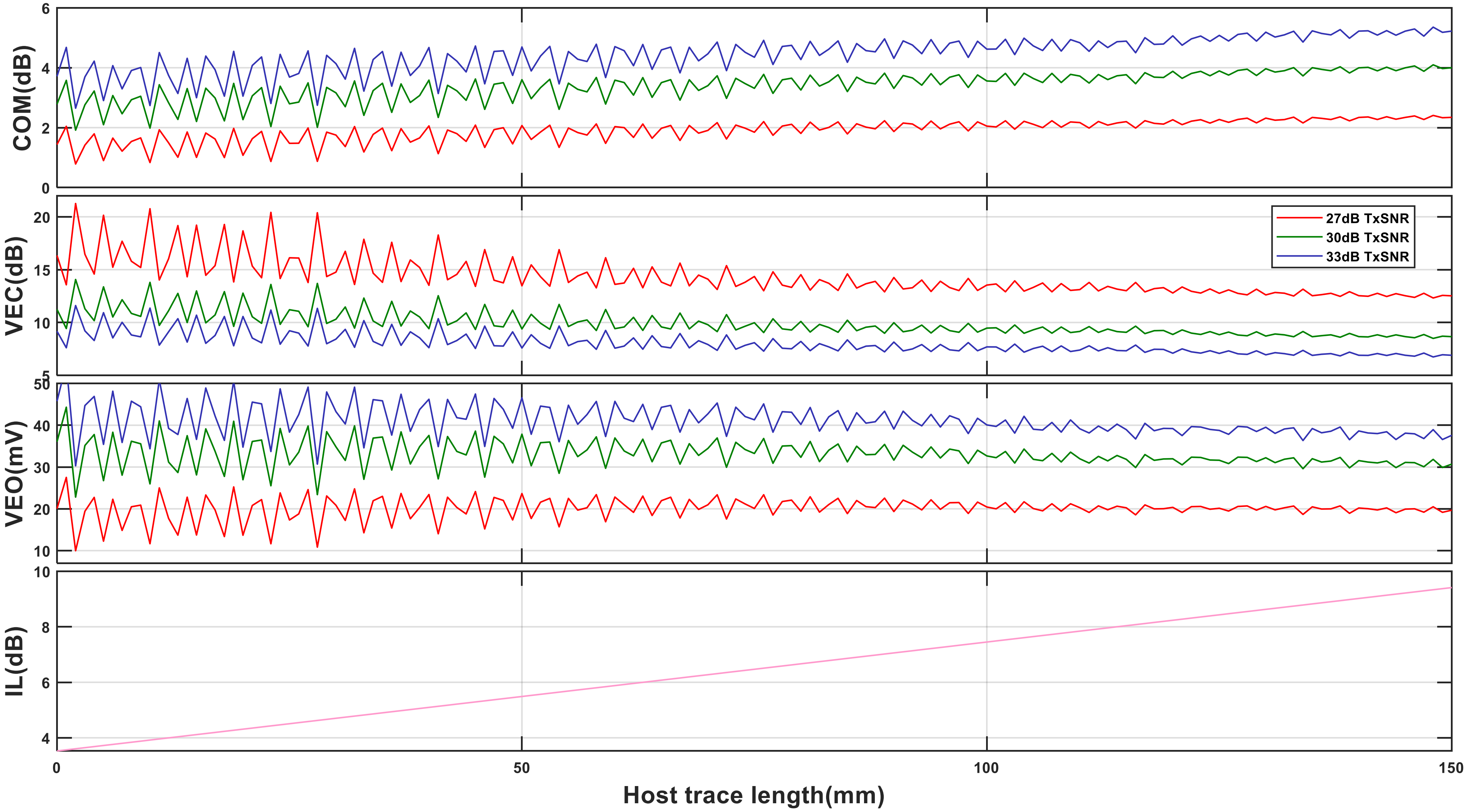
- PCB loss at 26.56GHz: ~0.04dB/mm, ~1dB/in.   (58mm is equivalent to the 2.3dB MCB loss being proposed in the cable small group).
- Package loss at 26.56GHz: 0.1dB/mm
- Insertion loss plotted in this presentation includes host, HCB and connector, but not package.

Effect of TXSNR

TP1a results by TxSNR

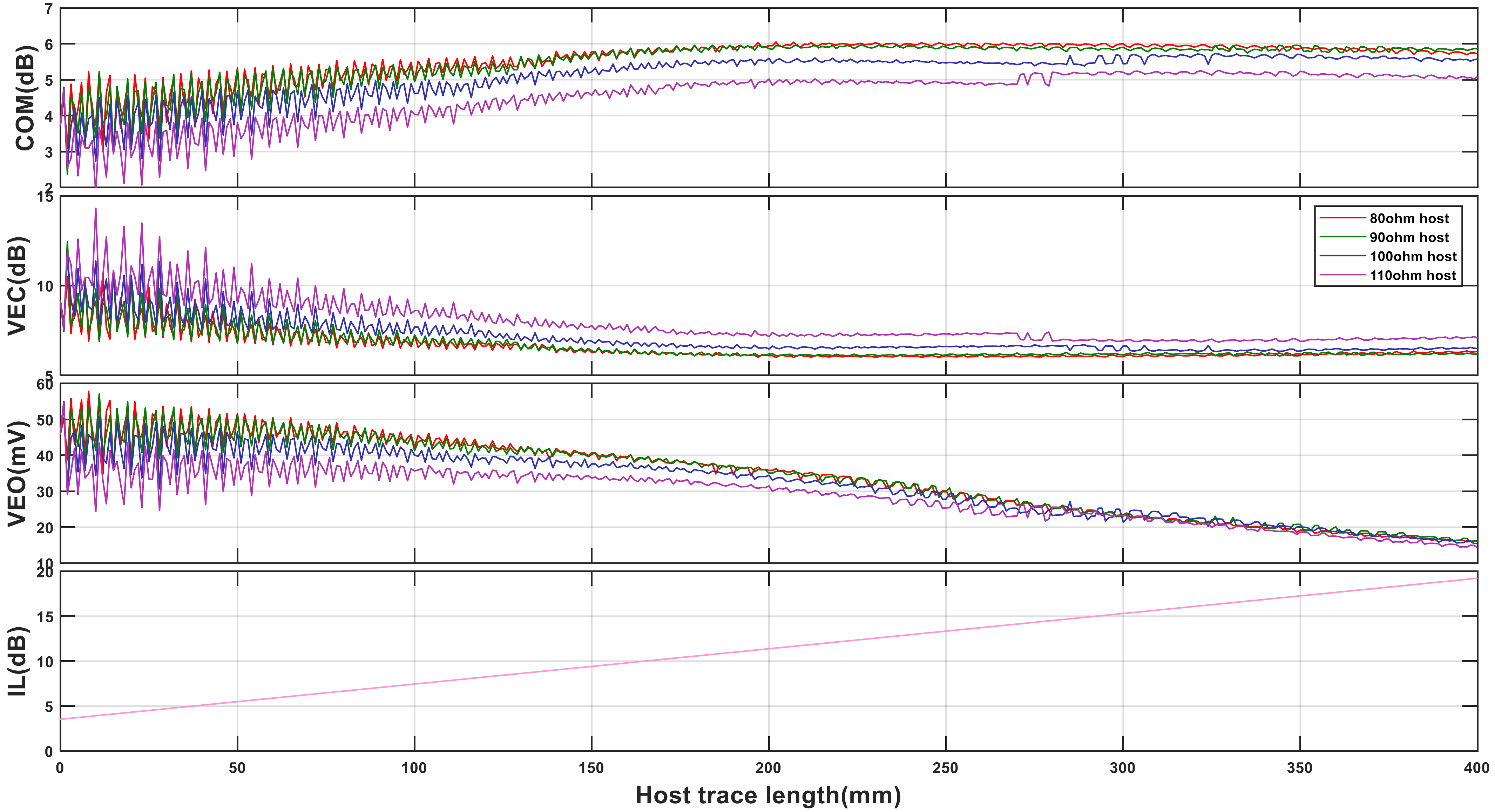


TP1a results by TxSNR

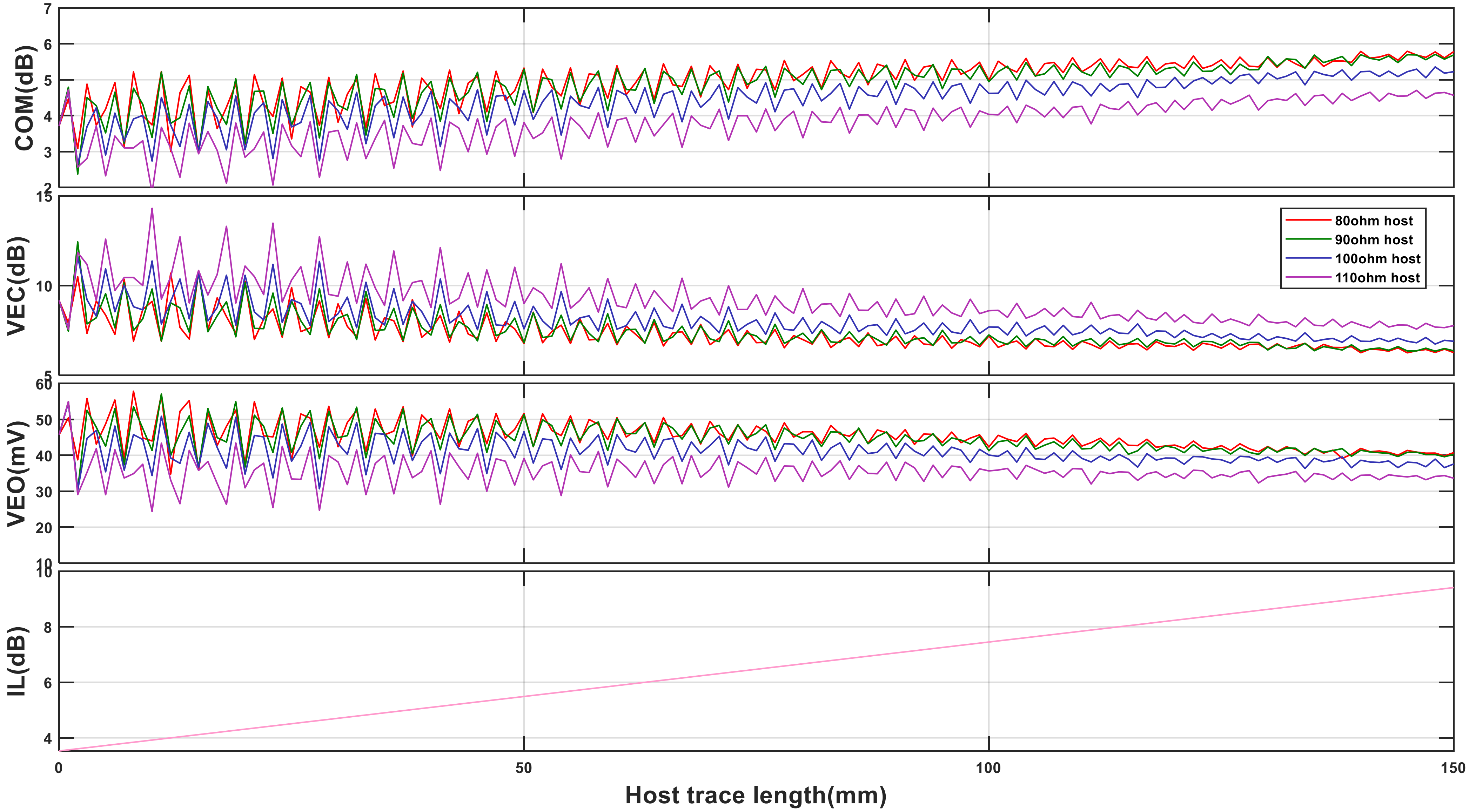


Effect of host trace impedance on TP1a performance

TP1a results by host impedance

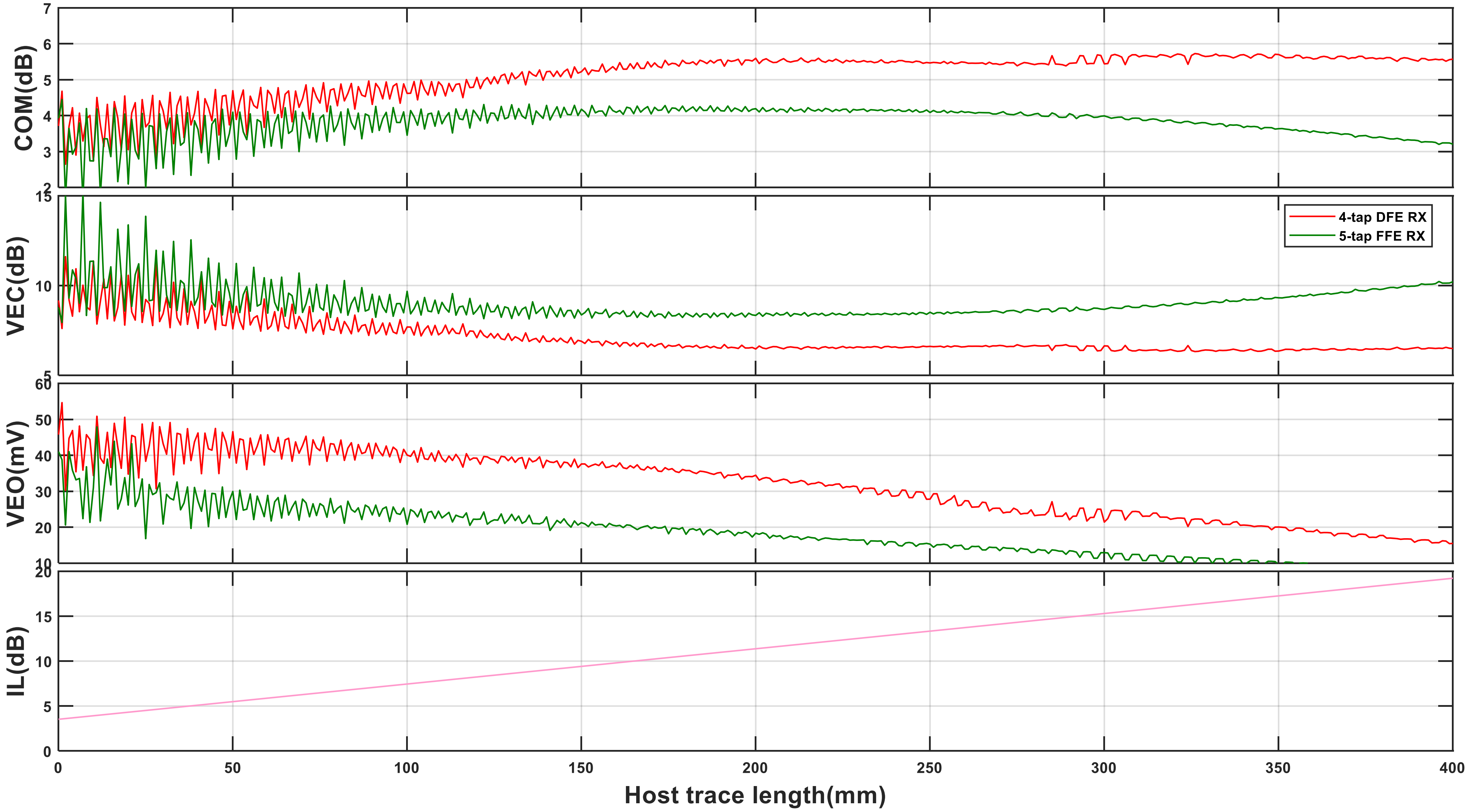


TP1a results by host impedance

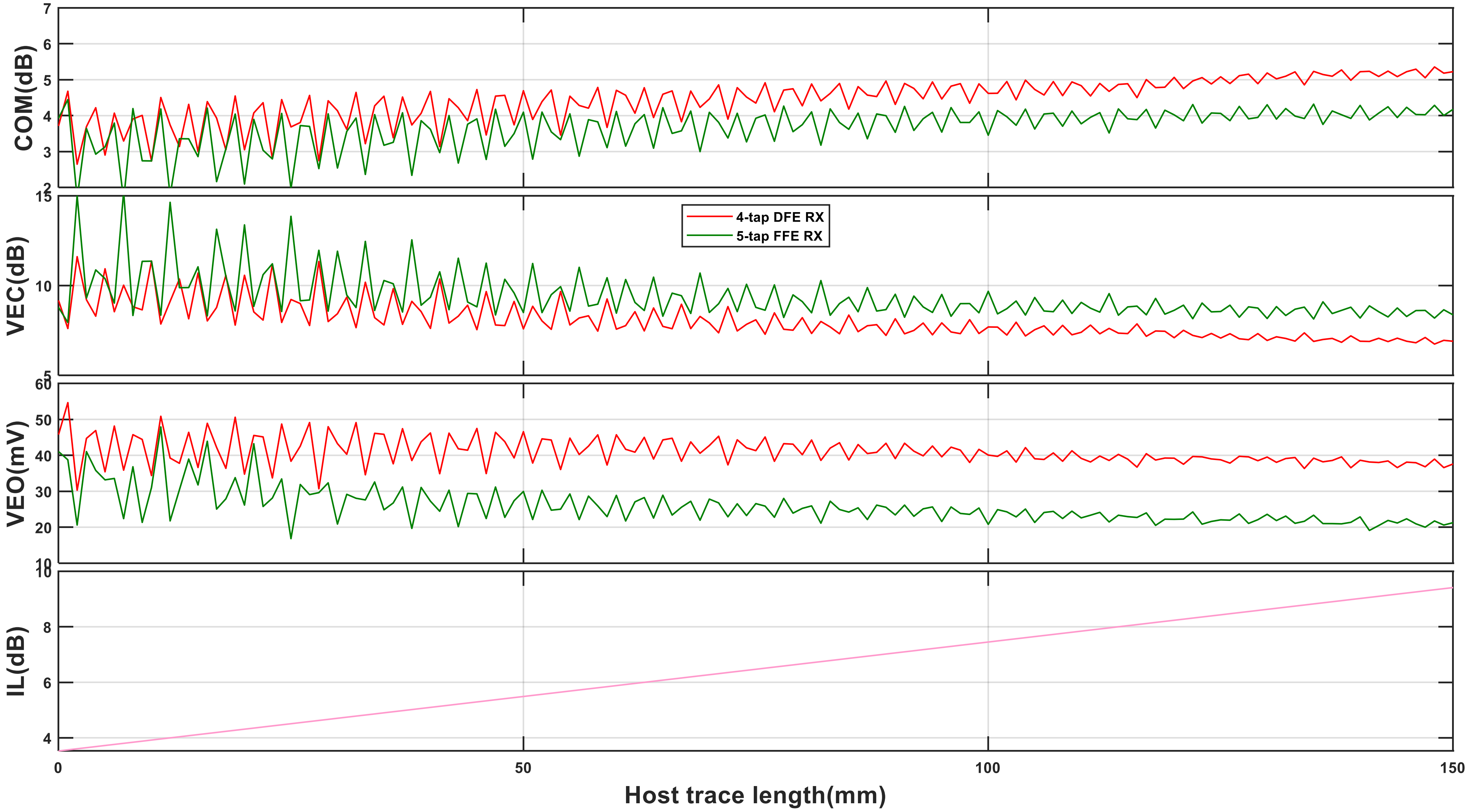


Effect of equalization

TP1a results by equalization



TP1a results by equalization

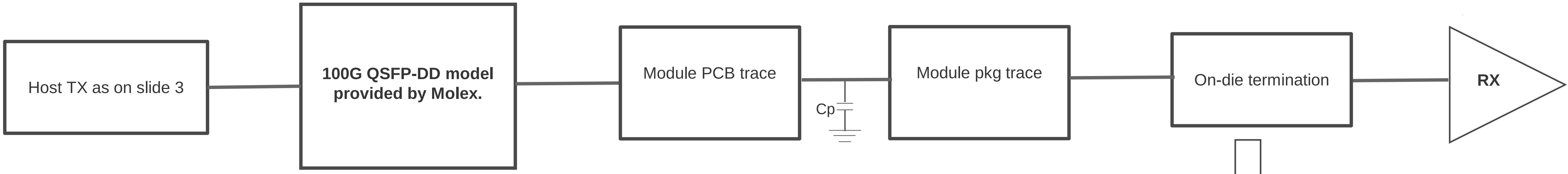


Conclusions and comments on TP1a performance.

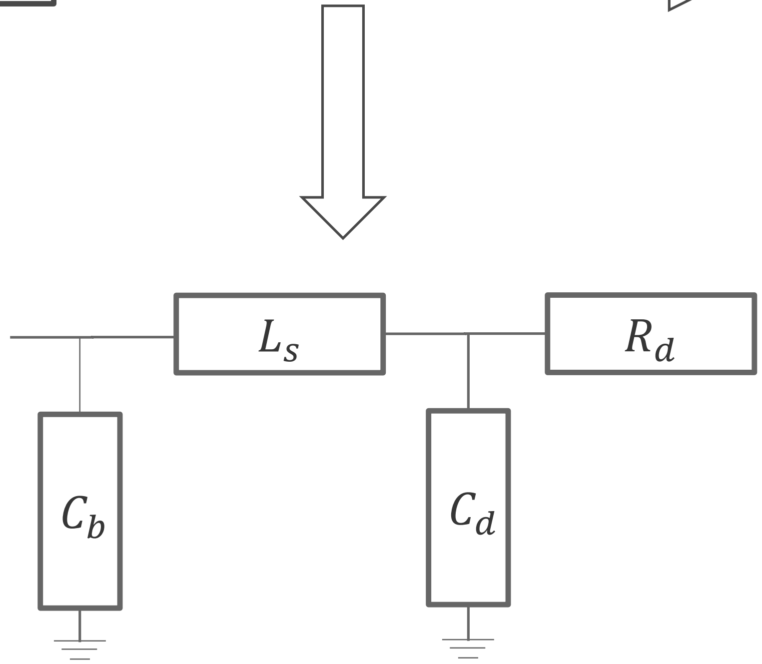
- The results of using the inductor model for the host ASIC have improved some of the results compared to just the capacitor model but it hasn’t affected the qualitative effects.
  - Decreasing the Tx SNR below 33dB significantly degrades the results
  - The host trace impedance at 110 Ohm significantly degrades the results
- Using the 5 tap FFE instead of the 4 tap DFE as a reference equalizer significantly degrades the performance with the die model that includes the inductor to represent a T-coil.

Investigation of the effect of package trace length and module die model on end to end COM.

Chip to module block diagram for end to end performance

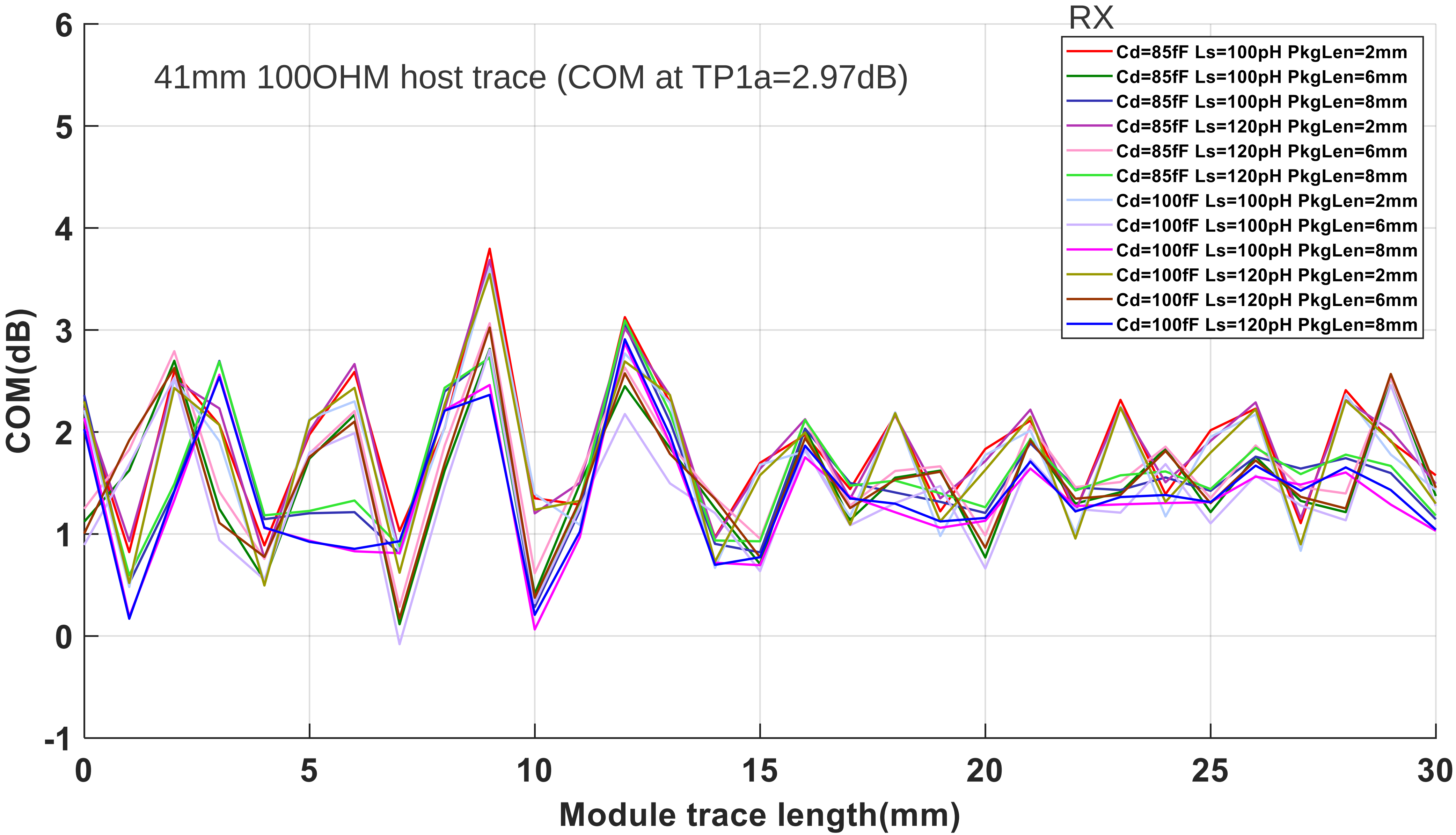


- RX termination Rd: 50ohm
- Module Package trace length: 2,6,8mm
- Module die model Ls=100pH, 120pH Cd=85fF, 120fF Cb=30fF
- Cp=87fF
- Module trace 92.5 Ohm
- Sweep module trace length. Trace impedance: 92.5OHM
- Crosstalk is not included.
- Lane 3 of the connector is used
- Eta0=8.2e-9 and TxSNR= 33dB
- For the initial simulations looking at the connector model the TxFIR was allowed to optimize for all conditions. For the later results while sweeping the host trace length the Tx FIR tap weights were held at the values that optimized the TP1a performance.
- Performance is simulated using COM 2.70
- The complete COM table is in the back-up

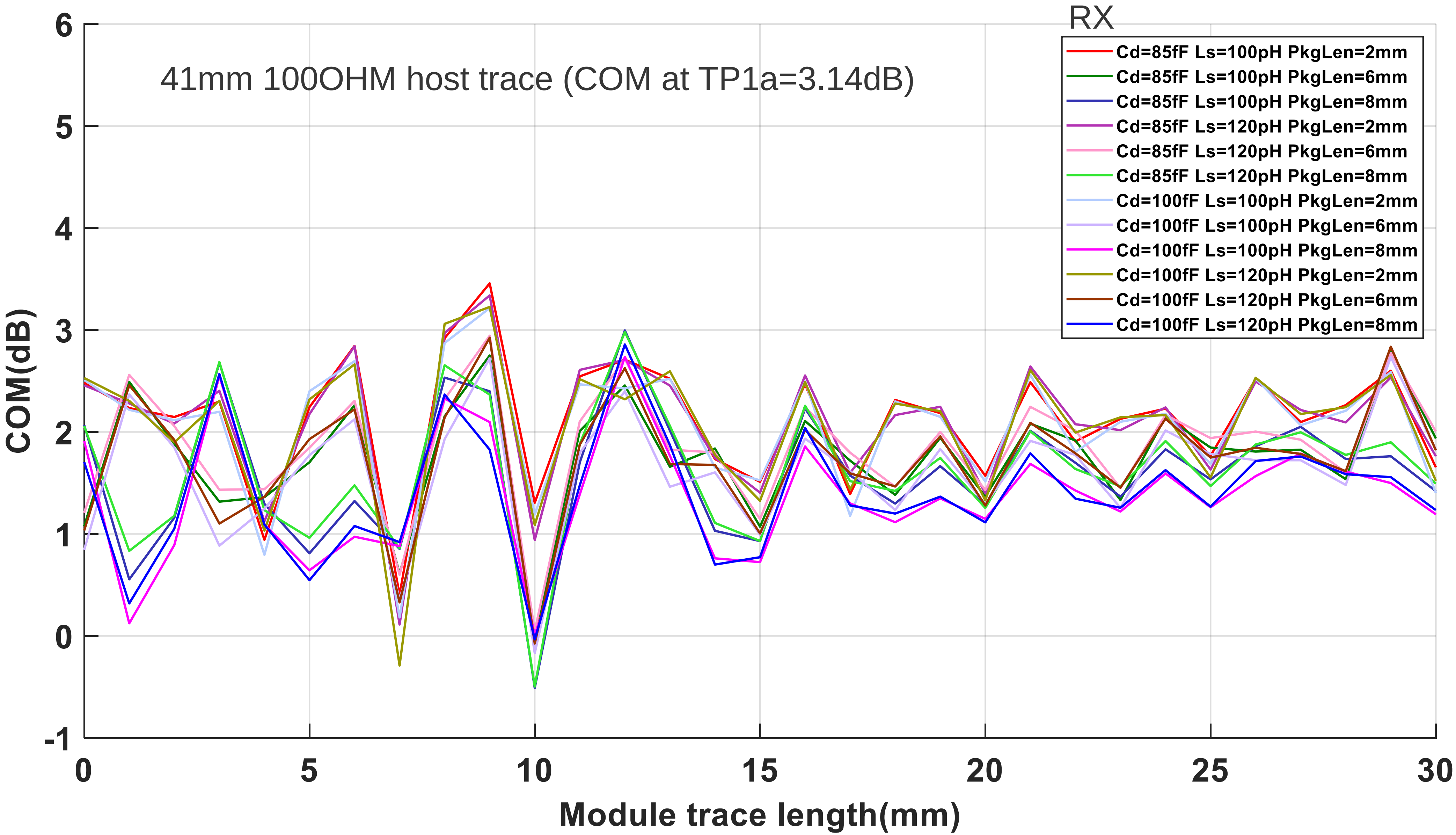


On-die inductor termination

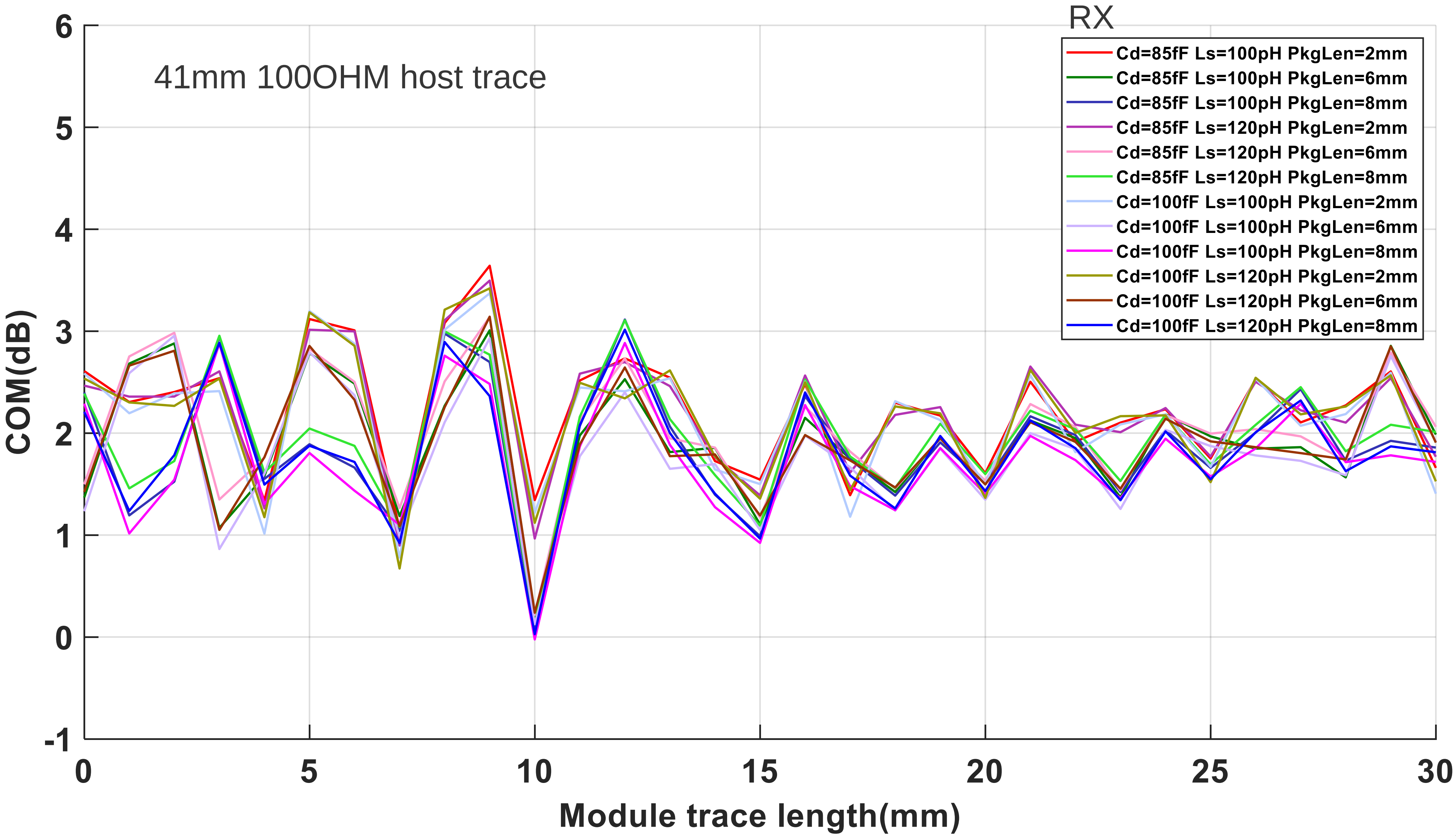
5-tap FFE end to end COM



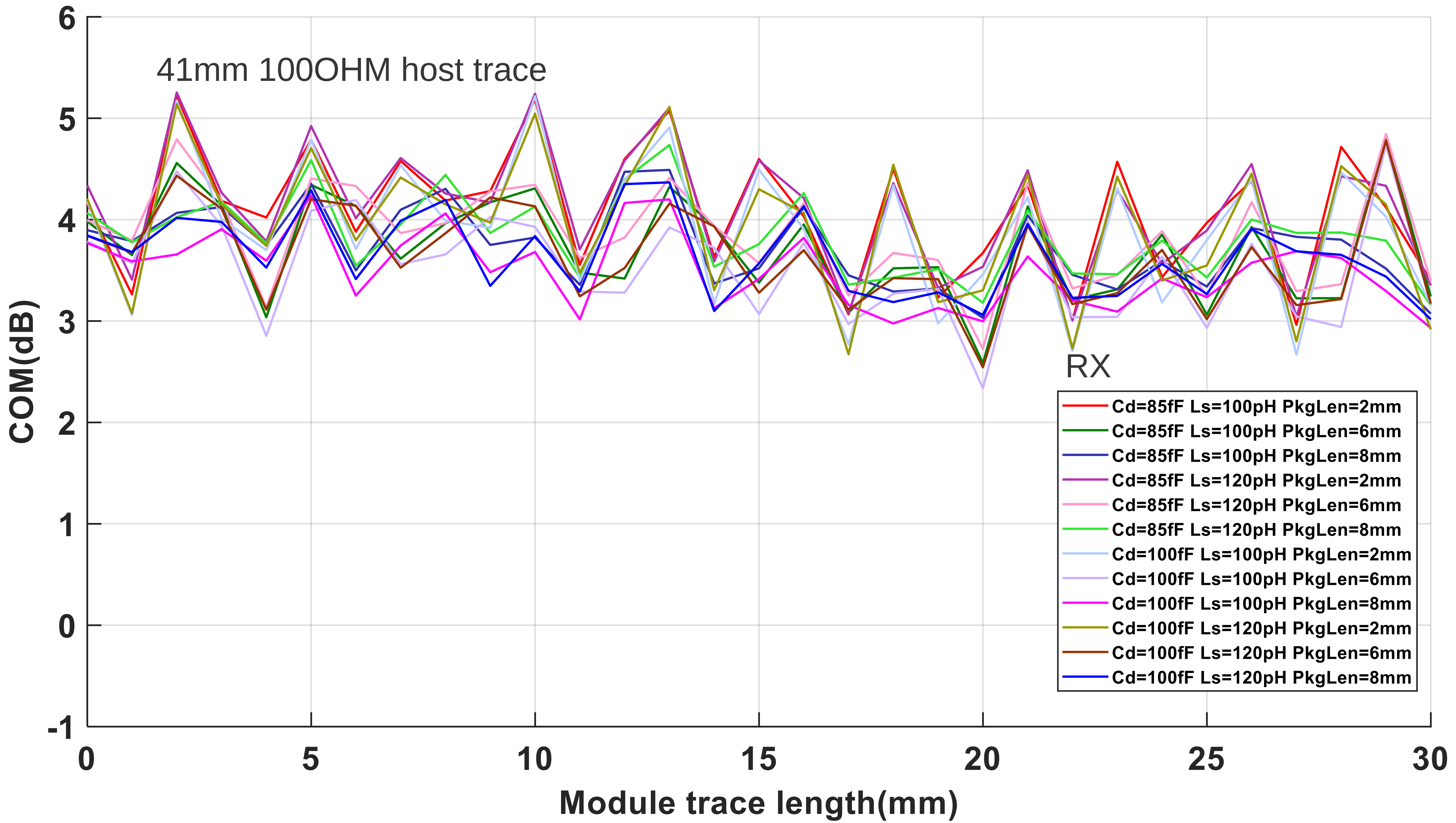
4-tap DFE end to end COM



7-tap DFE end to end COM



12-tap DFE end to end COM

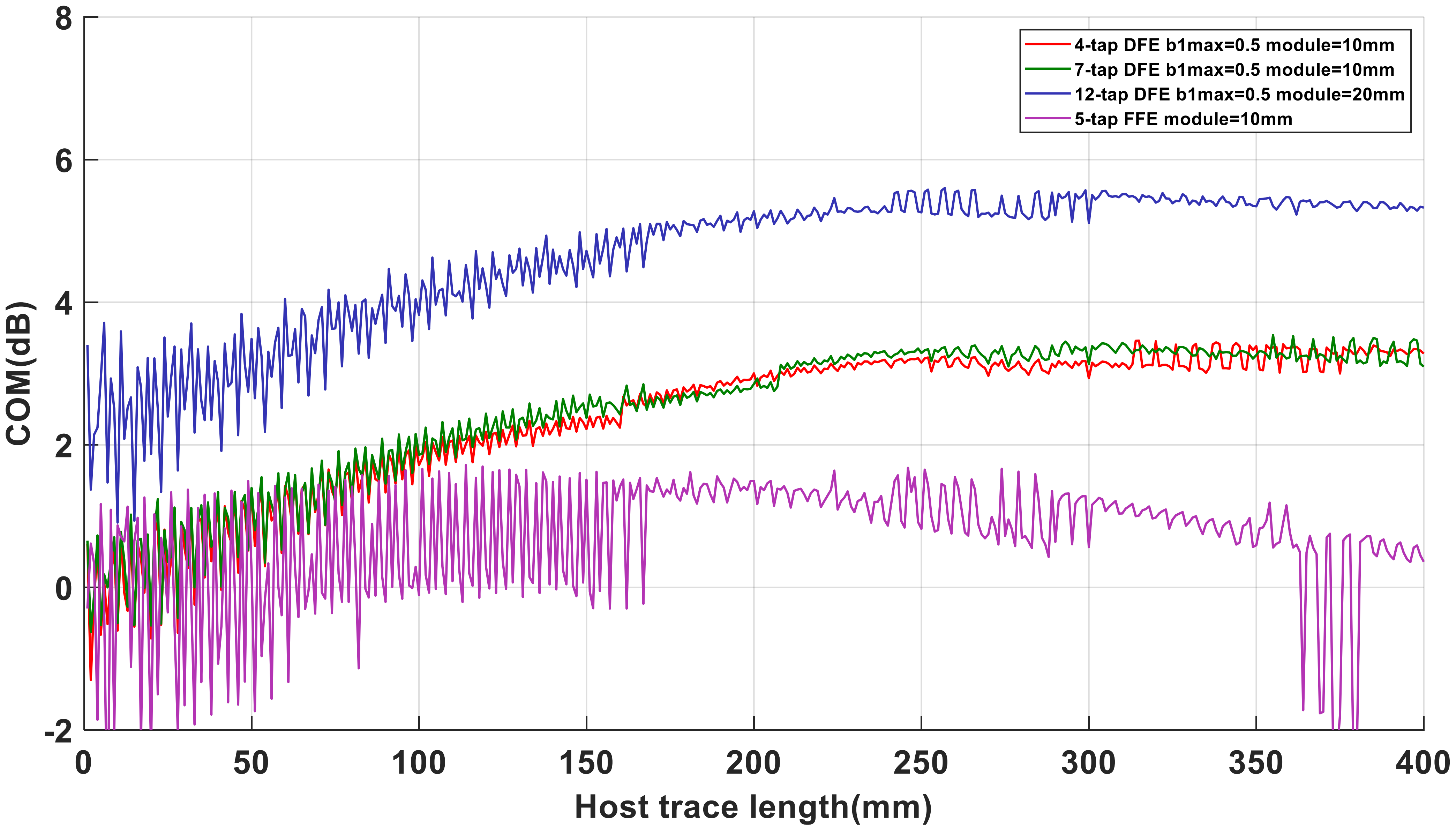


Conclusions and comments on module model.

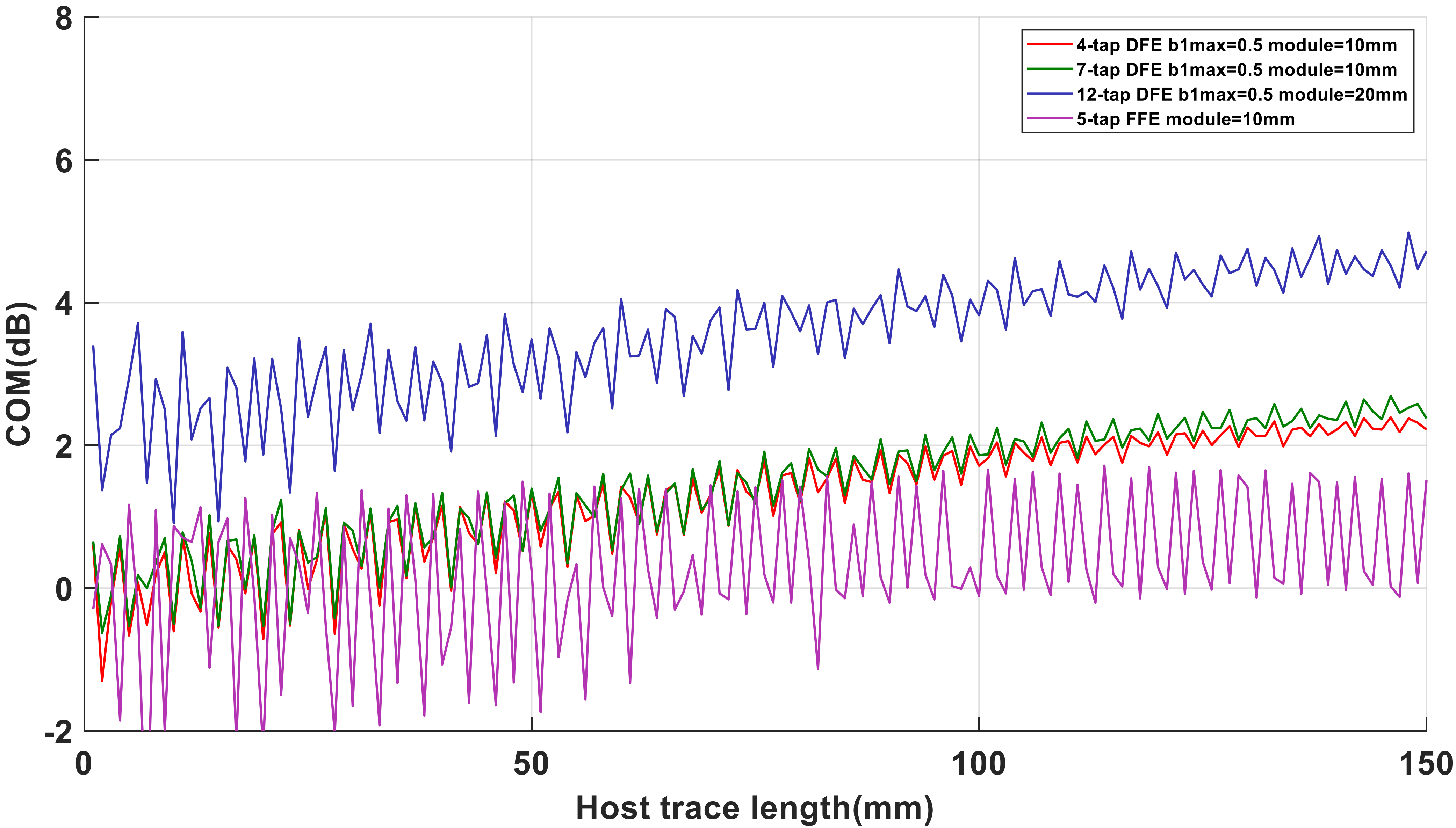
- The end to end COM performance is significantly worse than that at TP1a unless the 12 tap DFE is used.
- The 120pH inductor gave poorer performance than 100pH, whether the Cd value was 85fF or 100fF
- Cd value of 85fF gave somewhat better results but we felt it was rather optimistic.
- 8mm module trace gave significantly poorer results and we felt this was longer than likely to be in the module.
- Based on this a module package/die model of Ls=100pH, Cd=100fF, Cb=30fF and module package trace of 6mm was chosen for further simulation.

Investigation of Host trace length on end to end COM with different equalizers.

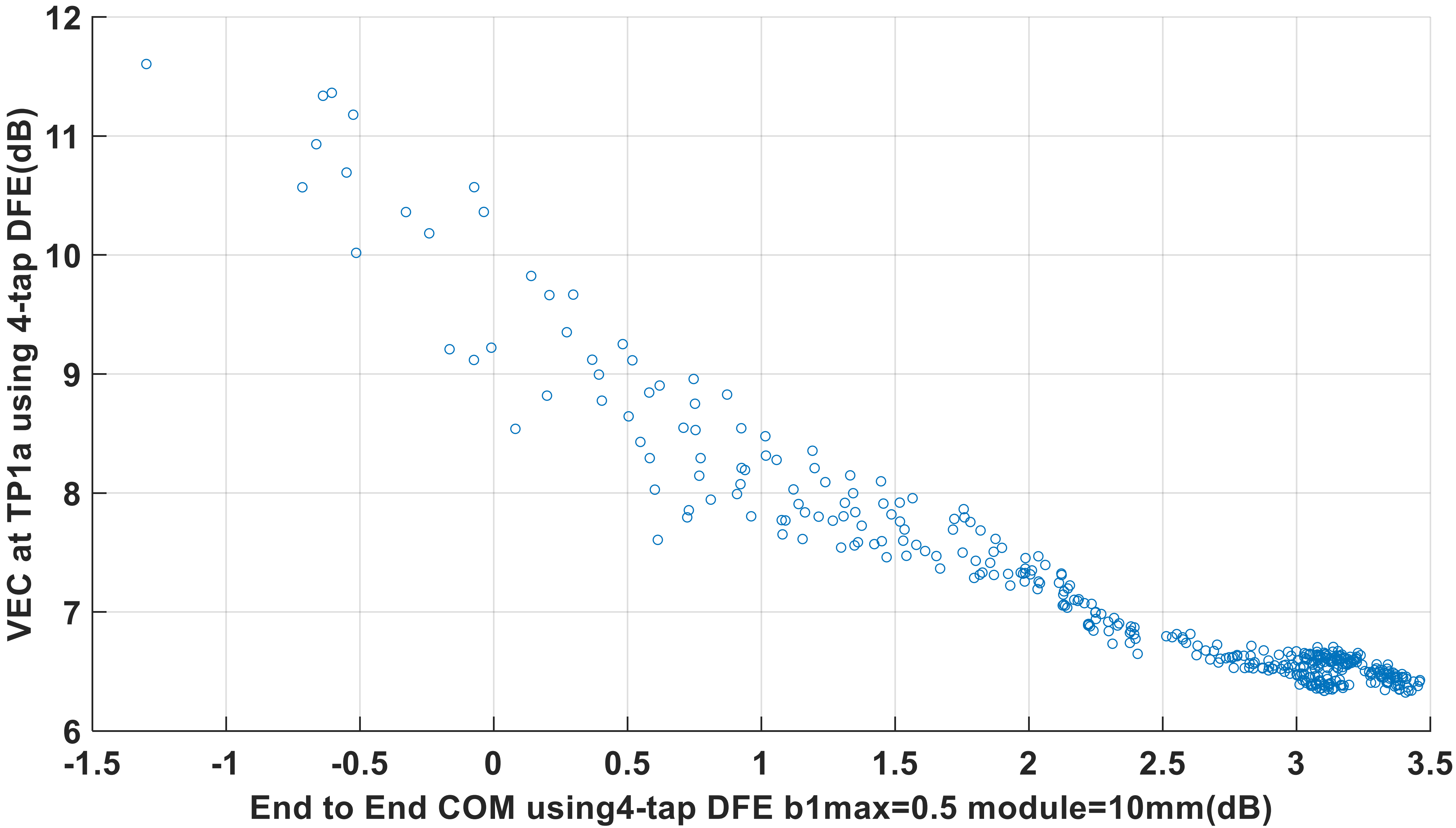
End to end COM



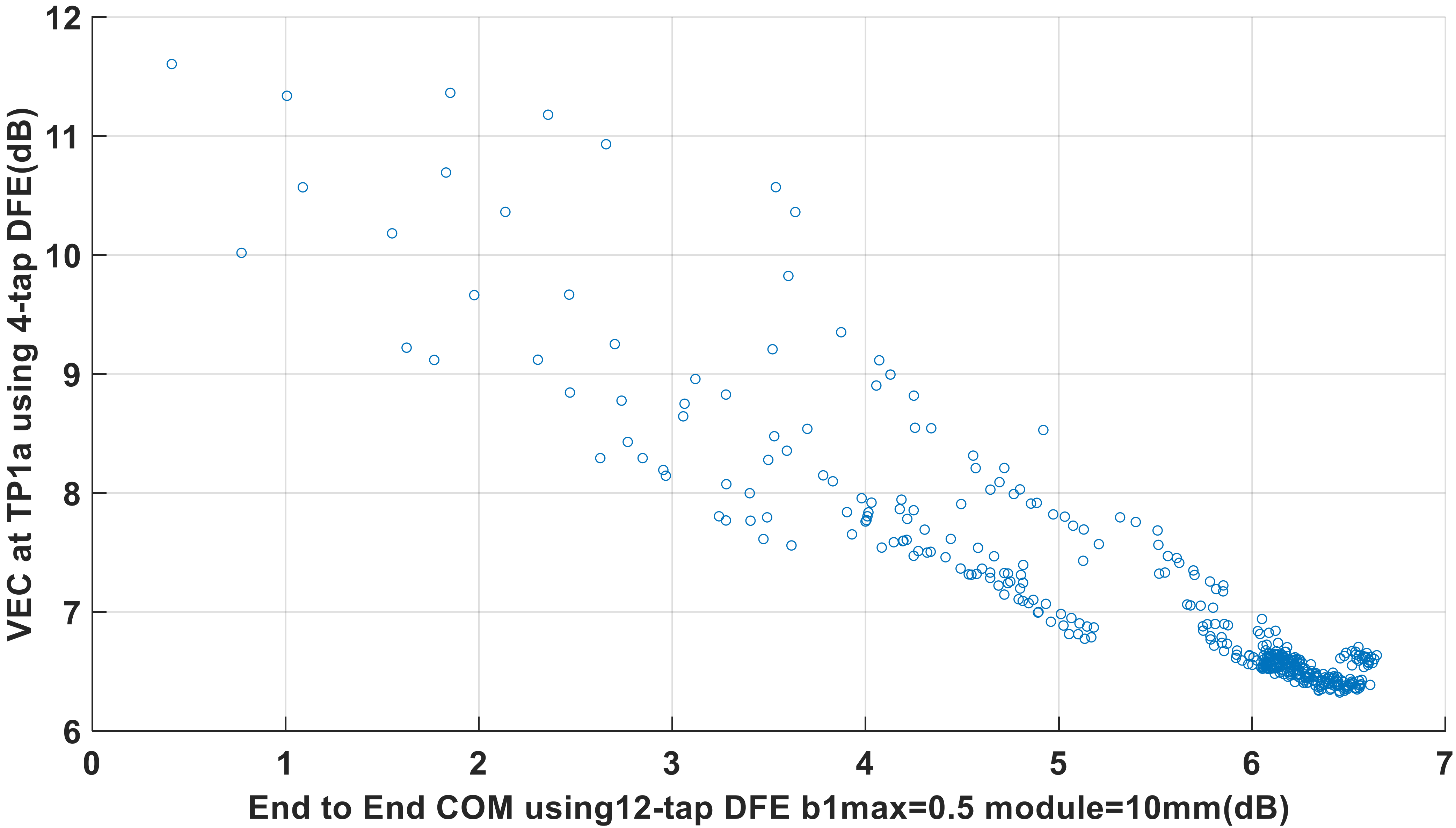
End to end COM



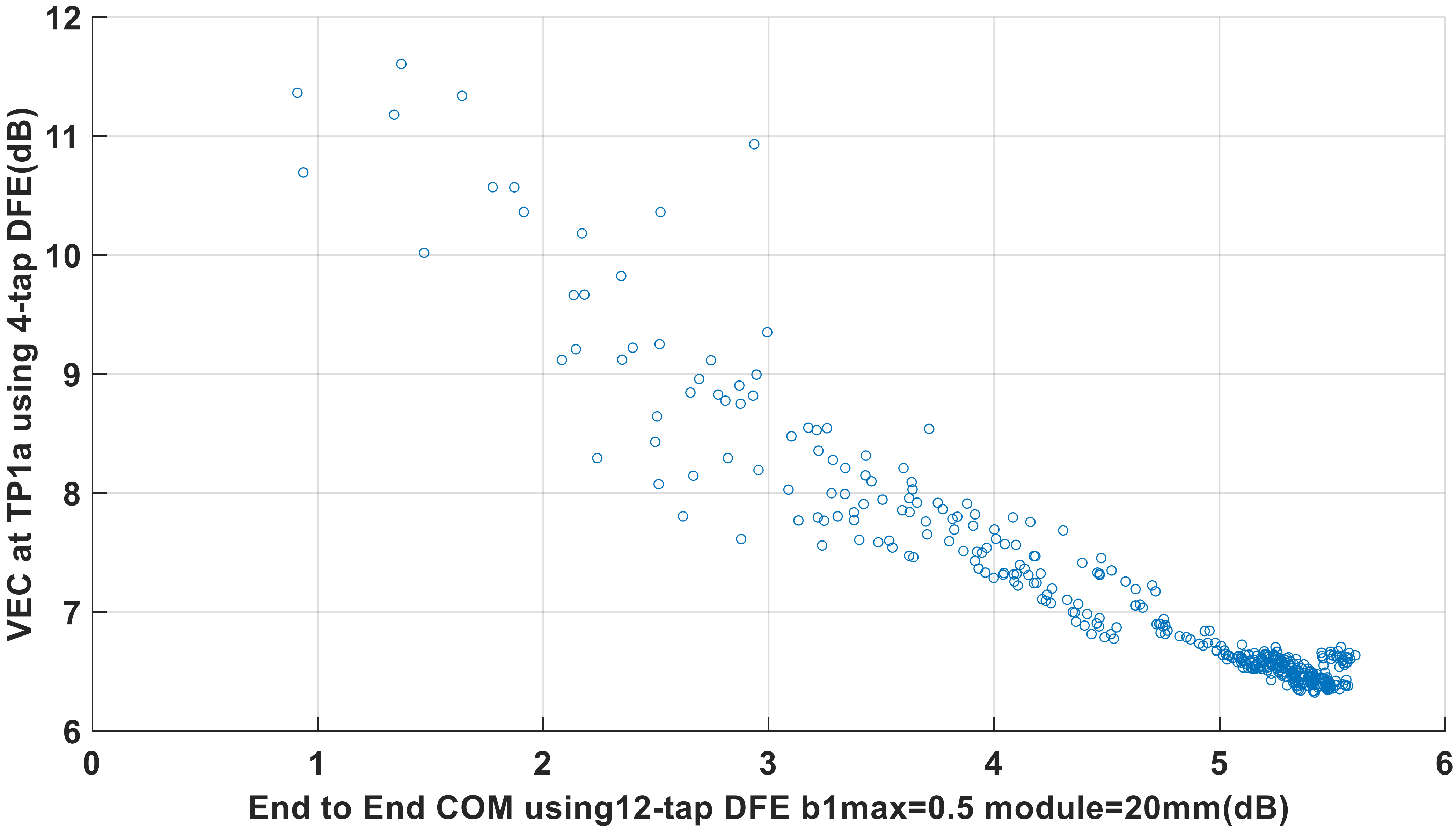
VEC at TP1a vs. End to End COM



VEC at TP1a vs. End to End COM



VEC at TP1a vs. End to End COM



Conclusions.

- With these module package and die models a stronger equalizer is needed in the module to provide adequate performance for the critical 50mm to 160mm host trace lengths where the host could also be used for the CR specification.
- With that stronger equalizer 3dB COM is achievable for the end to end performance provided the TP1a VEC with a 4tap DFE reference receiver is >= 7.5 dB . However that still doesn't enable the 50mm host trace length which needs a >=9dB VEC with that equalizer. With the >=9dB VEC spec at TP1a the end to end COM with the 12 tap DFE can be as bad as 2dB.
- Note that there are other impairments that have not been explored in this presentation. In particular the effect of vias in the host and module.

Back-up

TP1a COM spreadsheet

4-tap DFE

filter and Eq		
f_r	0.75	*fb
c(0)	0.6	
c(-1)	[-0.3:0.02:0]	
c(-2)	[0:.02:0.1]	
c(1)	[-0.1:0.05:0]	
N_b	4	UI
b_max(1)	0.5	
b_max(2..N_b)	0.2	
g_DC	[-14:1:-3]	dB
f_z	12.58	GHz
f_p1	20	GHz
f_p2	28	GHz
g_DC_HP	[-3:1:0]	
f_HP_PZ	1.328125	GHz
ffe_pre_tap_len	0	UI
ffe_post_tap_len	0	UI
Include PCB	1	logical
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.125	
ffe_backoff	0	

Table 93A-1 parameters		
Parameter	**Setting**	**Units**
f_b	53.125	GBd
f_min	0.05	GHz
Delta_f	0.01	GHz
C_d	[1.2e-4 0]	nF
L_s	[0.12, 0]	nH
C_b	[0.3e-4 0]	nF
z_p select	[1]	
z_p (TX)	[11.5 11.5; 1.8 1.8]	mm
z_p (NEXT)	[0 0; 0 0]	mm
z_p (FEXT)	[11.5 11.5; 1.8 1.8]	mm
z_p (RX)	[0 0; 0 0]	mm
C_p	[0.87e-4 0]	nF
R_0	50	Ohm
R_d	[50 50]	Ohm
A_v	0.415	V
A_fe	0.415	V
A_ne	0.6	V
L	4	
M	32	

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	[100 100]	Ohm

COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical

- HCB trace: 100ohm 63.8mm (2.5dB loss)

End to end COM spreadsheet

4/7/12-tap DFE

filter and Eq		
f_r	0.75	*fb
c(0)	0.6	
c(-1)	[-0.3:0.02:0]	
c(-2)	[0:.02:0.1]	
c(1)	[-0.1:0.05:0]	
N_b	4	UI
b_max(1)	0.5	
b_max(2..N_b)	0.2	
g_DC	[-14:1:-3]	dB
f_z	12.58	GHz
f_p1	20	GHz
f_p2	28	GHz
g_DC_HP	[-3:1:0]	
f_HP_PZ	1.328125	GHz
ffe_pre_tap_len	0	UI
ffe_post_tap_len	0	UI
Include PCB	1	logical
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.125	
ffe_backoff	0	

5-tap FFE

filter and Eq		
f_r	0.75	*fb
c(0)	0.6	
c(-1)	[-0.3:0.02:0]	
c(-2)	[0:.02:0.1]	
c(1)	[-0.1:0.05:0]	
N_b	0	UI
b_max(1)	0	
b_max(2..N_b)	0	
g_DC	[-14:1:-3]	dB
f_z	18.88	GHz
f_p1	28	GHz
f_p2	53.125	GHz
g_DC_HP	[-3:1:0]	
f_HP_PZ	0.00025	GHz
ffe_pre_tap_len	0	UI
ffe_post_tap_len	4	UI
Include PCB	1	logical
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.125	
ffe_backoff	0	

Table 93A-1 parameters

Parameter	Setting	Units
f_b	53.125	GBd
f_min	0.05	GHz
Delta_f	0.01	GHz
C_d	[1.2e-4 1.0e-4]	nF
L_s	[0.12, 0.1]	nH
C_b	[0.3e-4 0.3e-4]	nF
z_p select	[1]	
z_p (TX)	[11.5 11.5; 1.8 1.8]	mm
z_p (NEXT)	[0 0; 0 0]	mm
z_p (FEXT)	[11.5 11.5; 1.8 1.8]	mm
z_p (RX)	[2 2; 0 0]	mm
C_p	[0.87e-4 0.87e-4]	nF
R_0	50	Ohm
R_d	[50 50]	Ohm
A_v	0.415	V
A_fe	0.415	V
A_ne	0.6	V
L	4	
M	32	

Noise, jitter

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters

Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 92.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters

Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	[100 92.5]	Ohm

COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical

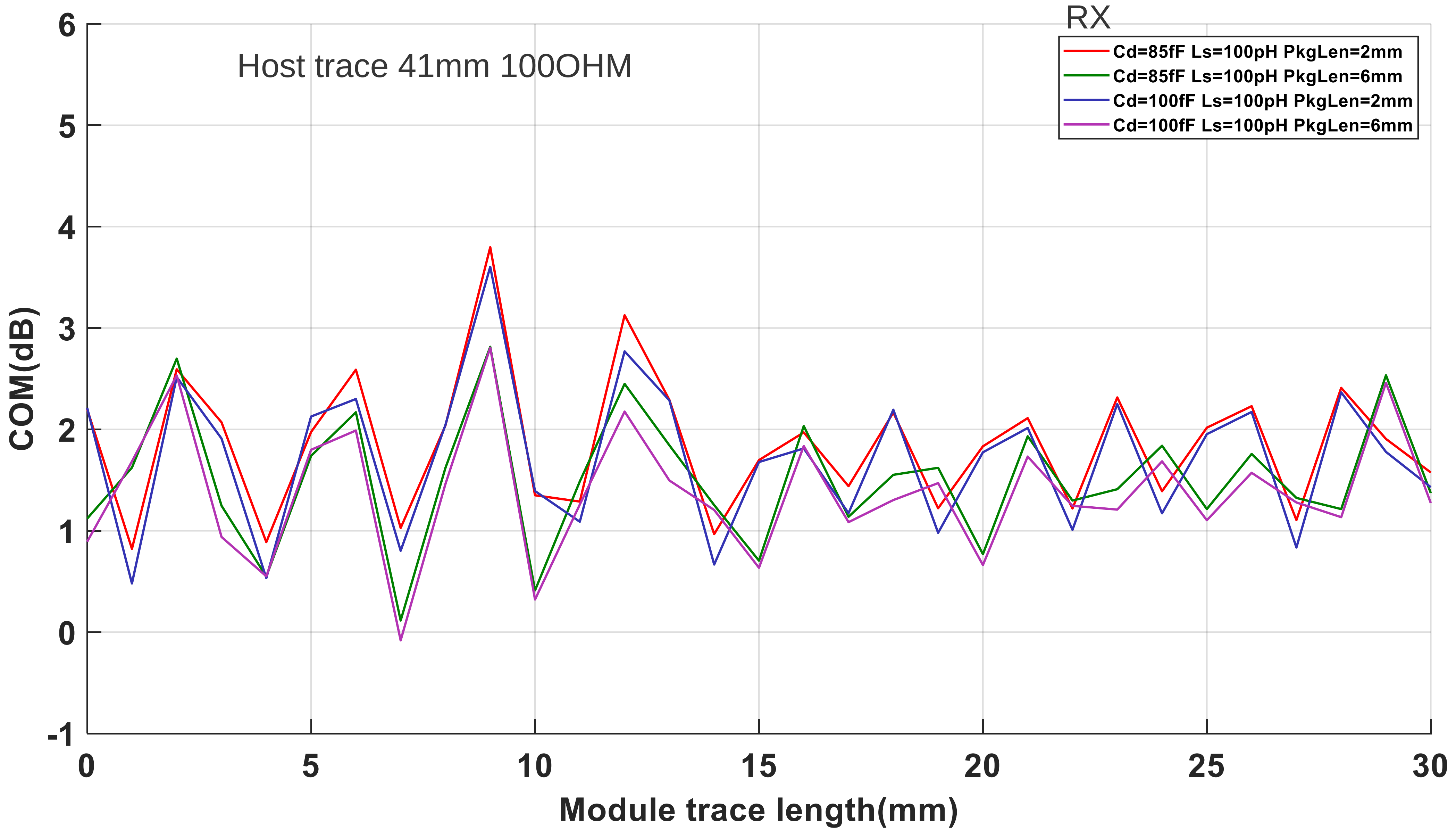
Rx

Cd: 85fF, 100fF

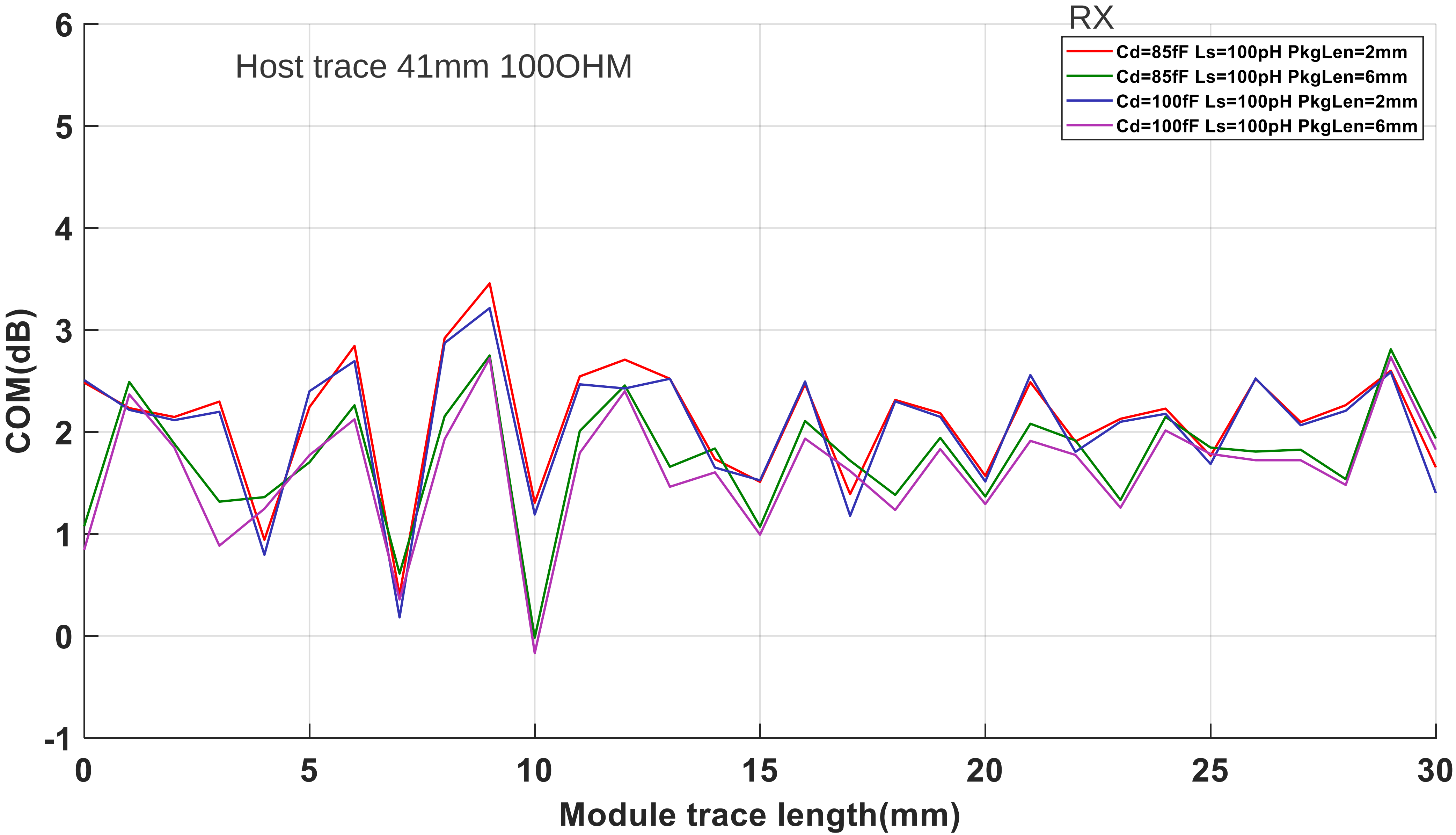
Ls: 100pH, 120pH

Pkg: no pth, [2,6,8]mm, 92.5OHM

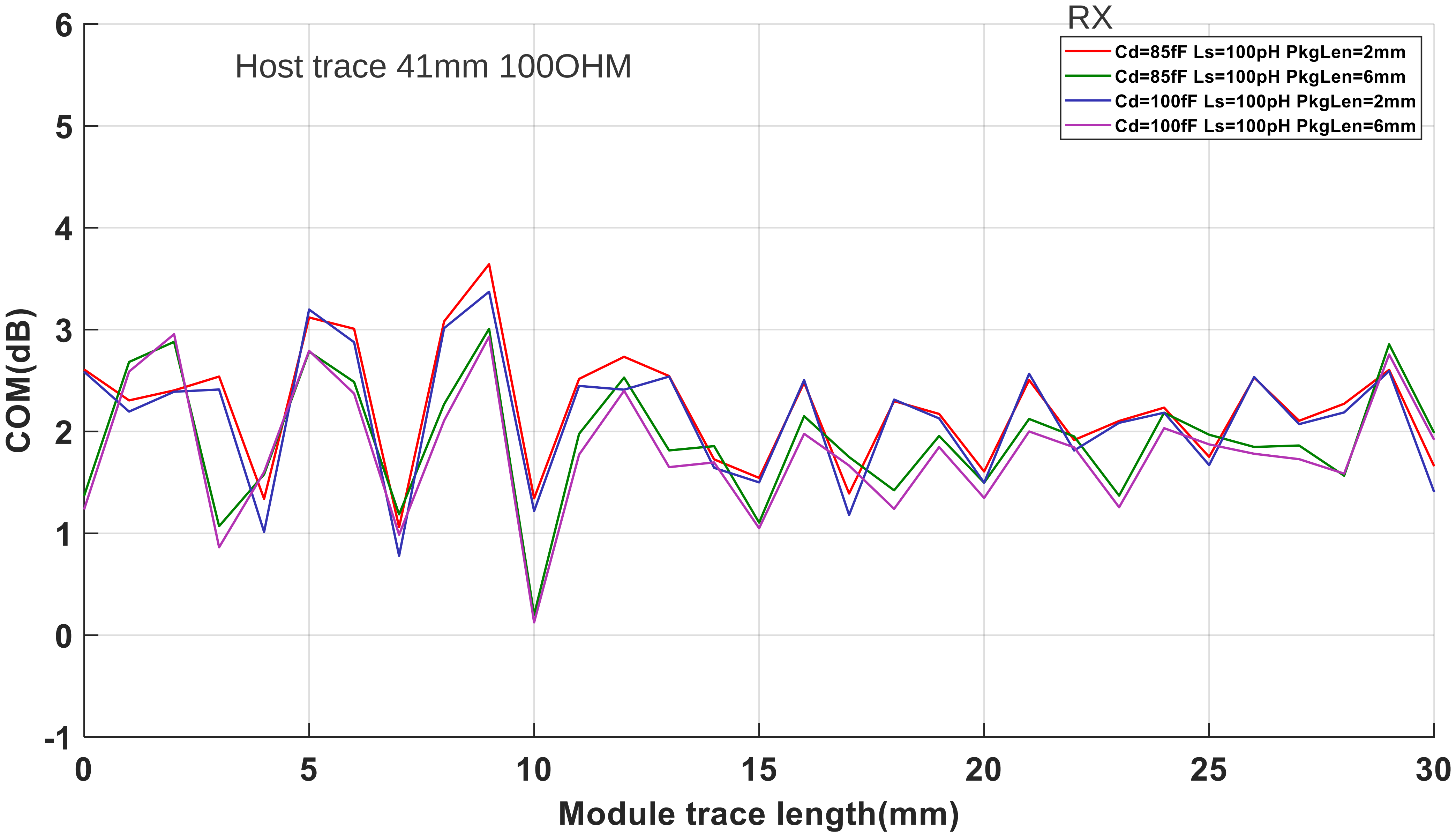
5-tap FFE end to end COM



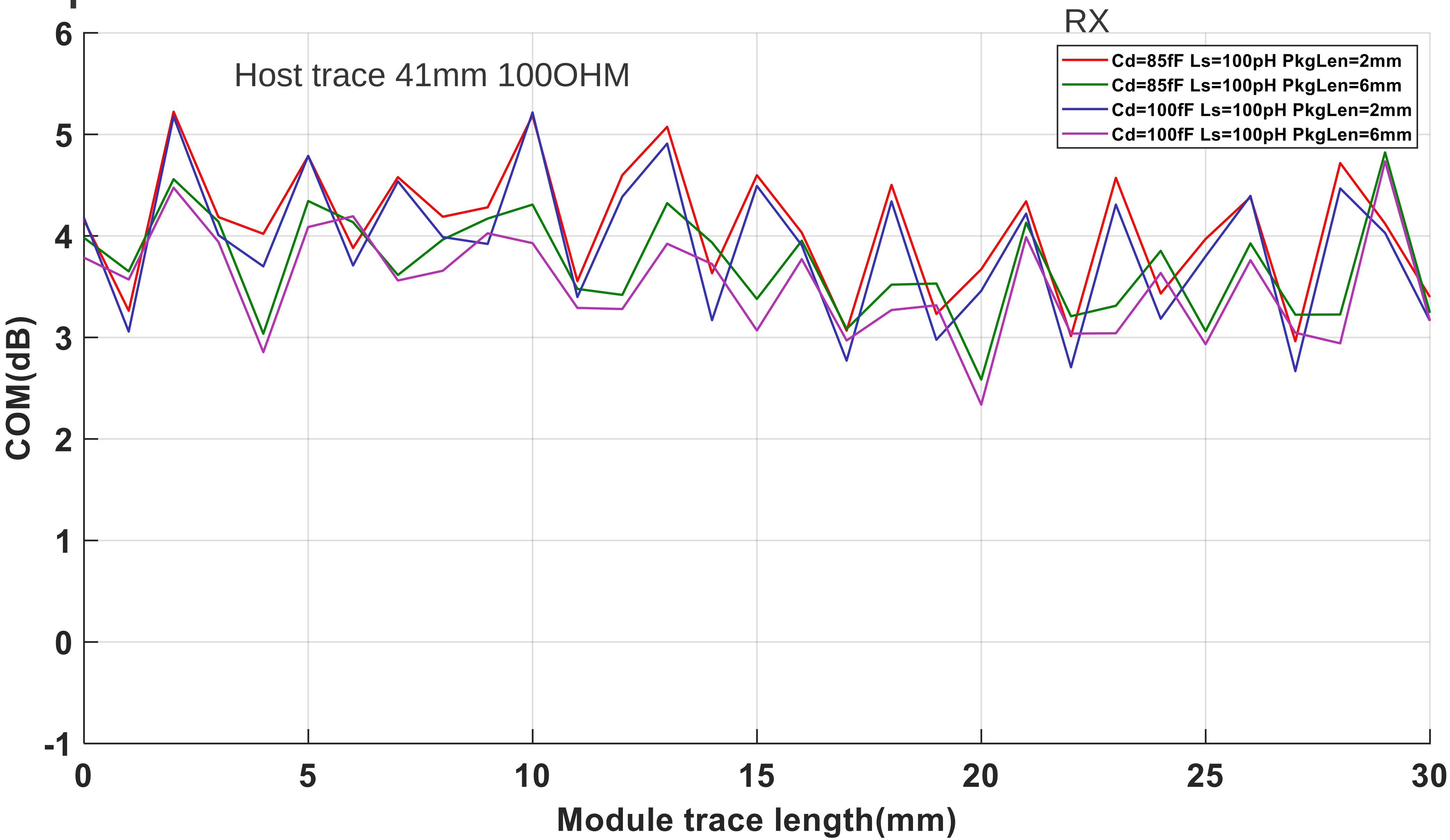
4-tap DFE end to end COM



7-tap DFE end to end COM



12-tap DFE end to end COM



End to end COM spreadsheet

The end to end COM is calculated with the Tx FIR tap weights locked to the optimized values from the previous TP1a simulations.

4/7/12-tap DFE

filter and Eq		
f_r	0.75	*fb
c(0)	0.6	
c(-1)	[-0.3:0.02:0]	
c(-2)	[0:.02:0.1]	
c(1)	[-0.1:0.05:0]	
N_b	4	UI
b_max(1)	0.5	
b_max(2..N_b)	0.2	
g_DC	[-14:1:-3]	dB
f_z	12.58	GHz
f_p1	20	GHz
f_p2	28	GHz
g_DC_HP	[-3:1:0]	
f_HP_PZ	1.328125	GHz
ffe_pre_tap_len	0	UI
ffe_post_tap_len	0	UI
Include PCB	1	logical
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.125	
ffe_backoff	0	

5-tap FFE

filter and Eq		
f_r	0.75	*fb
c(0)	0.6	
c(-1)	[-0.3:0.02:0]	
c(-2)	[0:.02:0.1]	
c(1)	[-0.1:0.05:0]	
N_b	0	UI
b_max(1)	0	
b_max(2..N_b)	0	
g_DC	[-14:1:-3]	dB
f_z	18.88	GHz
f_p1	28	GHz
f_p2	53.125	GHz
g_DC_HP	[-3:1:0]	
f_HP_PZ	0.00025	GHz
ffe_pre_tap_len	0	UI
ffe_post_tap_len	4	UI
Include PCB	1	logical
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.125	
ffe_backoff	0	

Table 93A-1 parameters

Parameter	Setting	Units
f_b	53.125	GBd
f_min	0.05	GHz
Delta_f	0.01	GHz
C_d	[1.2e-4 1.0e-4]	nF
L_s	[0.12, 0.1]	nH
C_b	[0.3e-4 0.3e-4]	nF
z_p select	[1]	
z_p (TX)	[11.5 11.5; 1.8 1.8]	mm
z_p (NEXT)	[0 0; 0 0]	mm
z_p (FEXT)	[11.5 11.5; 1.8 1.8]	mm
z_p (RX)	[2 2; 0 0]	mm
C_p	[0.87e-4 0.87e-4]	nF
R_0	50	Ohm
R_d	[50 50]	Ohm
A_v	0.415	V
A_fe	0.415	V
A_ne	0.6	V
L	4	
M	32	

Rx

Cd: 100fF

Ls: 100pH

Pkg: no PTH, 6mm, 92.5OHM

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters

Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 92.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters

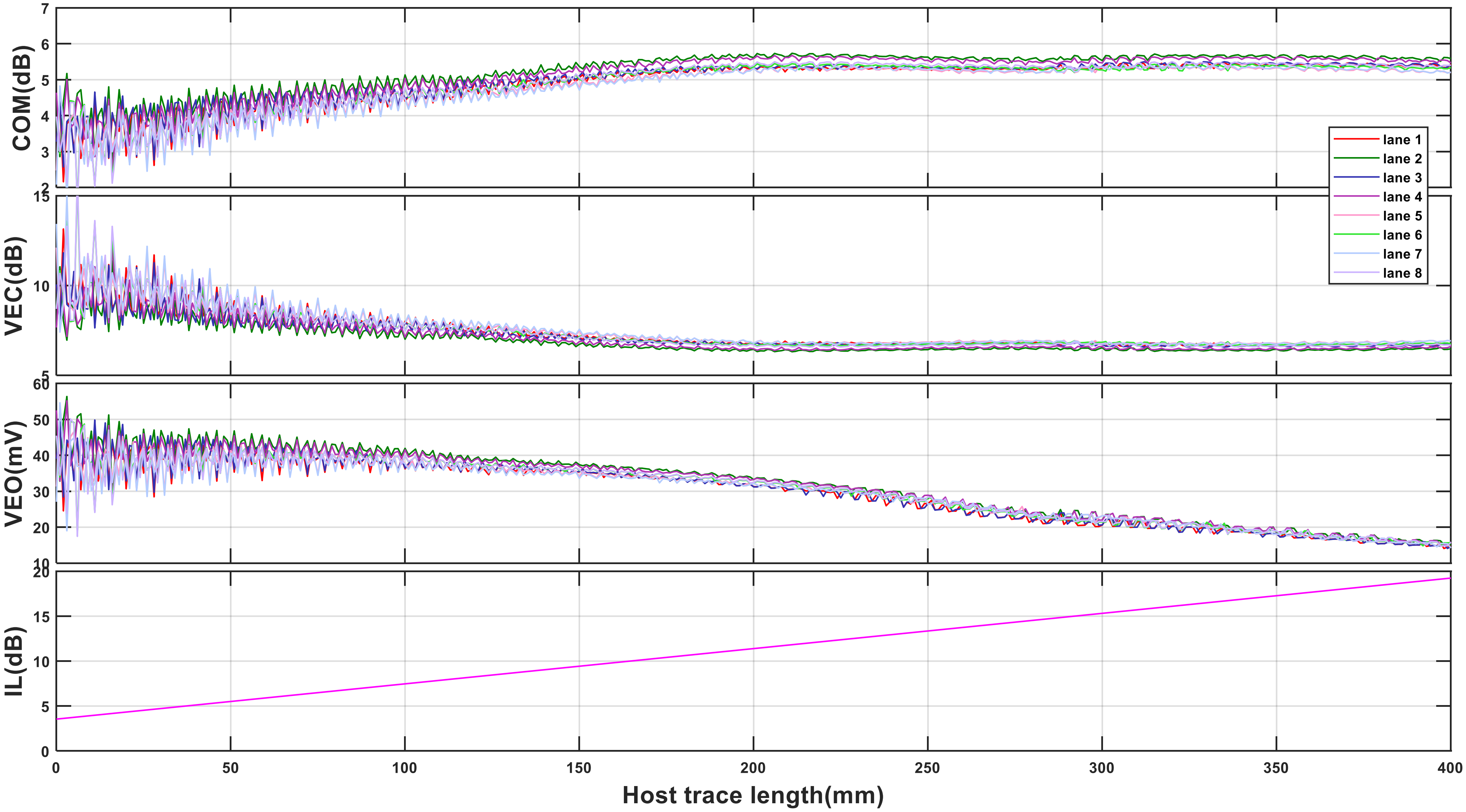
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	[100 92.5]	Ohm

COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical

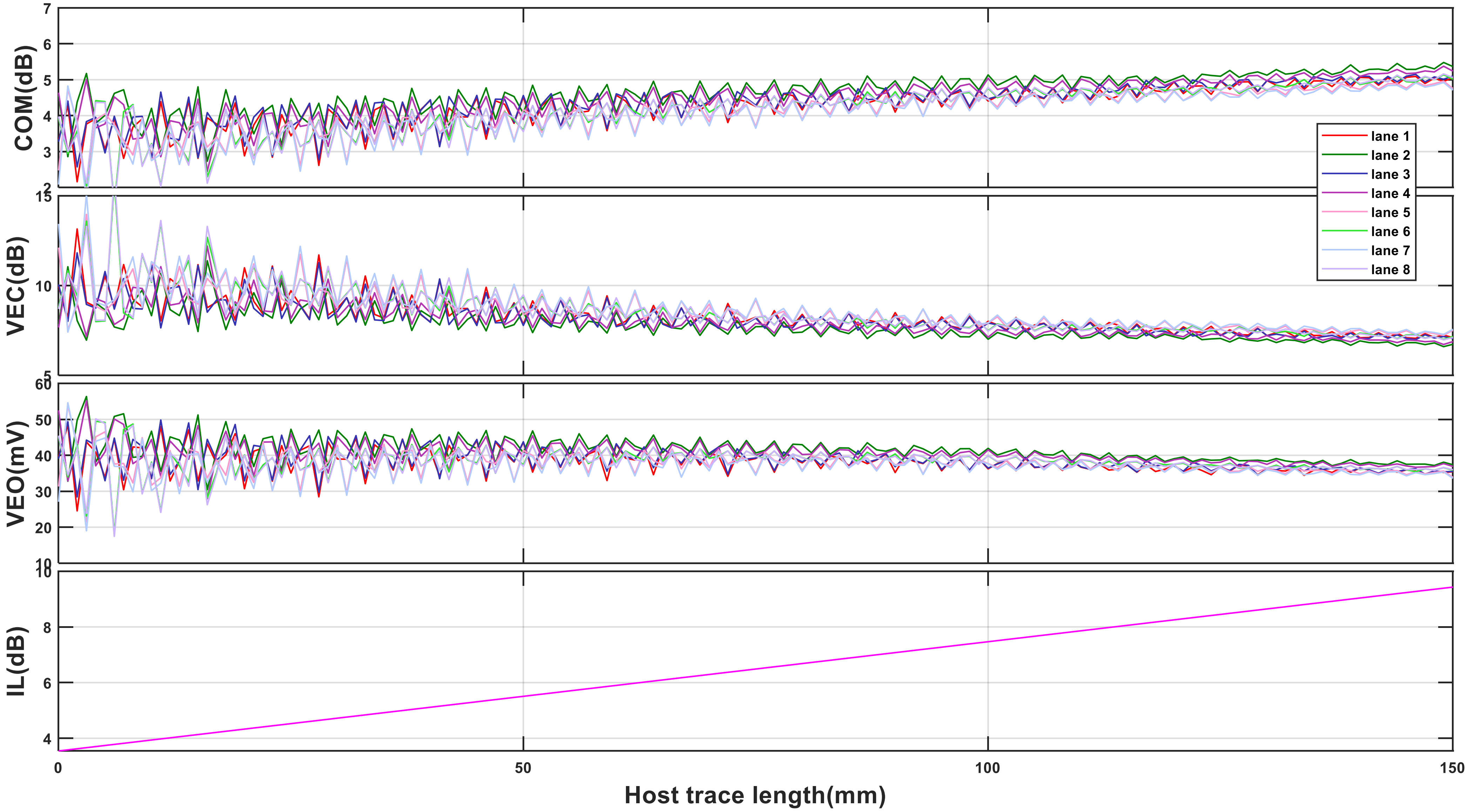
Back-up. Selected slides from Dudek_3ck_o1_0719

Effect of channel length, and connector lane, Capacitor Die model

Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host

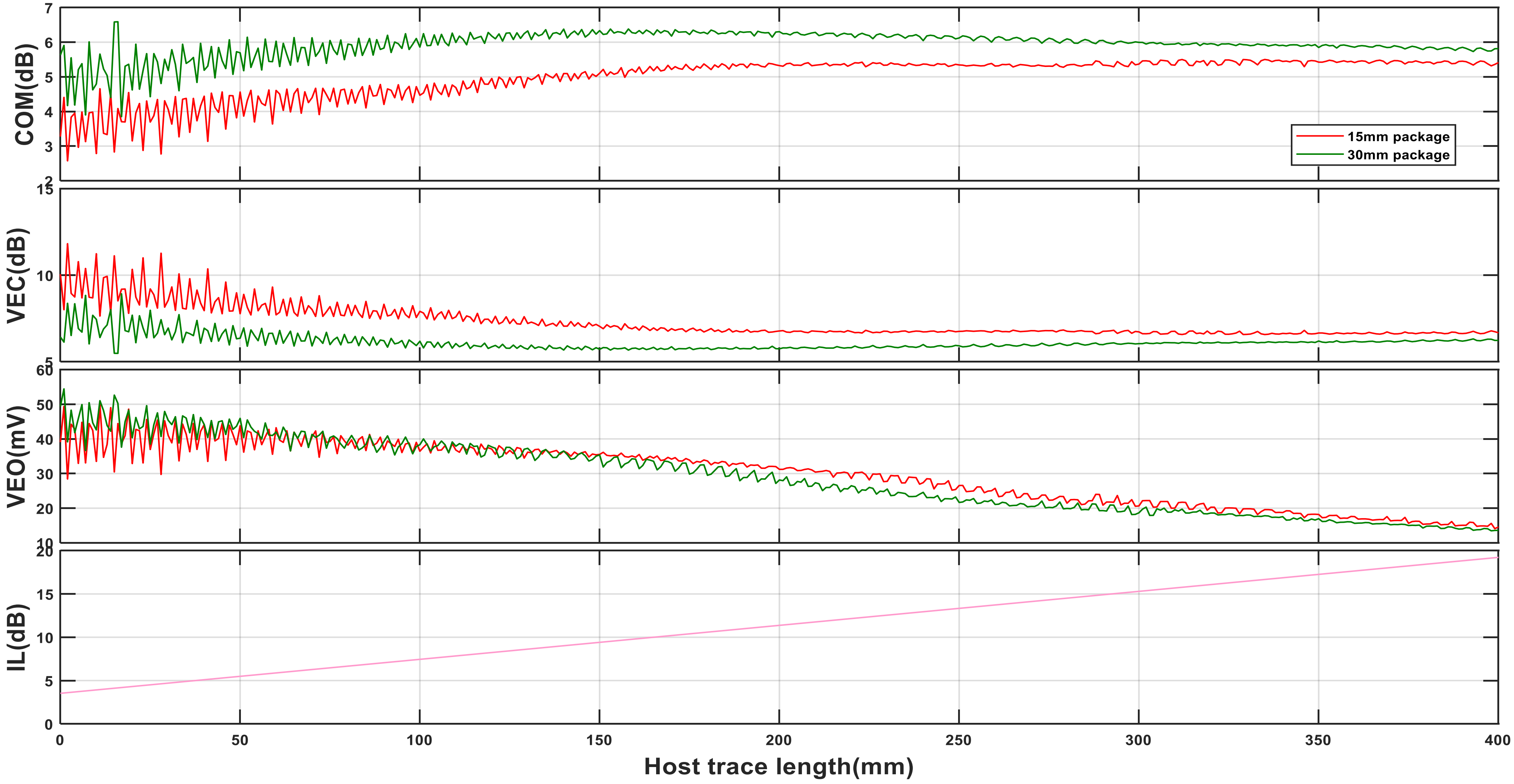


Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



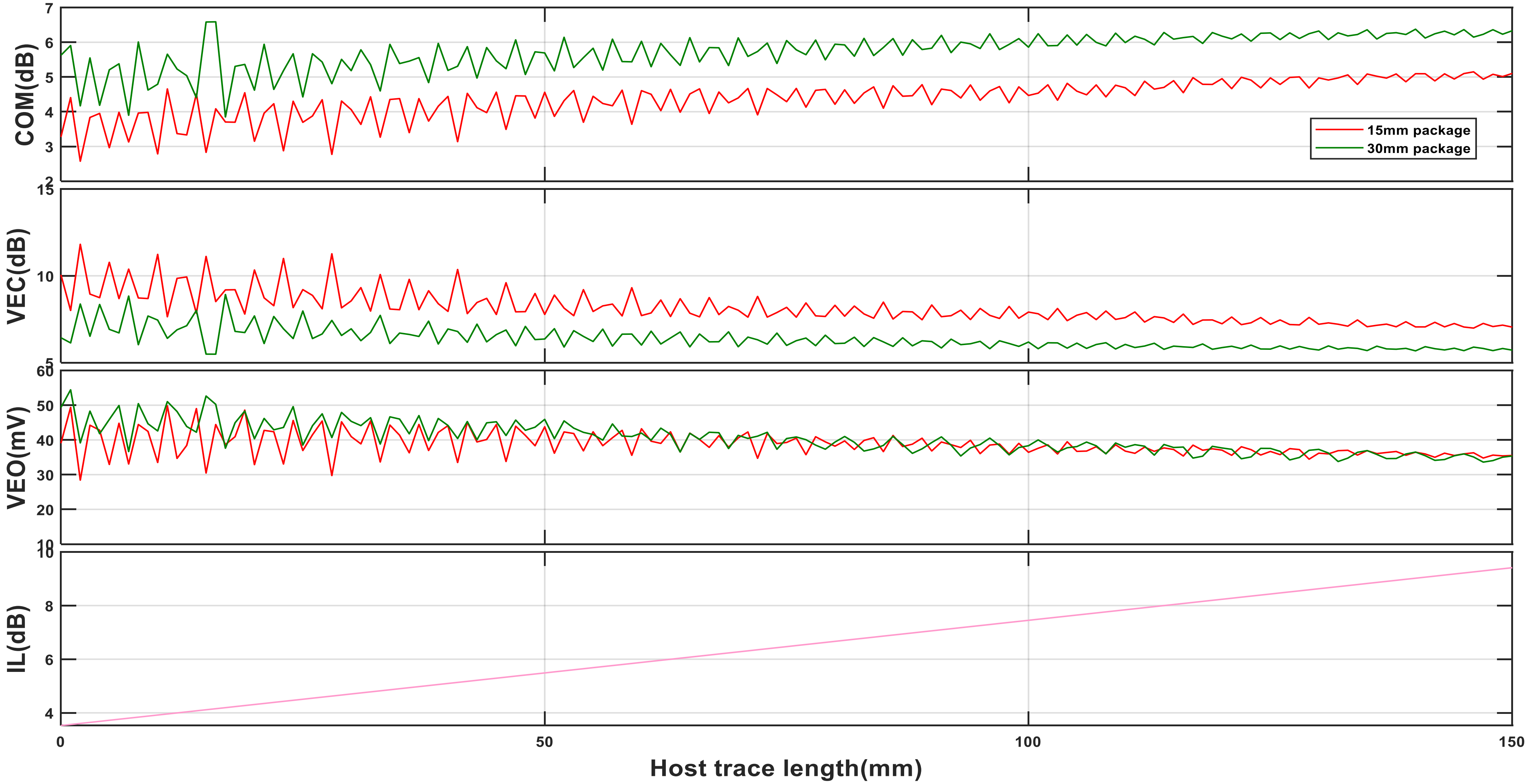
Effect of package length -Capacitor die model

Cd 0.11pF Ls 0pH Cb 0pF 100ohm host



Longer package trace (more loss) is better for COM and VEC although slightly worse for VEO

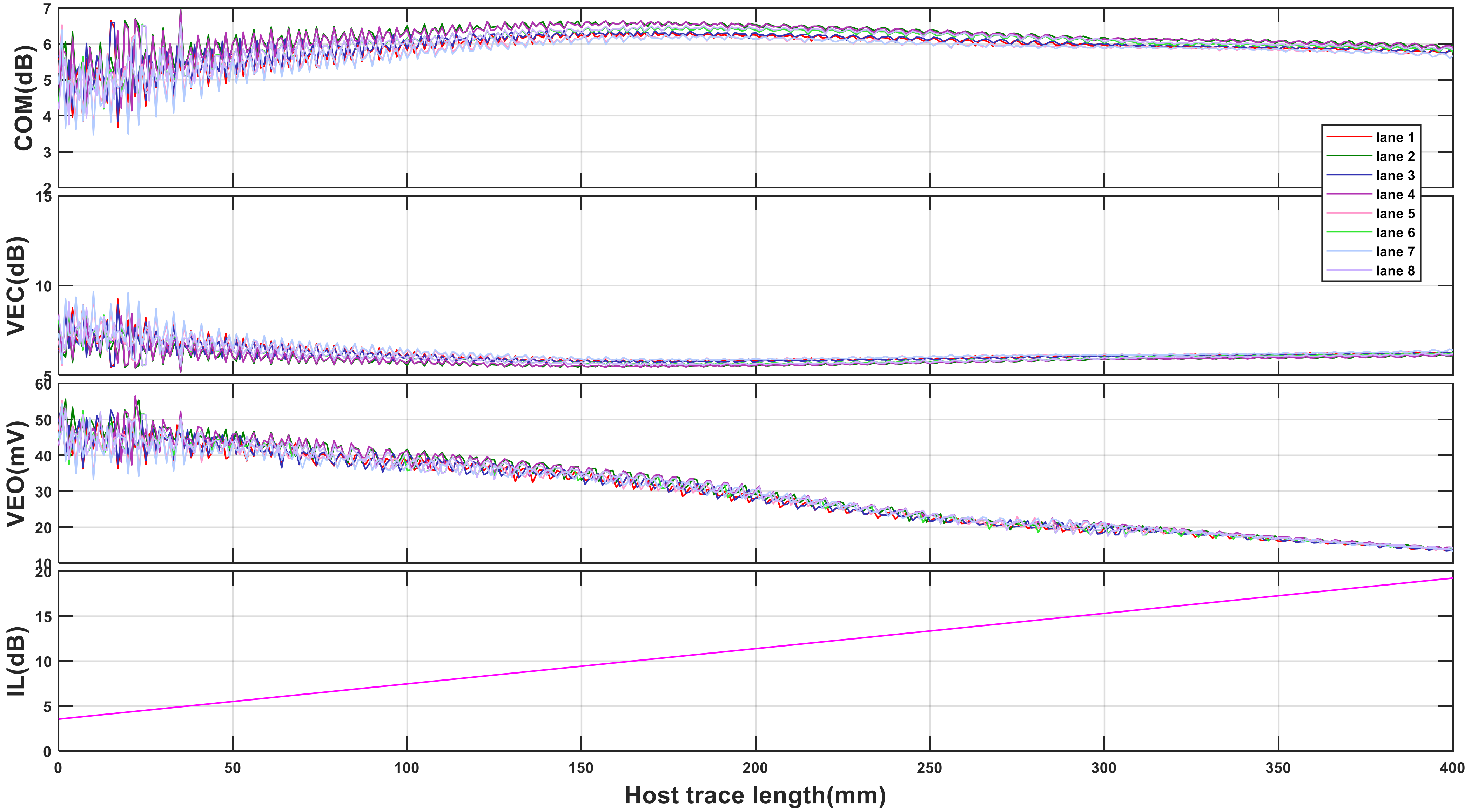
Cd 0.11pF Ls 0pH Cb 0pF 100ohm host



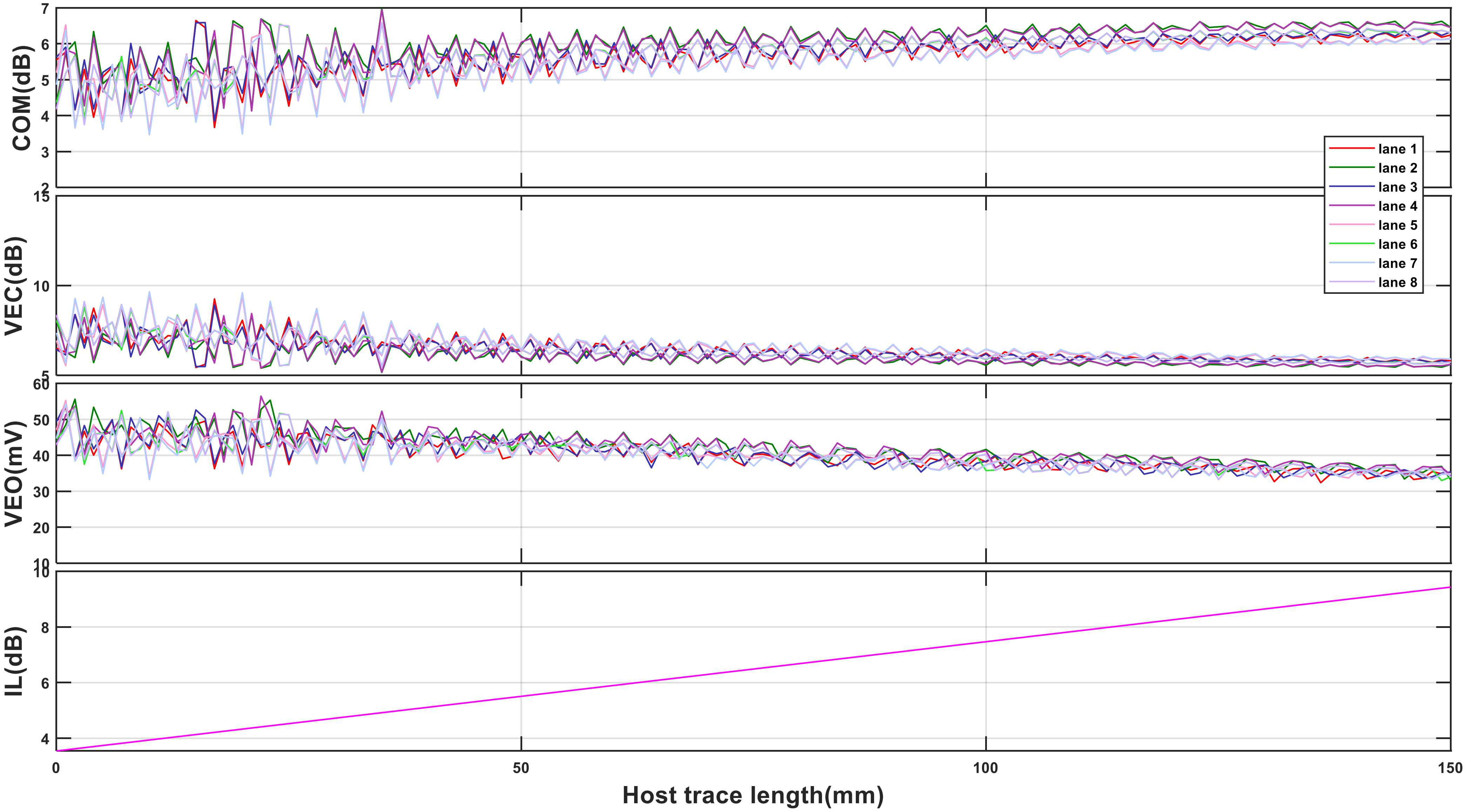
The “good” host trace lengths are different for different package lengths.

Effect of channel length, and connector lane on 30mm package

Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host -contd



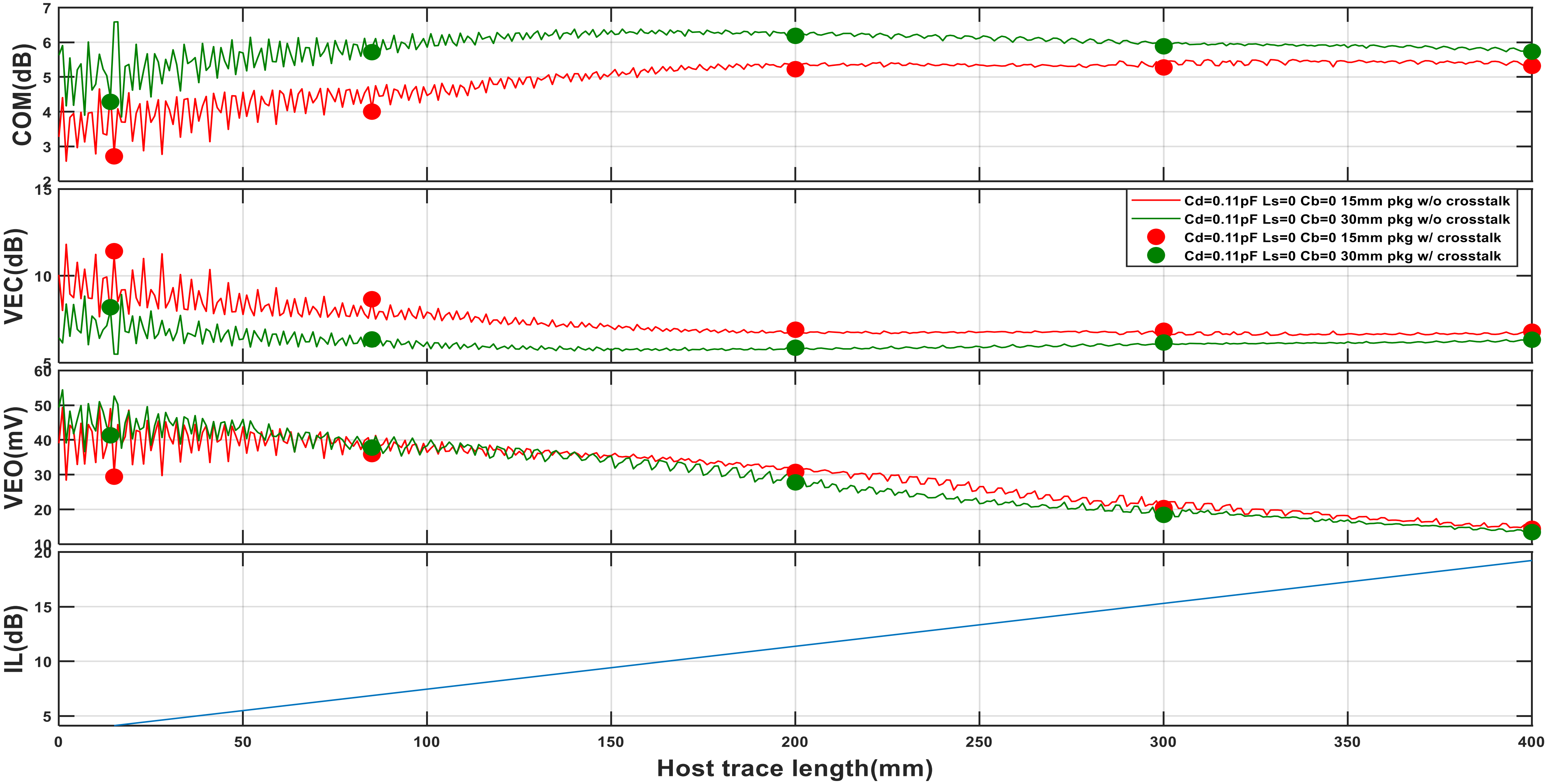
Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host



Effect of crosstalk

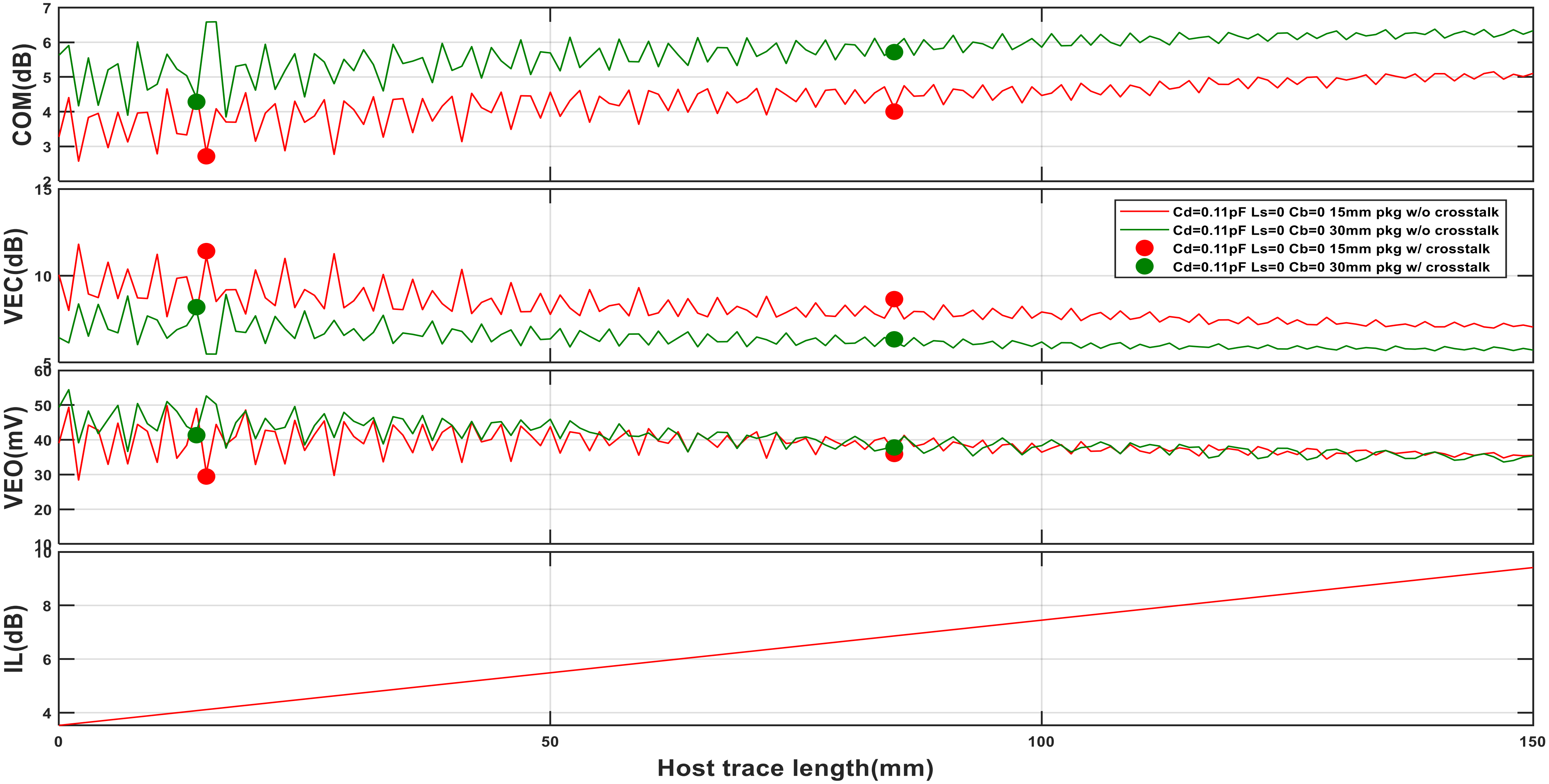
Performance was simulated just at some host lengths with connector crosstalk added

100ohm host impedance



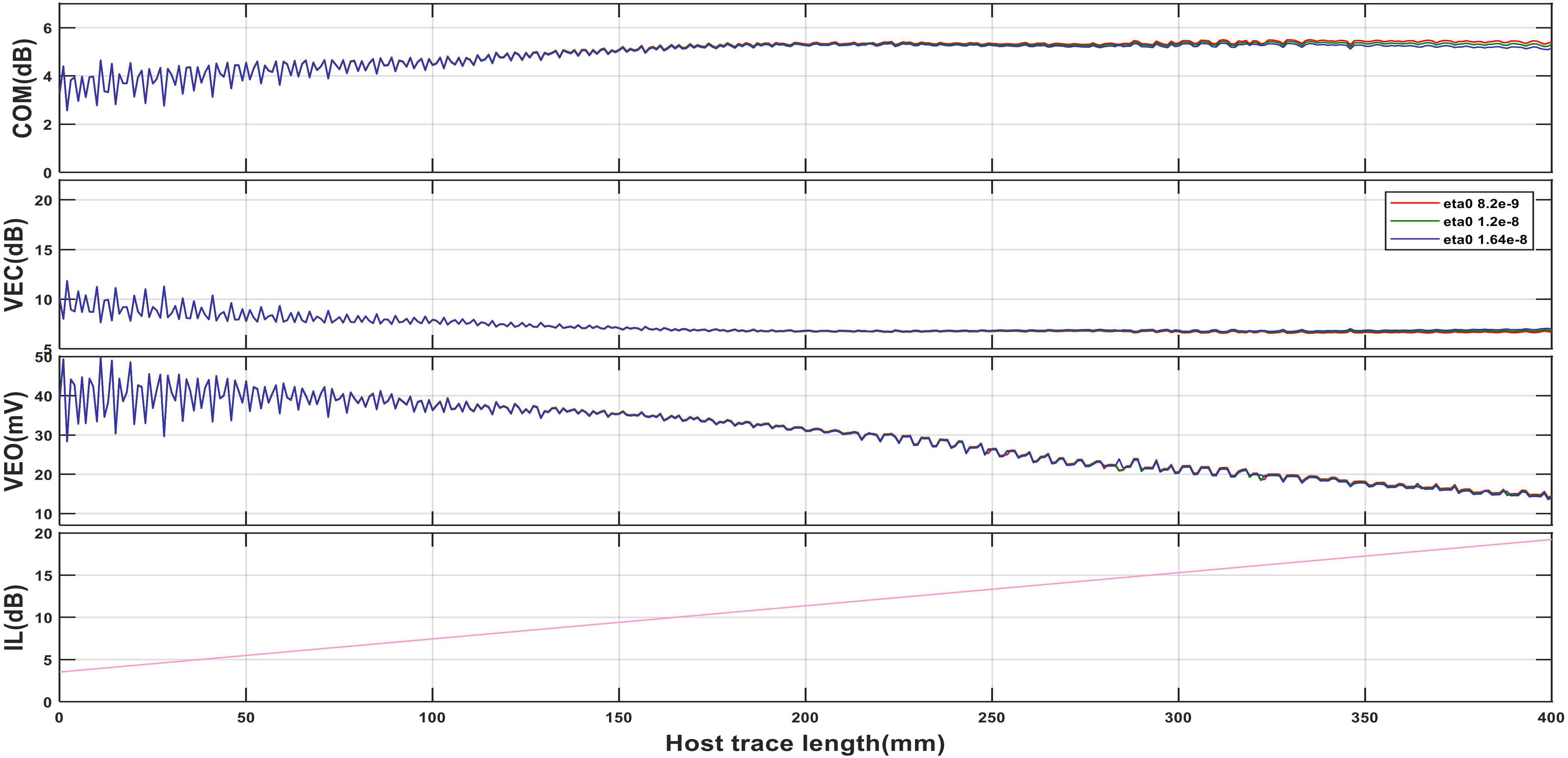
Crosstalk is not a significant degradation for this connector with these trace lengths.

100ohm host impedance



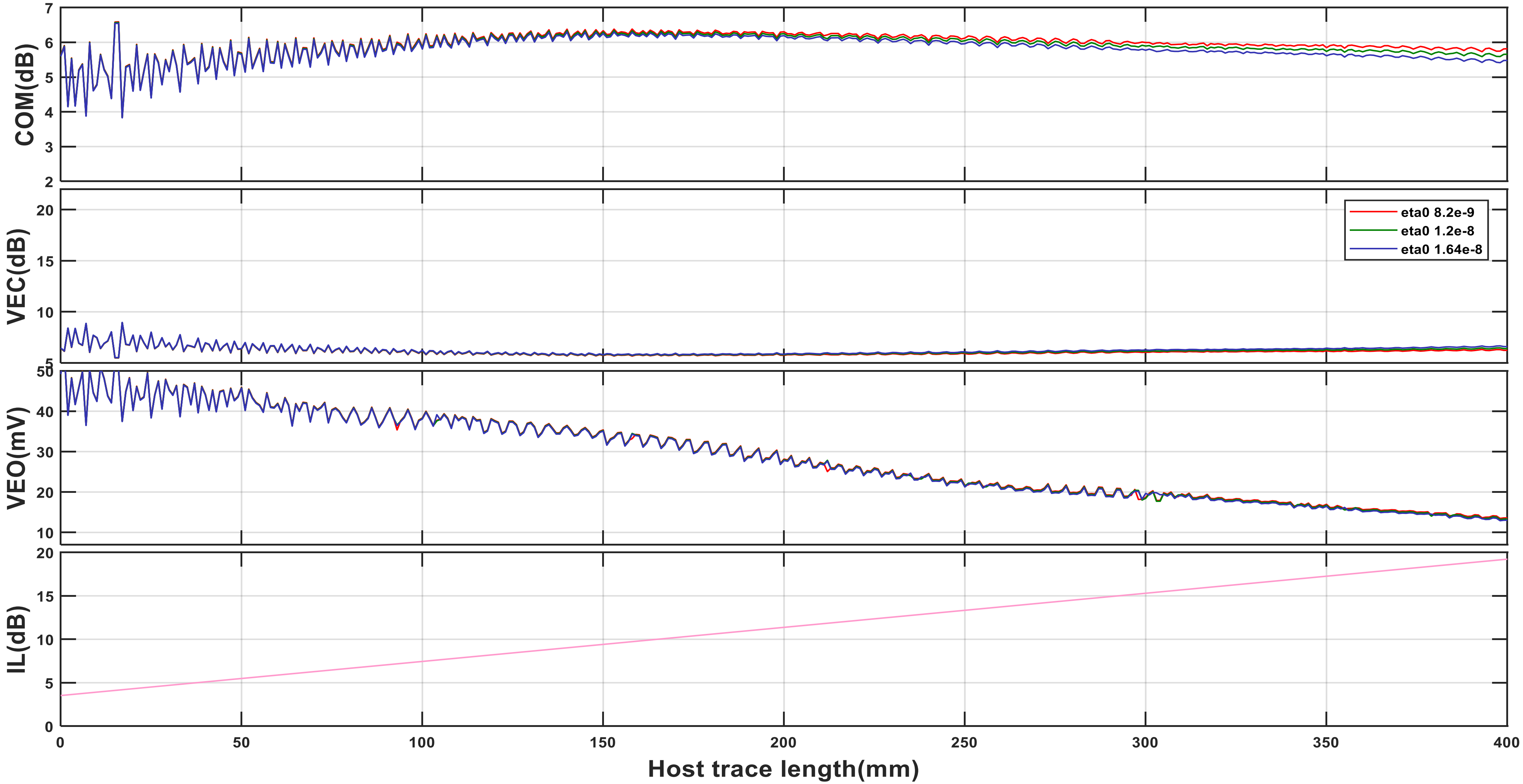
Effect of Eta0

Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



For the short package there is little effect in changing eta_0 in this range. However the required value for eta_0 to represent break-in needs to be evaluated.

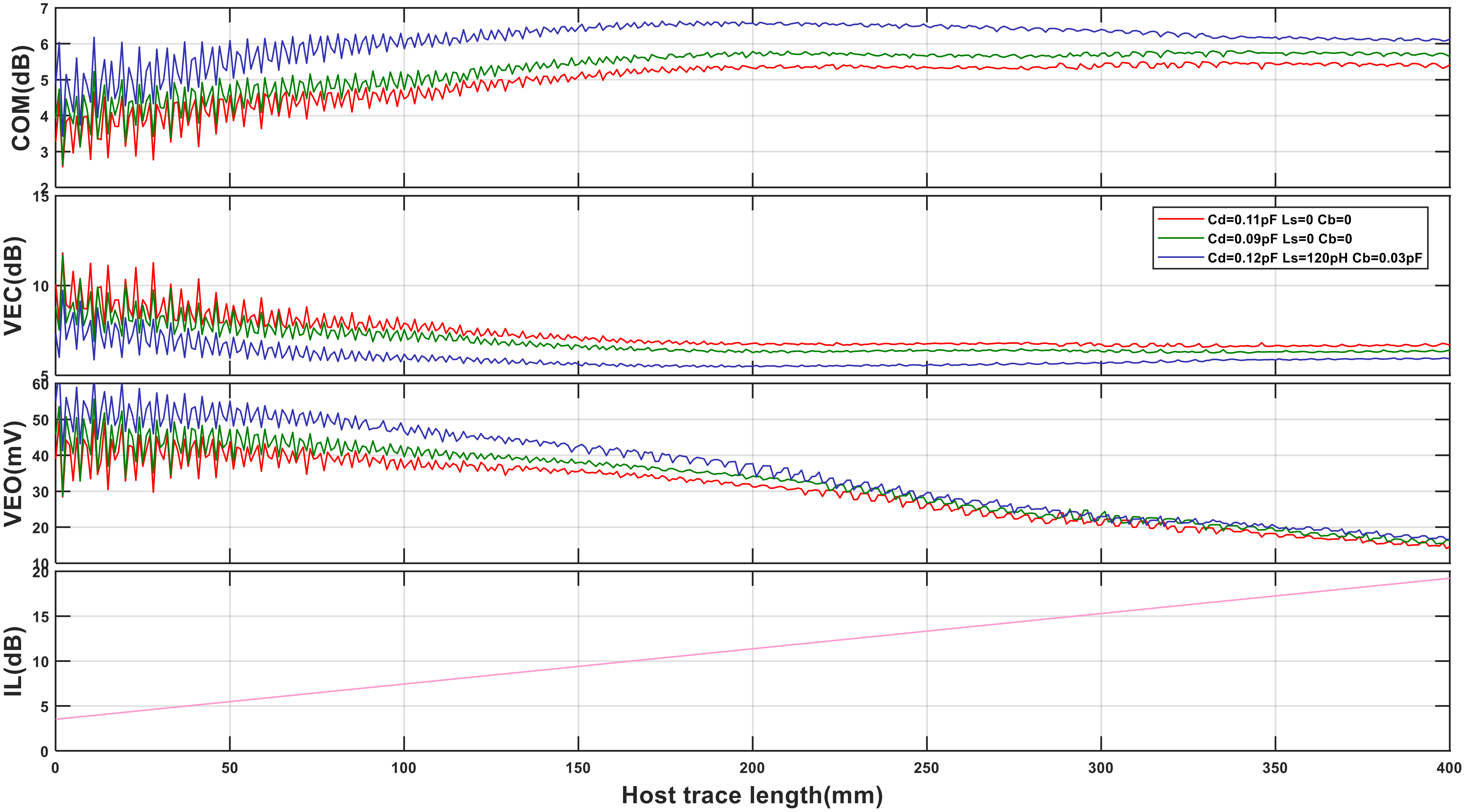
Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host



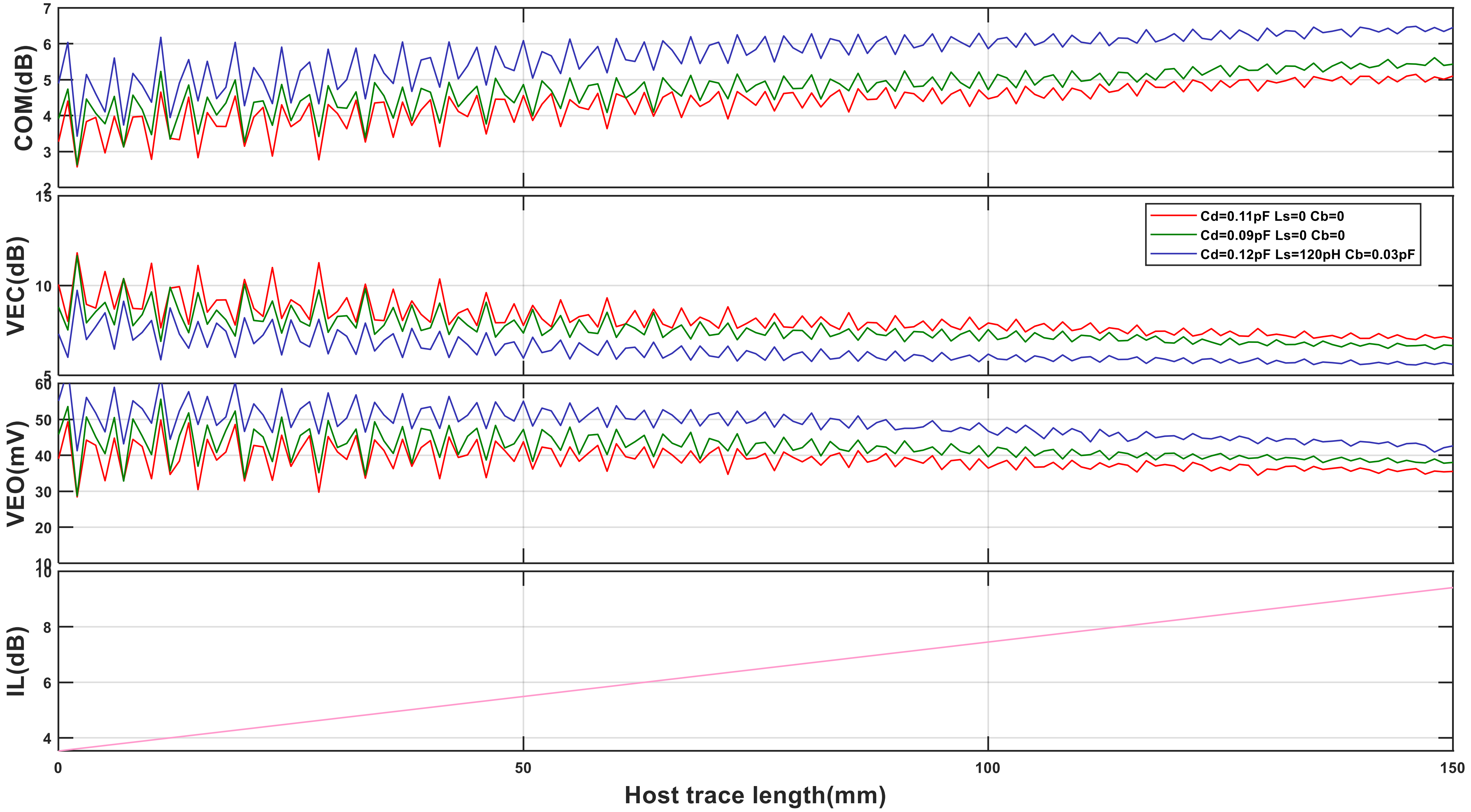
For the longer package changing eta0 in the range evaluated is still not significant even for the higher loss hosts

Effect of die model

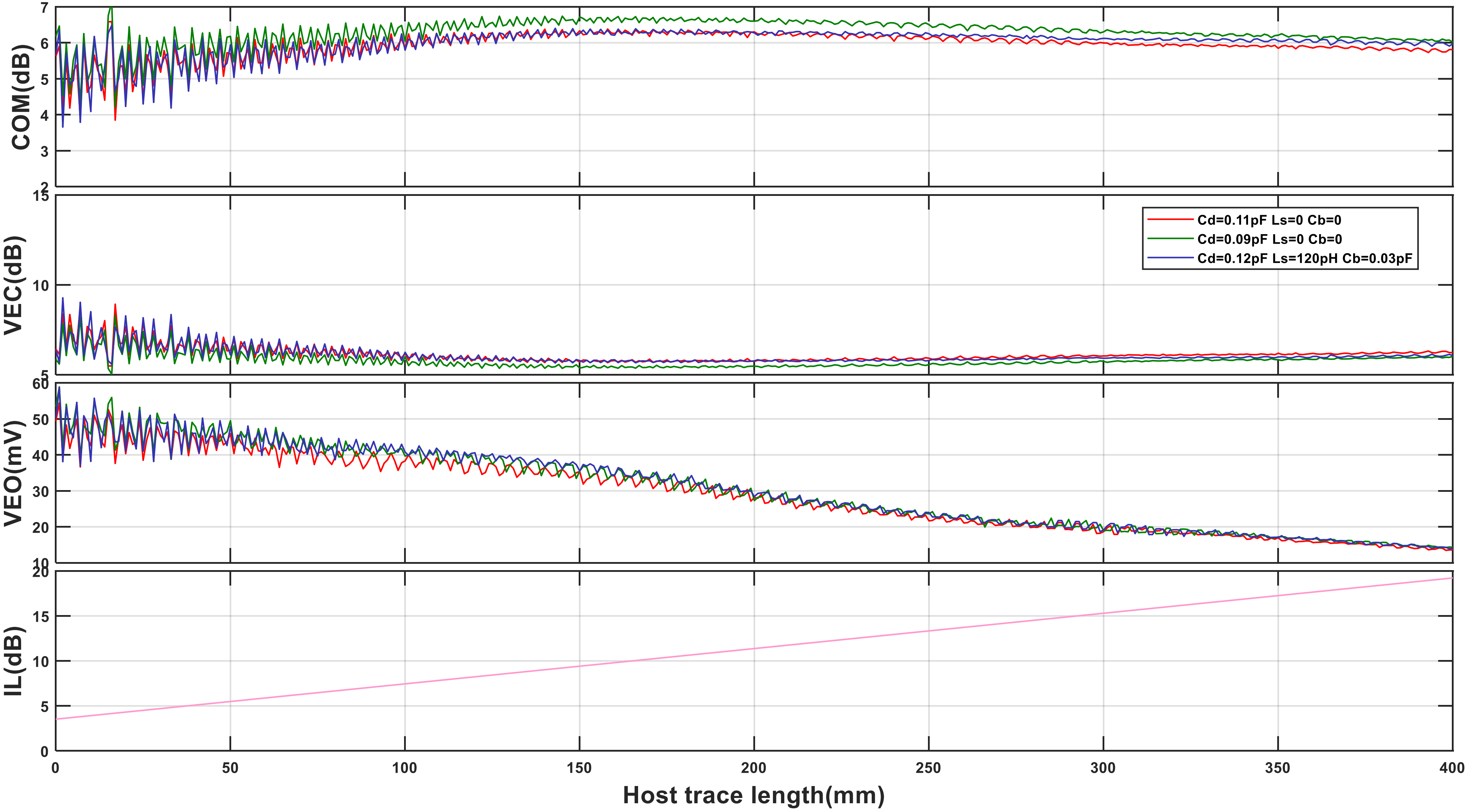
15mm pkg 100ohm host



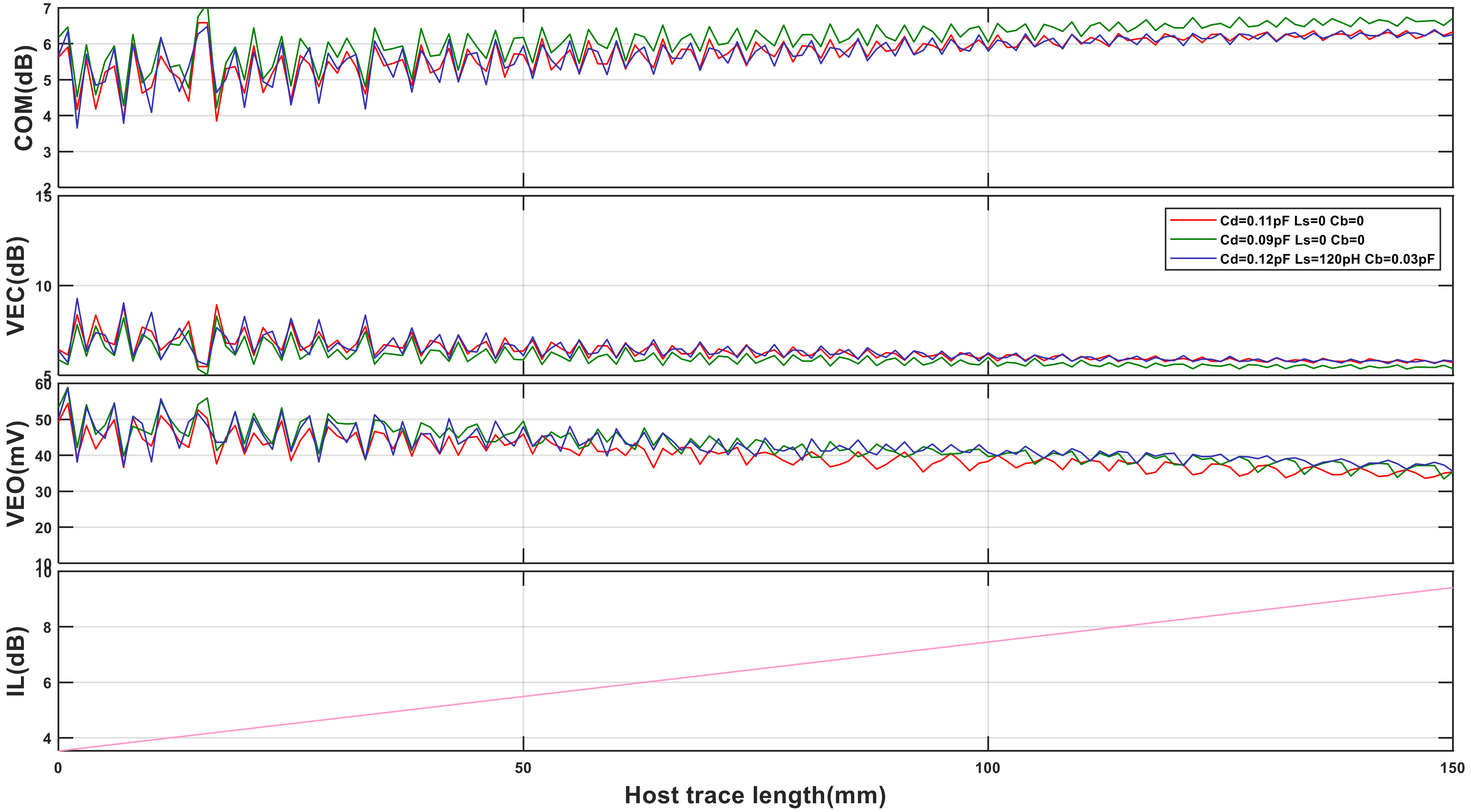
15mm pkg 100ohm host



30mm pkg 100ohm host



30mm pkg 100ohm host



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