#### MARVELL®

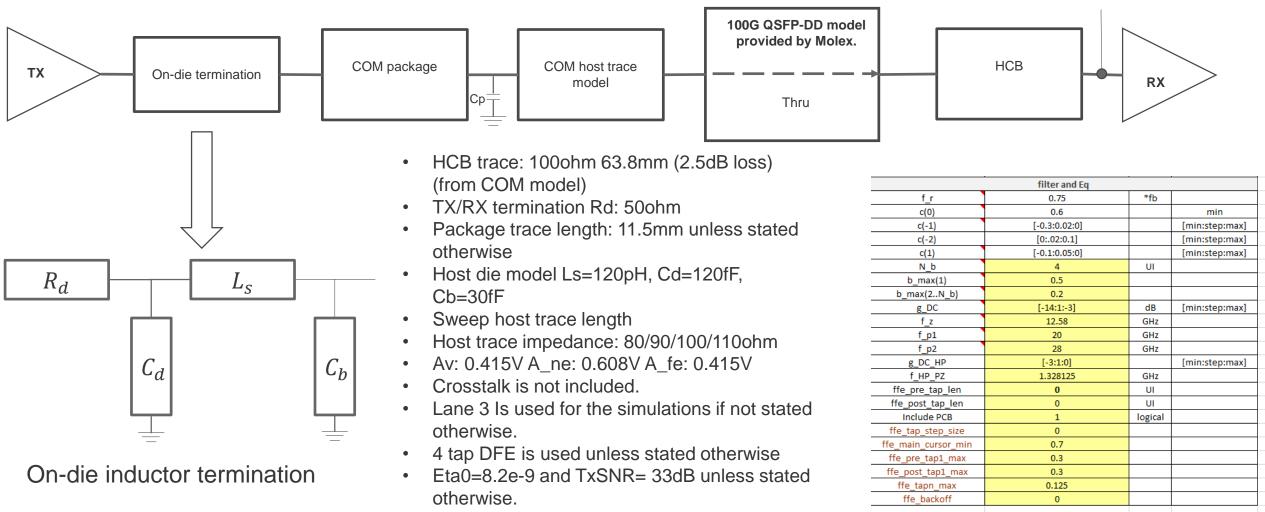
# Comparison of C2M performance at TP1a with whole channel performance.

Mike Dudek Tao Hu 9/3/2019 Presented at September 2019 Interim Indianapolis.

#### Introduction

- Dudek\_3ck\_01\_0719 explored the effect of host trace length on C2M TP1a performance with different die models, package lengths and some host impairments. It showed significant degradations and resonances at shorter host trace lengths. Unfortunately the "good host trace lengths" became "bad host trace lengths" if the connector lane or details of the die model etc. were changed. I.e. It is not possible to choose "good" lengths. The system needs to be designed to cope with the bad resonances.
- Since then the inductor model has been adopted for the host ASIC die model.
- This presentation provides more TP1a simulations with this host ASIC die model and presents simulations of the whole channel performance.
- It shows that a significantly stronger equalizer than the 5 tap FFE equalizer is required for adequate whole channel performance.
- The presentation also provides correlation between the VEC performance at TP1a and the whole channel performance and discusses the problem of setting a specification at TP1a.

## Chip to module block diagram for TP1a performance



Performance is simulated using COM 2.70

The complete COM table is in the back-up

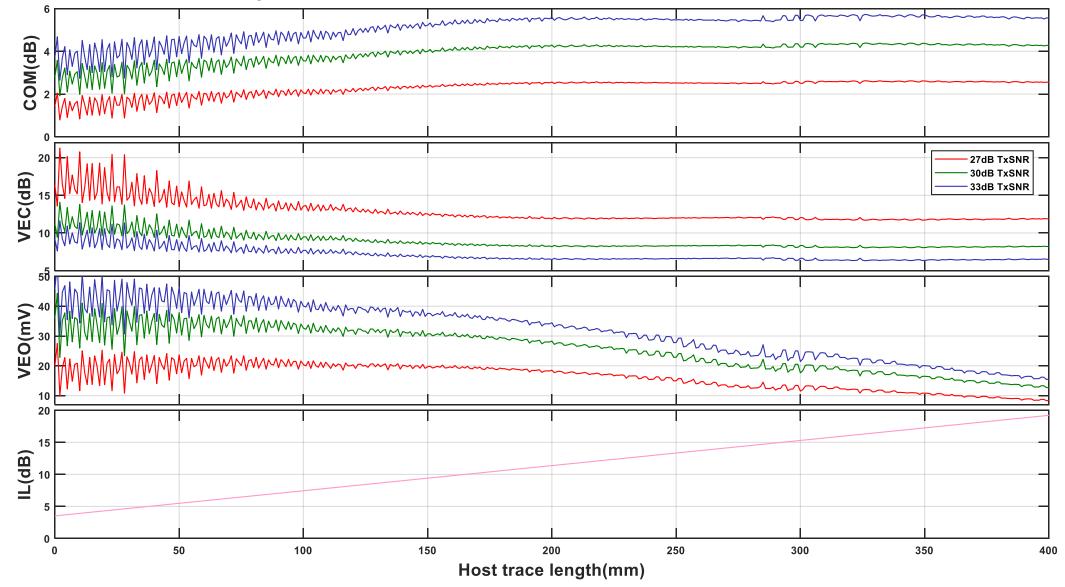
#### 4-tap DFE RX

#### COM PCB and package loss information

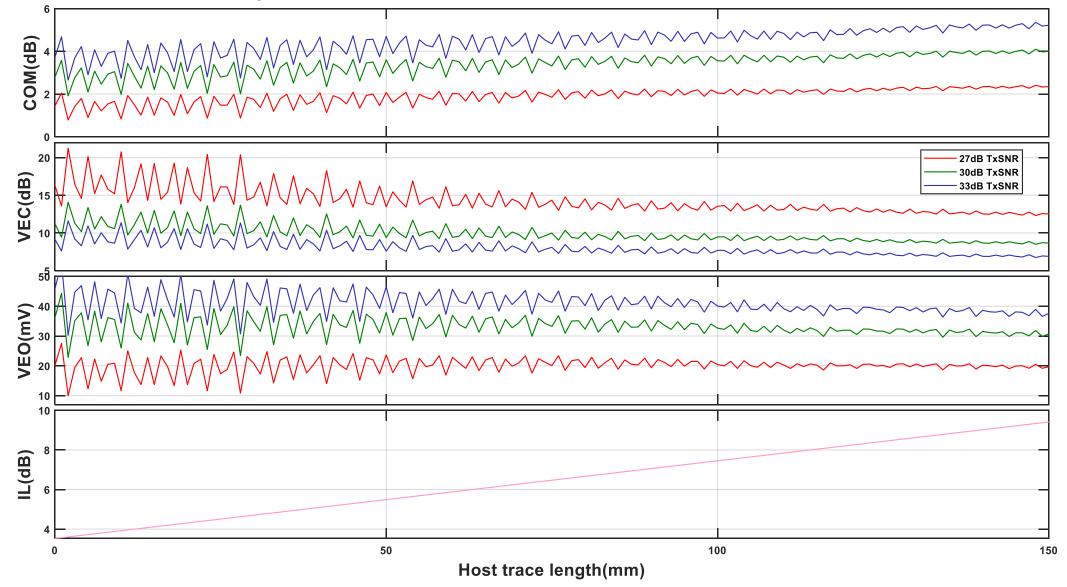
- PCB loss at 26.56GHz: ~0.04dB/mm, ~1dB/in. (58mm is equivalent to the 2.3dB MCB loss being proposed in the cable small group).
- Package loss at 26.56GHz: 0.1dB/mm
- Insertion loss plotted in this presentation includes host, HCB and connector, but not package.

#### Effect of TXSNR

TP1a results by TxSNR

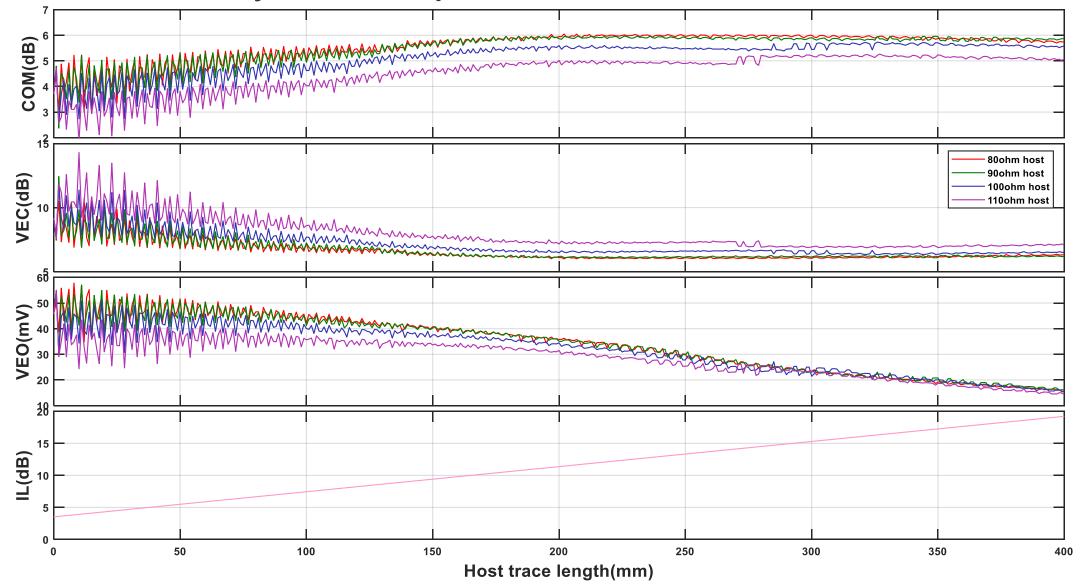


#### TP1a results by TxSNR

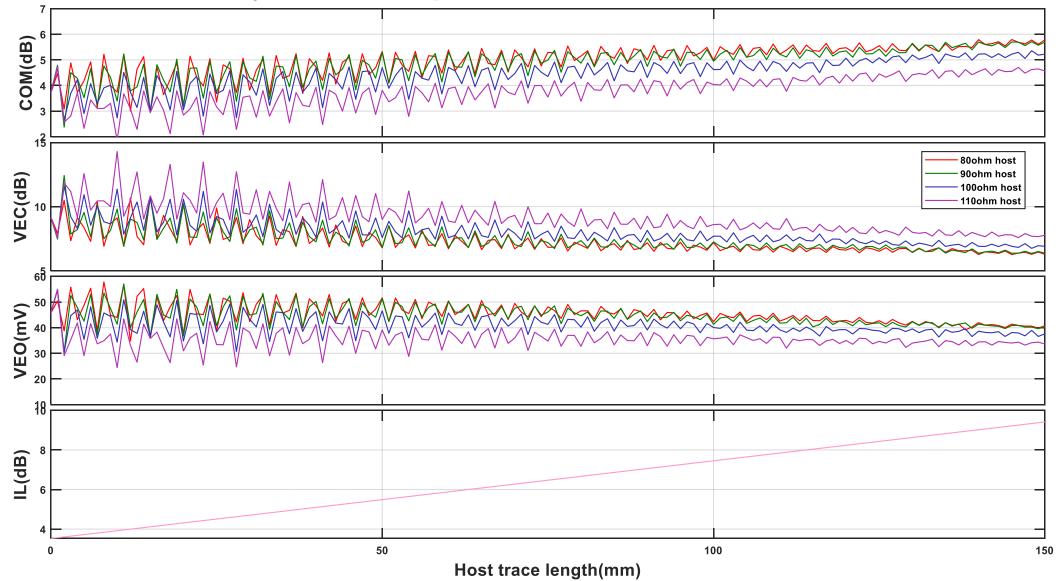


#### Effect of host trace impedance on TP1a performance

#### TP1a results by host impedance

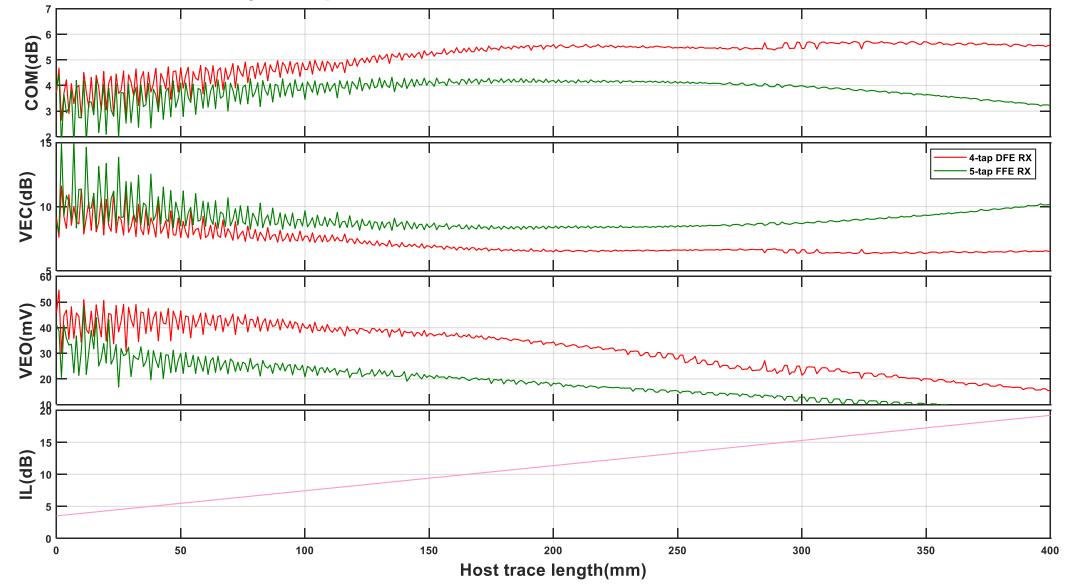


#### TP1a results by host impedance

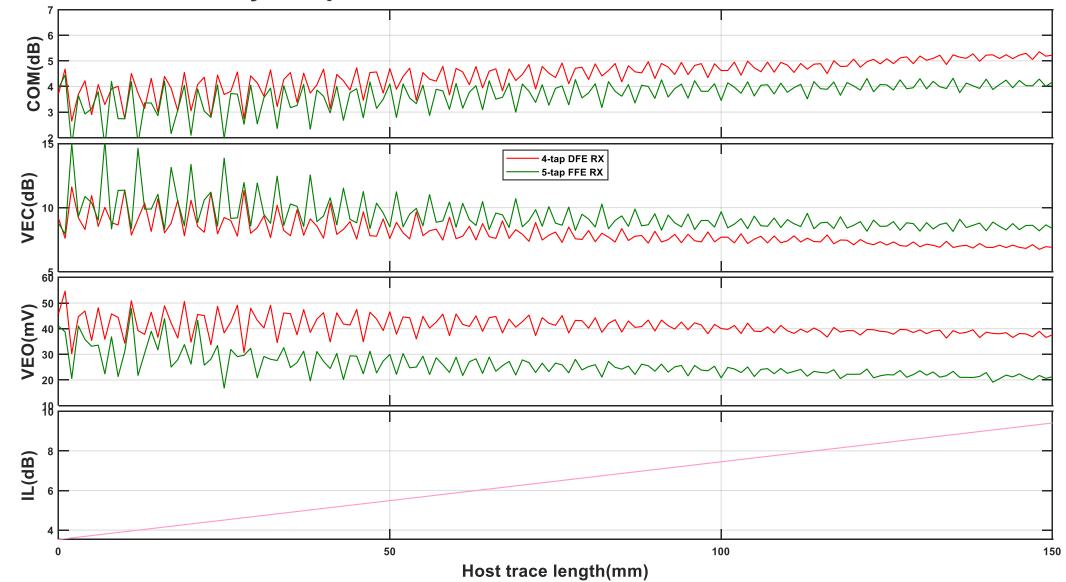


#### Effect of equalization

#### TP1a results by equalization



#### TP1a results by equalization

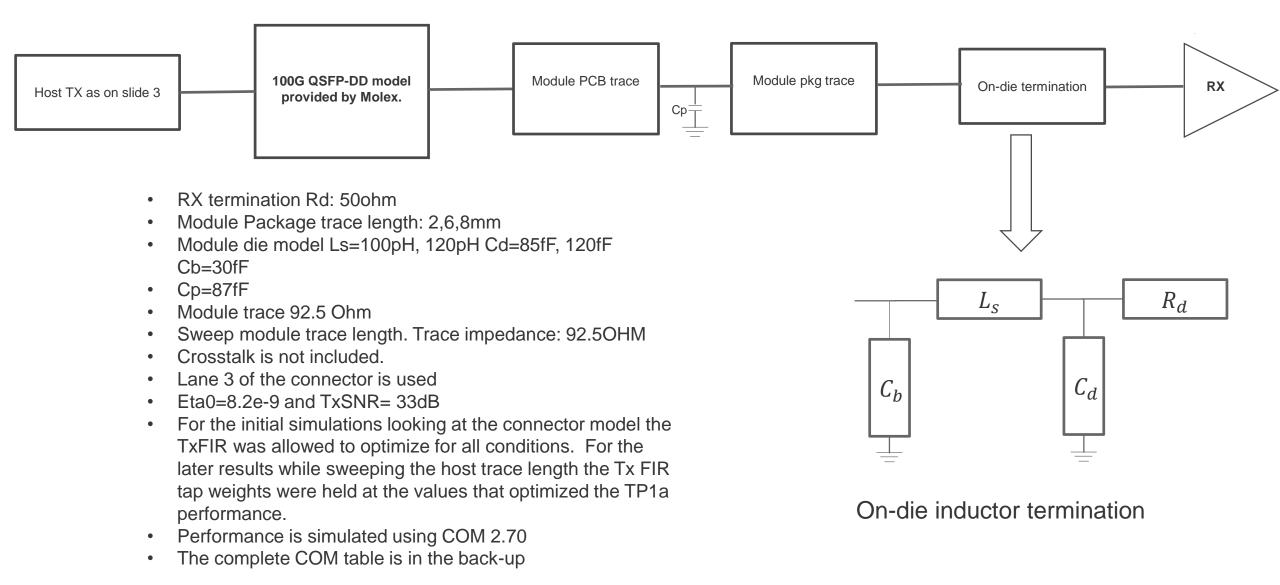


#### Conclusions and comments on TP1a performance.

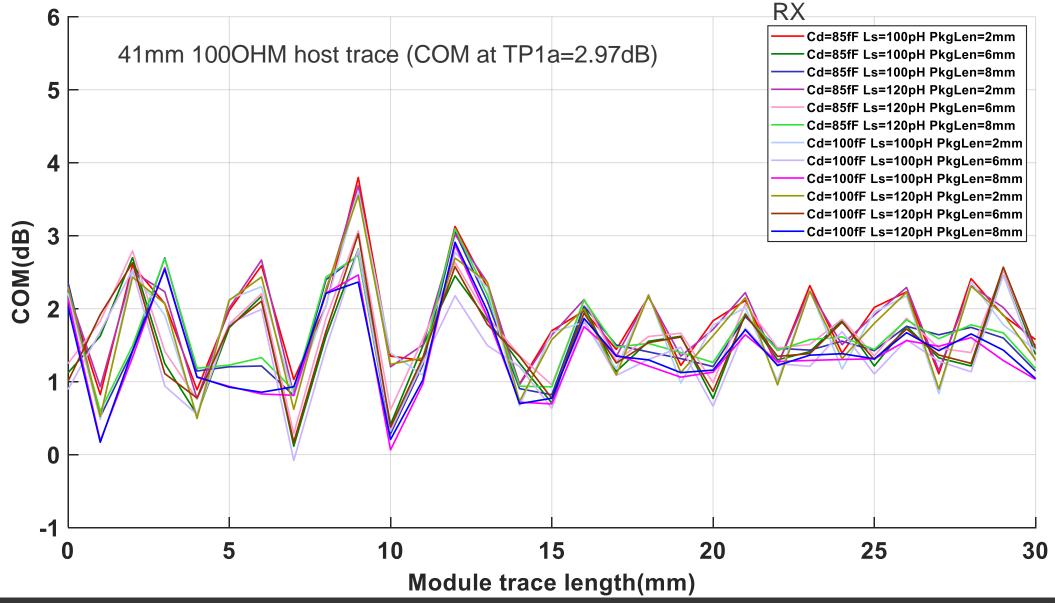
- The results of using the inductor model for the host ASIC have improved some of the results compared to just the capacitor model but it hasn't affected the qualitative effects.
  - Decreasing the Tx SNR below 33dB significantly degrades the results
  - The host trace impedance at 110 Ohm significantly degrades the results
- Using the 5 tap FFE instead of the 4 tap DFE as a reference equalizer significantly degrades the performance with the die model that includes the inductor to represent a T-coil.

Investigation of the effect of package trace length and module die model on end to end COM.

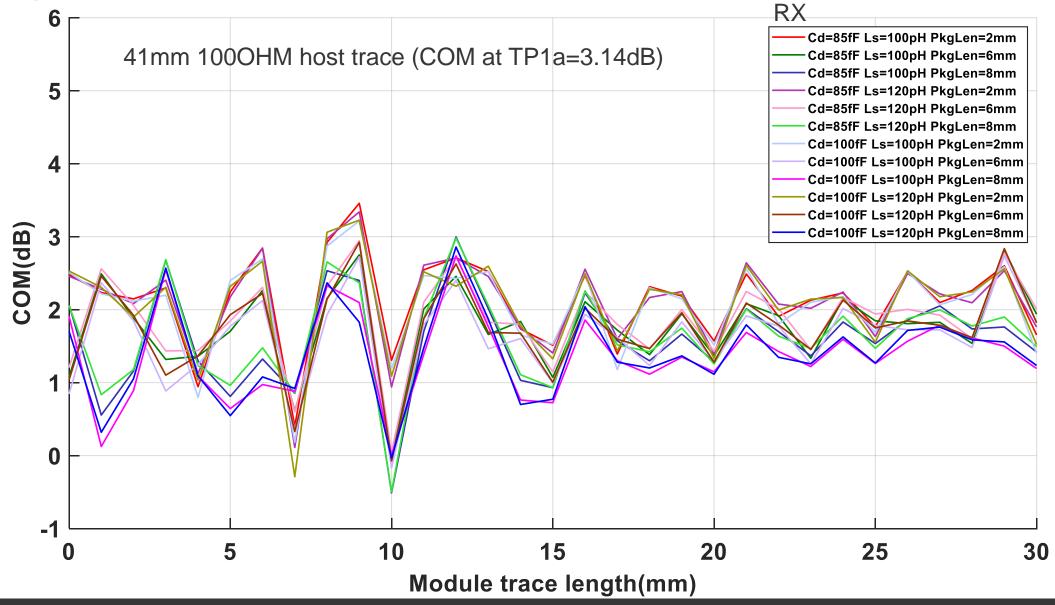
#### Chip to module block diagram for end to end performance



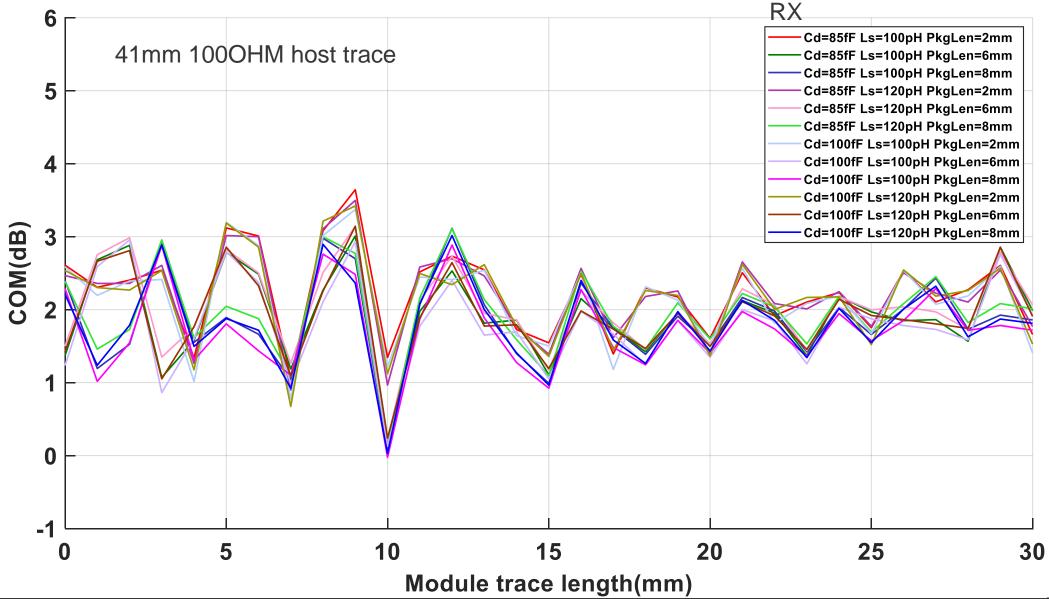
5-tap FFE end to end COM



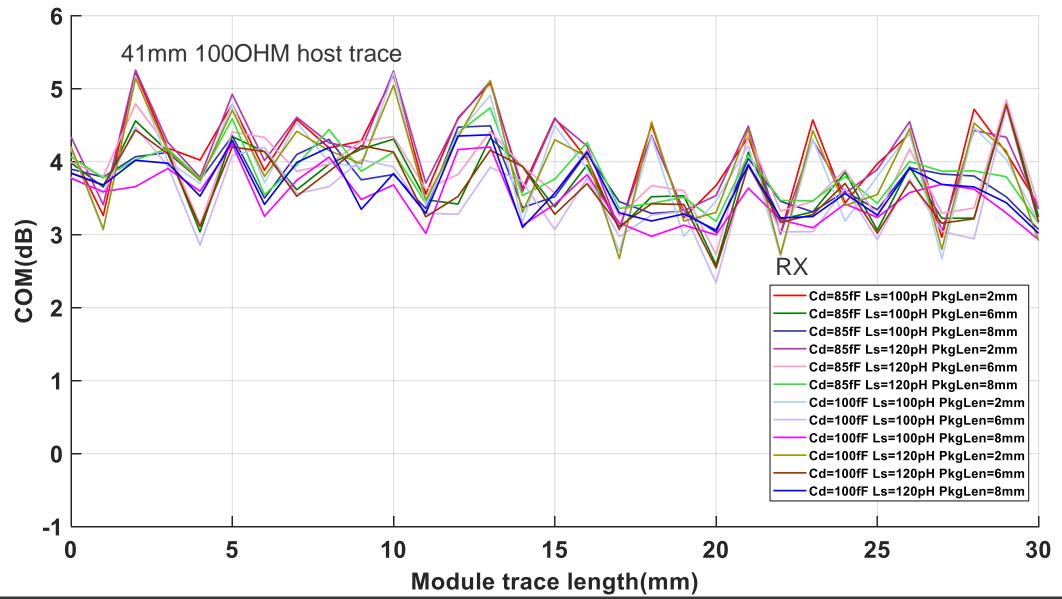
#### 4-tap DFE end to end COM



7-tap DFE end to end COM



12-tap DFE end to end COM

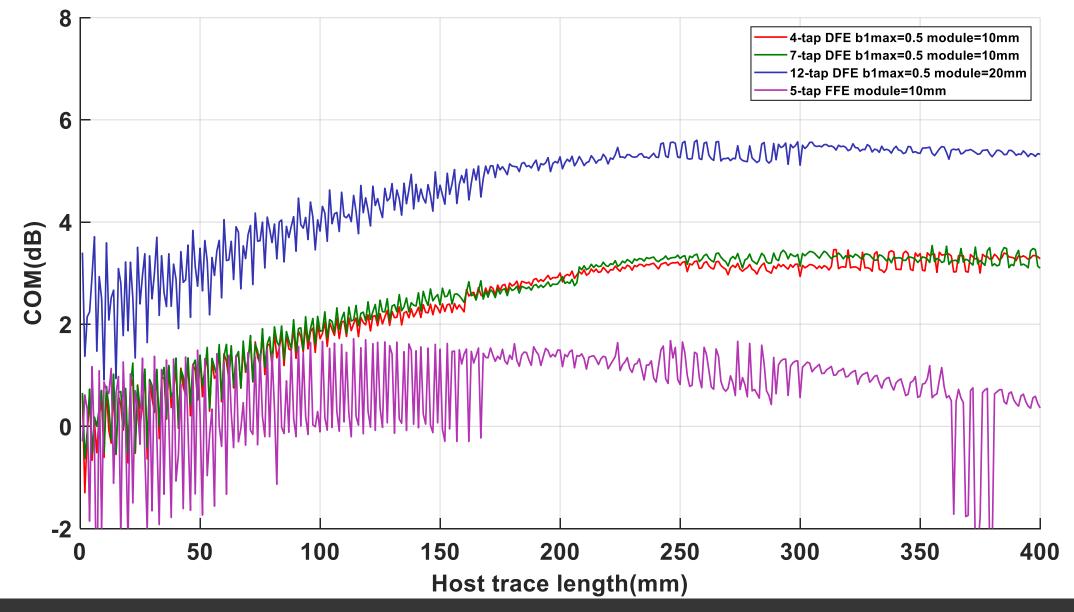


Conclusions and comments on module model.

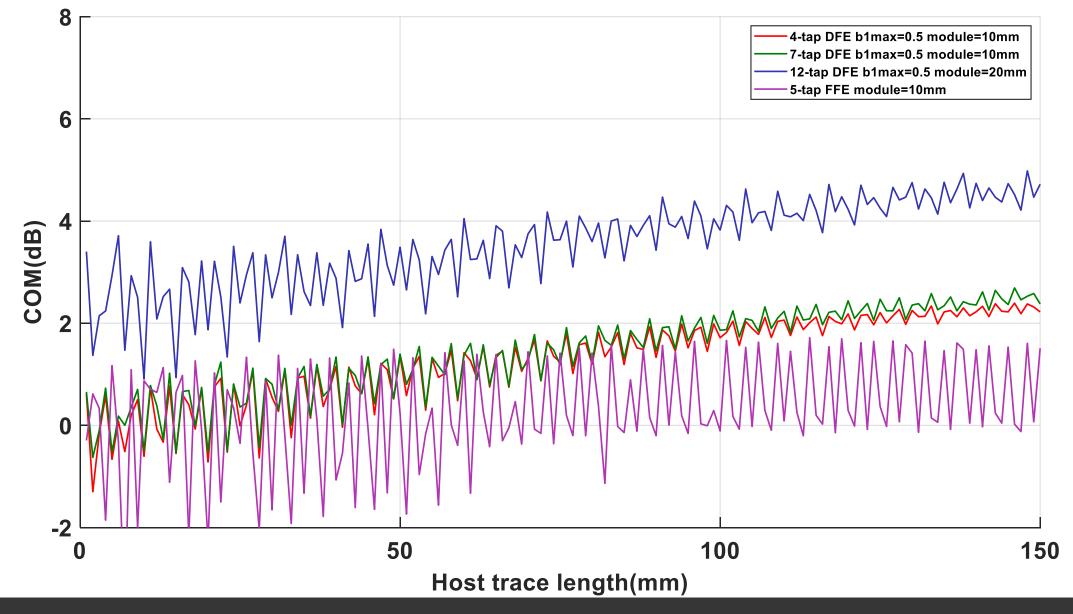
- The end to end COM performance is significantly worse than that at TP1a unless the 12 tap DFE is used.
- The 120pH inductor gave poorer performance than 100pH, whether the Cd value was 85fF or 100fF
- Cd value of 85fF gave somewhat better results but we felt it was rather optimistic.
- 8mm module trace gave significantly poorer results and we felt this was longer than likely to be in the module.
- Based on this a module package/die model of Ls=100pH, Cd=100fF, Cb=30fF and module package trace of 6mm was chosen for further simulation.

# Investigation of Host trace length on end to end COM with different equalizers.

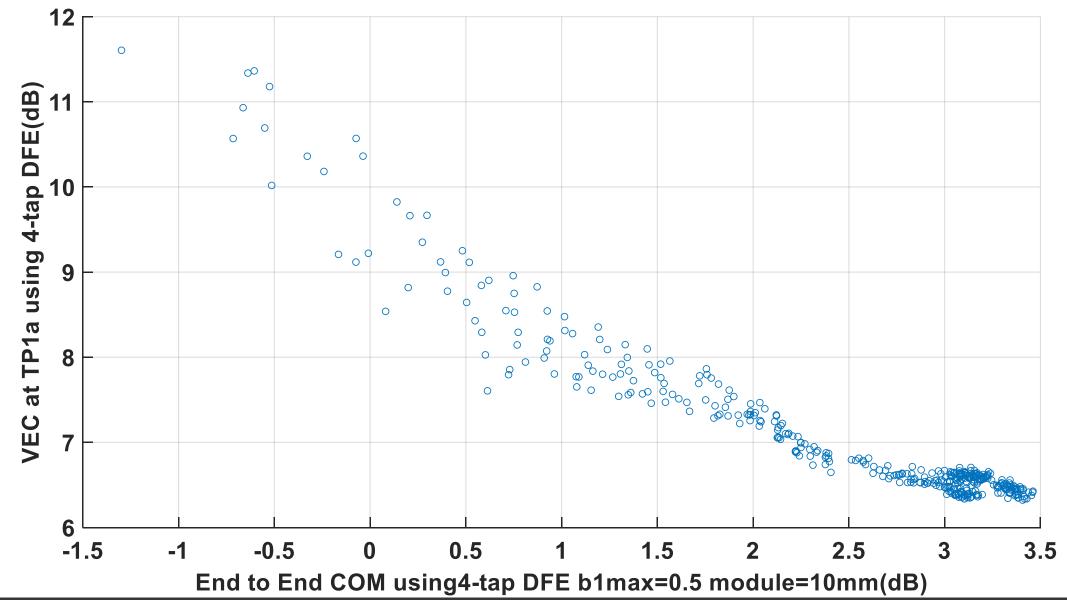
#### End to end COM



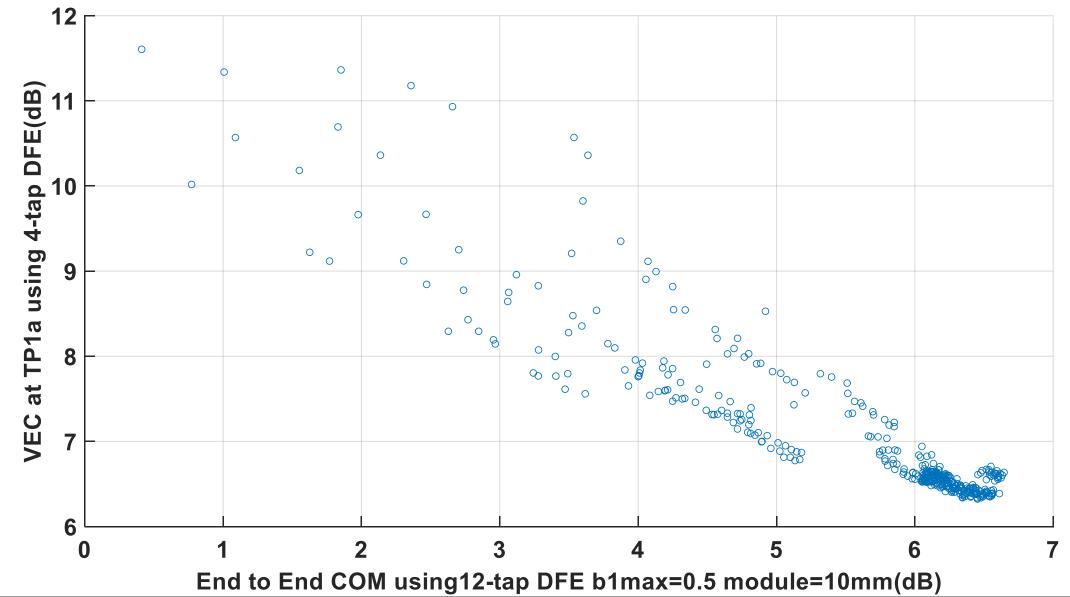
#### End to end COM



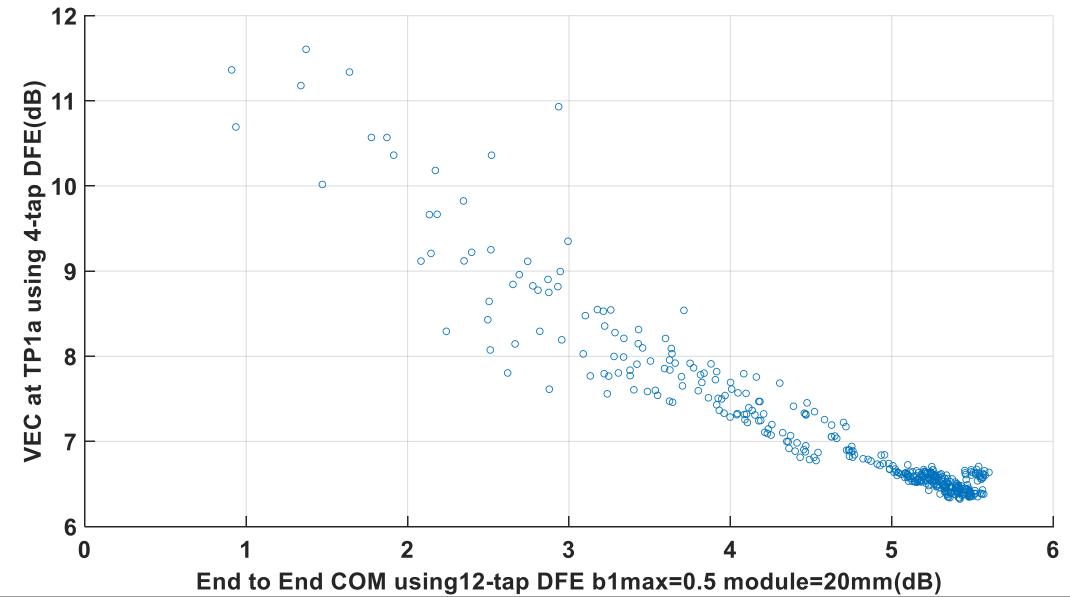
### VEC at TP1a vs. End to End COM



## VEC at TP1a vs. End to End COM



## VEC at TP1a vs. End to End COM



## Conclusions.

- With these module package and die models a stronger equalizer is needed in the module to provide adequate performance for the critical 50mm to 160mm host trace lengths where the host could also be used for the CR specification.
- With that stronger equalizer 3dB COM is achievable for the end to end performance provided the TP1a VEC with a 4tap DFE reference receiver is >= 7.5 dB. However that still doesn't enable the 50mm host trace length which needs a >=9dB VEC with that equalizer. With the >=9dB VEC spec at TP1a the end to end COM with the 12 tap DFE can be as bad as 2dB.
- Note that there are other impairments that have not been explored in this presentation. In particular the effect of vias in the host and module.

#### Back-up

#### TP1a COM spreadsheet

#### 4-tap DFE

	filter and Eq						Noise, jitter
f_r	0.75	*fb		sigma_RJ			
c(0)	0.6		Parameter	Table 93A-1 parameters Setting	Units	A_DD	
c(-1)	[-0.3:0.02:0]		f_b	53.125	GBd	eta_0	8
c(-2)	[0:.02:0.1]		f min	0.05	GHz	SNR TX	
c(1)	[-0.1:0.05:0]		Delta f	0.01	GHz		
N_b	4	UI	C_d	[1.2e-4 0]	nF		
b_max(1)	0.5		 L s	[0.12, 0]	nH		
b_max(2N_b)	0.2		 C b	[0.3e-4 0]	nF		
g_DC	[-14:1:-3]	dB			III	Tab	le 93A–3 paramet
fz	12.58	GHz	z_p select	[1]		Parameter	Setti
f_p1	20	GHz	z_p (TX)	[11.5 11.5; 1.8 1.8 ]	mm	package_tl_gamma0_a1_a2	[0 0.0009909
f_p2	28	GHz	z_p (NEXT)	[00; 00]	mm	package_tl_tau	6.1400
g_DC_HP	[-3:1:0]	GIL	z_p (FEXT)	[11.5 11.5; 1.8 1.8 ]	mm	package_Z_c	[87.5 87.5 ; 9
f HP PZ	1.328125	GHz	z_p (RX)	[00; 00 ]	mm	Tab	le 92–12 paramet
ffe_pre_tap_len	0	UI	C_p	[0.87e-4 0]	nF	Parameter	Setti
ffe_post_tap_len	0	UI	R_0	50	Ohm	board_tl_gamma0_a1_a2	[0 3.8206e-04
Include PCB	1	logical	R_d	[ 50 50]	Ohm	board_tl_tau	5.790E
ffe_tap_step_size	0	logical	A_v	0.415	V	board_Z_c	[100 1
ffe main cursor min	0.7		A_fe	0.415	V		
ffe_pre_tap1_max	0.3		A_ne	0.6	V		
ffe_post_tap1_max	0.3		L	4		COM Pass threshold	
ffe_tapn_max	0.125		M	32		ERL Pass threshold	
ffe_backoff	0					DER_0	1.
1		1					-

Noise, iitter 0.01 UI 0.02 UI 8.20E-09 V^2/GHz 33 dB 0.95

Table 93A–3 parameters							
Parameter	Setting	Units					
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]						
package_tl_tau	6.1400E-03	ns/mm					
package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	Ohm					
	Table 92–12 parameters						
Parameter	Setting						
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]						
board_tl_tau	5.790E-03	ns/mm					
board_Z_c	[100 100]	Ohm					
	1						

COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical

• HCB trace: 100ohm 63.8mm (2.5dB loss)

#### End to end COM spreadsheet

c(-1)	[-0.3:0.02:0]									
c(-2)	[0:.02:0.1]									
	[-0.1:0.05:0]	UI								
b_max(1)	0.5			Table 02A 1 parameters	Noise, jitter					
b_max(2N_b)	0.2					sigma Bl	0.01	UI		
			Parameter	Setting	Units					
			fb	52 125	GRd	A_DD	0.02	UI		
p1						eta 0	8 20E-09	V^2/GHz		
			f_min	0.05	GHz					
f_HP_PZ	1.328125	GHz	Delta f	0.01	GHz	SNR_TX	33	dB		
ffe_pre_tap_len	0	UI				R LM	0.95			
	0		C_d	[1.2e-4 1.0e-4]	nF		0.00			
		logical	1.5	[0.12, 0.1]	nH					
			C_b	[0.3e-4 0.3e-4]	nF	Т	Table 93A–3 parameters			
ffe post tap1 max	0.3		z pselect	[1]		Parameter	Setting	Units		
ffe_tapn_max	0.125					package tl gamma0 a1 a2	[0 0.0009909 0.0002772]			
ffe_backoff	0		z_p(IX)	[11.5 11.5; 1.8 1.8 ]	mm			ns/mm		
	filter and Eq		z_p (NEXT)	[00;00]	mm			Ohm		
f_r	0.75	*fb	7 n (FEXT)	[11 5 11 5 1 8 1 8 ]	mm					
c(0)						I	able 92–12 parameters			
			z_p (RX)	[2 2; 0 0 ]	mm					
			Ср	[0.87e-4 0.87e-4]	nF		0			
N b	0	UI	_					ns/mm		
b_max(1)	0							Ohm		
b_max(2N_b)	0		R_d	[ 50 50]	Ohm	board_2_c	[100 52.5]	Unin		
g_DC			A v	0.415	V					
f_z			_							
t_p1			A_fe	0.415	V					
-		GHZ	A ne	0.6	V					
f HP PZ	0.00025	GHz	<u></u>			COM Pass threshold	3	dB		
ffe_pre_tap_len	0	UI	L	4		EBL Dass throshold	10.5	dB		
ffe_post_tap_len	4	UI	м	32			-	uв		
Include PCB	1	logical				DER_0	1.00E-05			
					_	 T r	6 16E 02	nc		
			<b>Rx</b> Cd: 85fF, 100fF				0.105-03	ns		
						FORCE_TR	1	logical		
						_				
ffe tapn max	0.125									
	c(-2) c(1) N_b b_max(1) b_max(2N_b) g_DC f_z f_p1 f_p2 g_DC_HP f_HP_PZ ffe_pre_tap_len ffe_post_tap_len Include PCB ffe_tap_step_size ffe_main_cursor_min ffe_post_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_tap_step_size ffe_main_cursor_min ffe_post_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max ffe_bost_tap1_max	c(-2)         [0:.02:0.1]           c(1)         [-0.1:0.05:0]           N_b         4           b_max(1)         0.5           b_max(2N_b)         0.2           g_DC         [-14:1:-3]           f_z         12.58           f_p1         20           f_P2         28           g_DC_HP         [-3:1:0]           f_HP_PZ         1.328125           ffe_pre_tap_len         0           Include PCB         1           ffe_tap_step_size         0           ffe_post_tap_len         0.3           ffe_post_tap_max         0.3           ffe_tap_step_size         0           ffe_tap_max         0.3           ffe_tap_ode         0           ffe_backoff         0           ffe_backoff         0           c(0)         0.6           c(-1)         [-0.3:0.02:0]           c(-2)         [0:02:0.1]           c(1)         [-0.1:0.05:0]           N_b         0           b_max(1)         0           b_max(2N_b)         0           g_DC         [-14:1:-3]           f_z         18.88 <tr< td=""><td>c(-2)         [0:.02:0.1]           c(1)         [-0.1:0.05:0]           N_b         4         UI           b_max(1)         0.5         <math>\Box</math>           b_max(2N_b)         0.2         <math>\Box</math>           g_DC         [-14:1:-3]         dB           f_z         12.58         GHz           f_p1         20         GHz           f_p2         28         GHz           g_DC_HP         [-3:1:0]         GHz           f_f_PPZ         1.328125         GHz           ffe_pre_tap_len         0         UI           Include PCB         1         logical           ffe_tap_step_size         0         UI           include PCB         1         logical           ffe_tap_max         0.3         O           ffe_post_tap1_max         0.3         O           ffe_backoff         0         O           c(0)         0.6         C(-1)         Co:0:0:0]           c(-1)         [-0.3:0.02:0]         C(-2)         Ci:0:0:0:1]           c(1)         [-0.1:0.05:0]         O         UI           b_max(1)         0         UI         D           b_max(1)</td><td><math>c(2)</math>       [0:02:0.1]         <math>(1)</math>       [0.1:0.05:0]         <math>N_{b}b</math>       4       UI         <math>b_{max(2,N,b)}</math>       0.2         <math>g_{DC}</math>       [4:4:1:-3]       dB         <math>f_{p1}2</math>       28       GHz         <math>f_{p2}2</math>       28       GHz         <math>g_{DC}</math>       [4:4:1:-3]       dB         <math>f_{p2}2</math>       28       GHz         <math>f_{p2}2</math>       28       GHz         <math>f_{p2}2</math>       28       GHz         <math>f_{p2}2</math>       28       GHz         <math>f_{p2}2</math>       1.328125       GHz         <math>f_{fe_post_tap_len}</math>       0       UI         <math>ffe_past_tap_len</math>       0       UI         <math>ffe_past_tap_max</math>       0.3       T         <math>ffe_past_tap_max</math>       0.125       Z_p (NEXT)         <math>f_{f}r</math>       0.75       *fb         <math>c(0)</math>       0.6       UI         <math>f_{r}r</math>       0.75       *fb         <math>c(1)</math>       [-0.1:0.05:0]       Z_p (REXT)         <math>z_p (RX)</math>       C_pp       R_d         <math>g_p CC</math>       [-14:1:-3]       dB         <math>f_{r}_{p1}</math>       28       GHz         <math>f_{p2}</math> <td< td=""><td>d(2)       [0:2031]         (d)       [-010050]       [-010050]         N b       4       UI         b_mat(1)       0.5       [-010050]         mas(1)       0.5       [-010050]       [-010050]         <math>g_{0}C</math>       (1441-3)       dB       dH         <math>g_{0}C</math>       (1441-3)       dB       dH       f_b       53.125         ftp:       (149, 20)       0.01       C_d       [1.2e-41.0e-4]         fte.pot.tp.pl.en       0       UI       C_d       [1.2e-41.0e-4]         fte.pot.tp.lmax       0.3       [-1.2e-41.0e-4]       L_s       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-1.2e-4]       [-2.2e]       [0.3e-40.3e-4]       [-2.2e]       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-2.2e]       [0.3e-40.3e-4]       [-2.2e]       [0.12, 0.1]       [-2.2e]       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-2.2e]       [0</td><td><math display="block">\begin{array}{c c c c c c c c c c c c c c c c c c c </math></td><td><math display="block">\begin{array}{c c c c c c c c c c c c c c c c c c c </math></td><td>d-3         (0.030-31)         (0.030-31)           (43)         (0.030-31)         (0.030-31)           (43)         (0.030-31)         (0.030-31)           (10)         (14)</td></td<></td></tr<>	c(-2)         [0:.02:0.1]           c(1)         [-0.1:0.05:0]           N_b         4         UI           b_max(1)         0.5 $\Box$ b_max(2N_b)         0.2 $\Box$ g_DC         [-14:1:-3]         dB           f_z         12.58         GHz           f_p1         20         GHz           f_p2         28         GHz           g_DC_HP         [-3:1:0]         GHz           f_f_PPZ         1.328125         GHz           ffe_pre_tap_len         0         UI           Include PCB         1         logical           ffe_tap_step_size         0         UI           include PCB         1         logical           ffe_tap_max         0.3         O           ffe_post_tap1_max         0.3         O           ffe_backoff         0         O           c(0)         0.6         C(-1)         Co:0:0:0]           c(-1)         [-0.3:0.02:0]         C(-2)         Ci:0:0:0:1]           c(1)         [-0.1:0.05:0]         O         UI           b_max(1)         0         UI         D           b_max(1)	$c(2)$ [0:02:0.1] $(1)$ [0.1:0.05:0] $N_{b}b$ 4       UI $b_{max(2,N,b)}$ 0.2 $g_{DC}$ [4:4:1:-3]       dB $f_{p1}2$ 28       GHz $f_{p2}2$ 28       GHz $g_{DC}$ [4:4:1:-3]       dB $f_{p2}2$ 28       GHz $f_{p2}2$ 28       GHz $f_{p2}2$ 28       GHz $f_{p2}2$ 28       GHz $f_{p2}2$ 1.328125       GHz $f_{fe_post_tap_len}$ 0       UI $ffe_past_tap_len$ 0       UI $ffe_past_tap_max$ 0.3       T $ffe_past_tap_max$ 0.125       Z_p (NEXT) $f_{f}r$ 0.75       *fb $c(0)$ 0.6       UI $f_{r}r$ 0.75       *fb $c(1)$ [-0.1:0.05:0]       Z_p (REXT) $z_p (RX)$ C_pp       R_d $g_p CC$ [-14:1:-3]       dB $f_{r}_{p1}$ 28       GHz $f_{p2}$ <td< td=""><td>d(2)       [0:2031]         (d)       [-010050]       [-010050]         N b       4       UI         b_mat(1)       0.5       [-010050]         mas(1)       0.5       [-010050]       [-010050]         <math>g_{0}C</math>       (1441-3)       dB       dH         <math>g_{0}C</math>       (1441-3)       dB       dH       f_b       53.125         ftp:       (149, 20)       0.01       C_d       [1.2e-41.0e-4]         fte.pot.tp.pl.en       0       UI       C_d       [1.2e-41.0e-4]         fte.pot.tp.lmax       0.3       [-1.2e-41.0e-4]       L_s       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-1.2e-4]       [-2.2e]       [0.3e-40.3e-4]       [-2.2e]       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-2.2e]       [0.3e-40.3e-4]       [-2.2e]       [0.12, 0.1]       [-2.2e]       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-2.2e]       [0</td><td><math display="block">\begin{array}{c c c c c c c c c c c c c c c c c c c </math></td><td><math display="block">\begin{array}{c c c c c c c c c c c c c c c c c c c </math></td><td>d-3         (0.030-31)         (0.030-31)           (43)         (0.030-31)         (0.030-31)           (43)         (0.030-31)         (0.030-31)           (10)         (14)</td></td<>	d(2)       [0:2031]         (d)       [-010050]       [-010050]         N b       4       UI         b_mat(1)       0.5       [-010050]         mas(1)       0.5       [-010050]       [-010050] $g_{0}C$ (1441-3)       dB       dH $g_{0}C$ (1441-3)       dB       dH       f_b       53.125         ftp:       (149, 20)       0.01       C_d       [1.2e-41.0e-4]         fte.pot.tp.pl.en       0       UI       C_d       [1.2e-41.0e-4]         fte.pot.tp.lmax       0.3       [-1.2e-41.0e-4]       L_s       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-1.2e-4]       [-2.2e]       [0.3e-40.3e-4]       [-2.2e]       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-2.2e]       [0.3e-40.3e-4]       [-2.2e]       [0.12, 0.1]       [-2.2e]       [0.12, 0.1]         fte.pot.tp.lmax       0.3       [-2.2e]       [0	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	d-3         (0.030-31)         (0.030-31)           (43)         (0.030-31)         (0.030-31)           (43)         (0.030-31)         (0.030-31)           (10)         (14)		

Ls: 100pH, 120pH

Pkg: no pth, [2,6,8]mm, 92.5OHM

filter and Eq

0.75

0.6

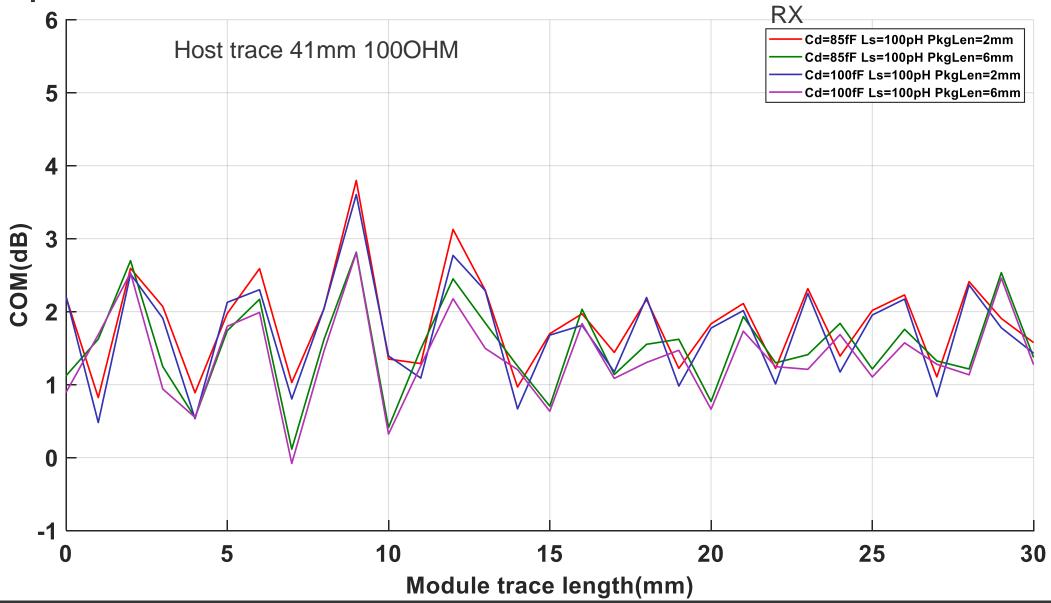
[-0.3:0.02:0]

f\_r c(0)

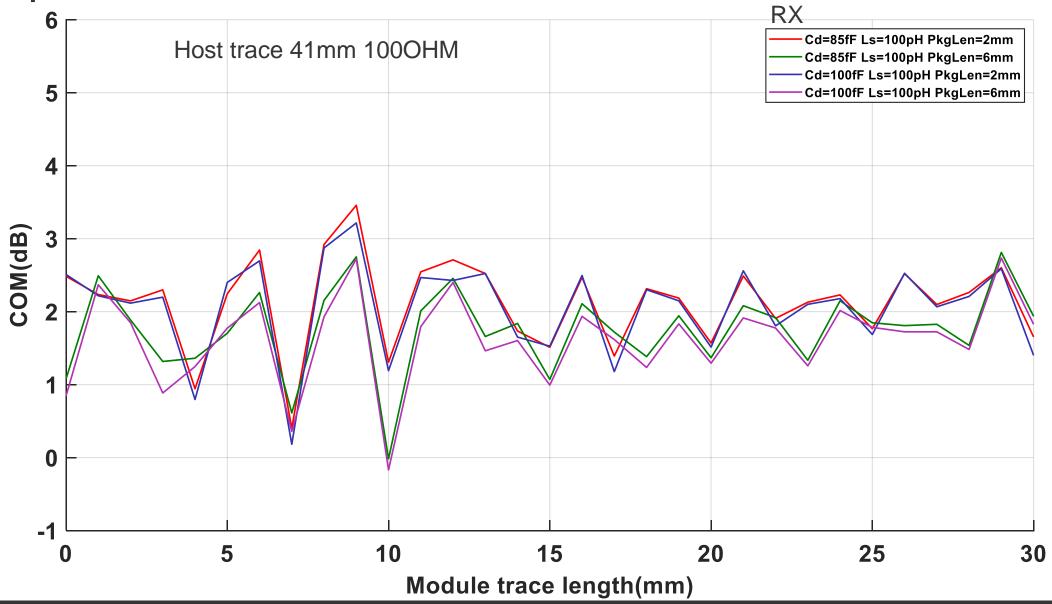
c(-1)

\*fb

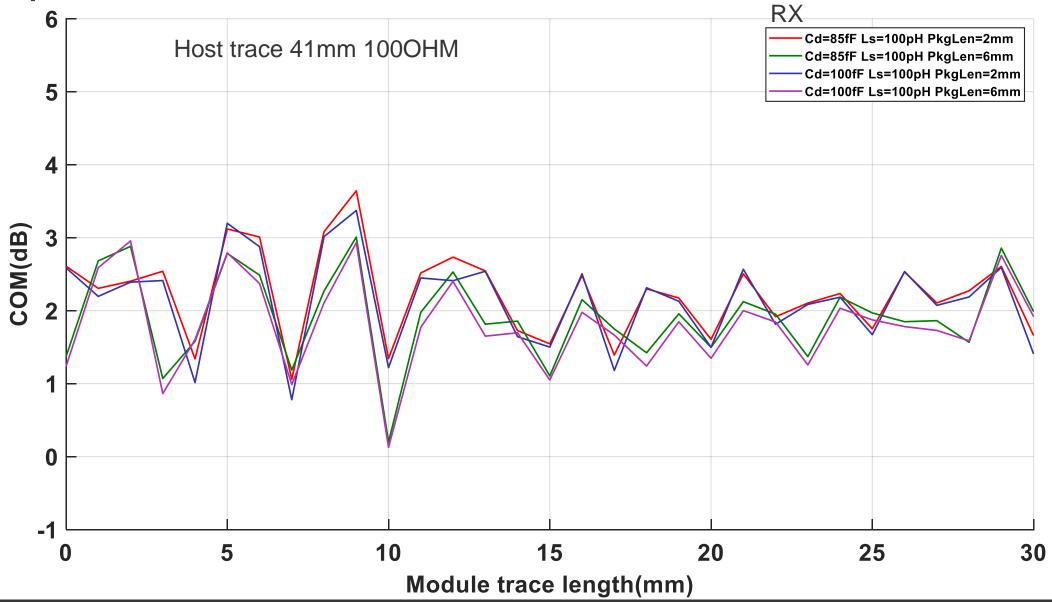
5-tap FFE end to end COM



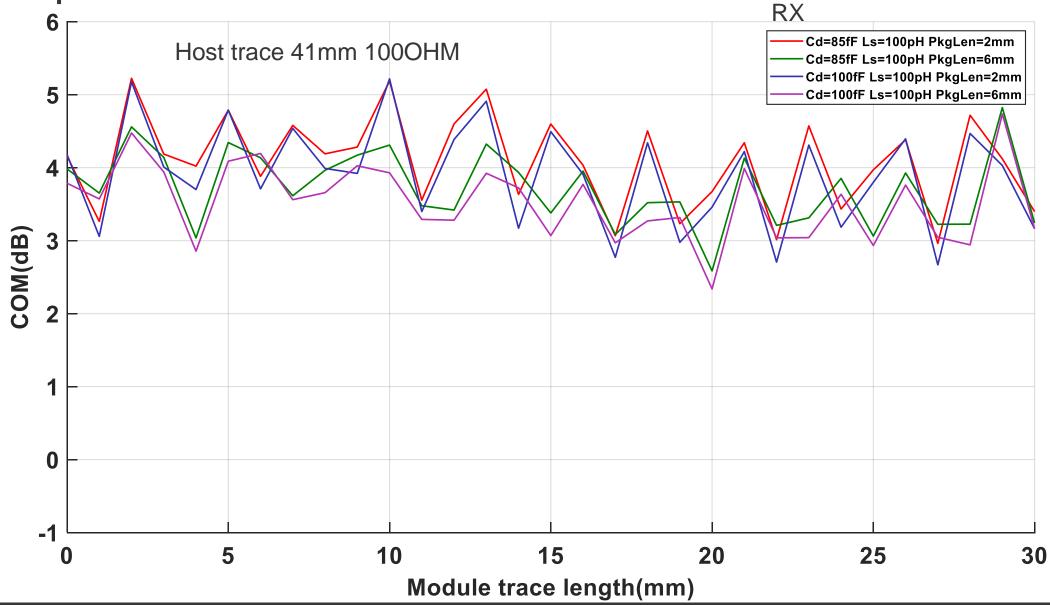
4-tap DFE end to end COM



7-tap DFE end to end COM



12-tap DFE end to end COM



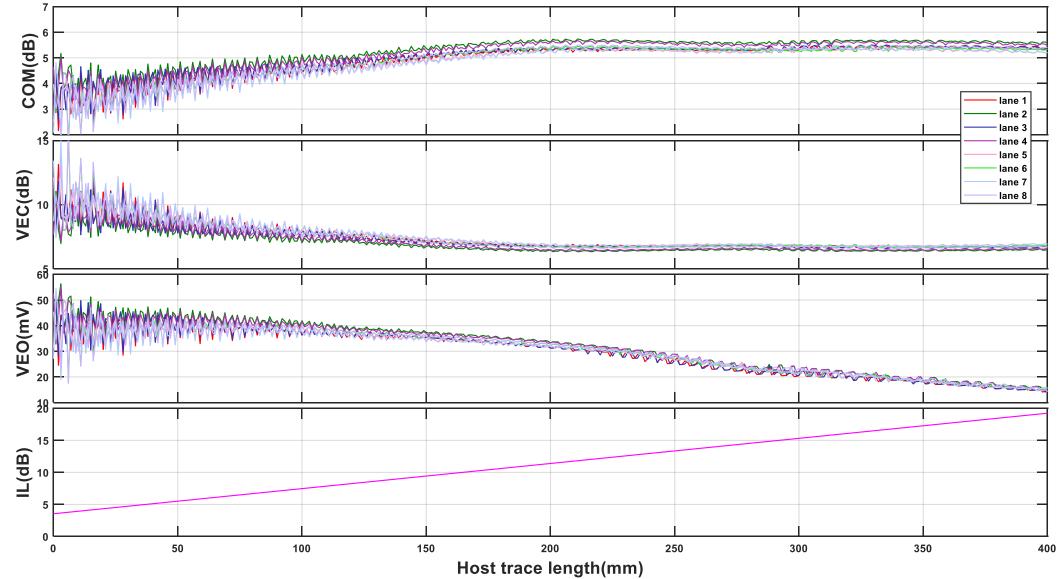
		filter and Eq		End to	and CON	lonro	nadehaat					
	f_r	0.75	*fb				causheel					
	c(0)	0.6		End to end COM spreadsheet								
	c(-1) c(-2)	[-0.3:0.02:0]	++	The end to end COM is calculated with the Tx								
	c(-2)	[-0.1:0.05:0]										
	N b	4	UI	EID top woight	FIR tap weights locked to the optimized							
	b max(1)	0.5		FIR tap weight	s locked to the optil							
	b_max(2N_b)	0.2		unduna fuene the								
	g_DC	[-14:1:-3]	dB	values from the	e previous TP1a sin	nulations.						
4/7/12-tap [		12.58	GHz		-		· · · · · · · · · · · · · · · · · · ·					
	i_br	20	GHz		Table 024 4 server atom	Noise, jitter						
	f_p2	28 [-3:1:0]	GHz		Table 93A-1 parameters		sigma Bl	0.01	UI			
	g_DC_HP f HP PZ	1.328125	GHz	Parameter	Setting	Units	sigma_RJ	0.01	0			
	ffe pre tap len	0	UI	fb	53.125	GBd	A DD	0.02	UI			
	ffe_post_tap_len	0	UI					8 205 00	VANCUS			
	Include PCB	1	logical	f_min	0.05	GHz	eta_0	8.20E-09	V^2/GHz			
	ffe_tap_step_size	0		Delta f	0.01	GHz	SNR TX	33	dB			
	ffe_main_cursor_min	0.7						0.05				
	ffe_pre_tap1_max	0.3		C_d	[1.2e-4 1.0e-4]	nF	R_LM	0.95				
	ffe_post_tap1_max	0.3		Ls	[0.12, 0.1]	nH	I	I	1			
	ffe_tapn_max	0.125		 C b	[0.3e-4 0.3e-4]	nE						
	ffe_backoff	0			·	nF	-					
		filter and Eq		z_p select [1]			Table 93A–3 parameters					
	<u>f_r</u>	0.75	*fb	z_p (TX)	[11.5 11.5; 1.8 1.8 ]	mm	Parameter	Setting	Units			
	c(0)	0.6					package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]				
	c(-1)	[-0.3:0.02:0]	_	z_p (NEXT)	[00; 00]	mm	package_tl_tau	6.1400E-03	ns/mm			
	c(-2) c(1)	[0:.02:0.1] [-0.1:0.05:0]	_	z_p (FEXT)	[11.5 11.5; 1.8 1.8 ]	mm	package_Z_c	[87.5 92.5 ; 92.5 92.5 ]	Ohm			
	N b	0	UI	z_p (RX)	[22;00]	mm						
	b_max(1)	0					Т	able 92–12 parameters	-			
	b_max(2N_b)	0		C_p	[0.87e-4 0.87e-4]	nF	Parameter	Setting				
	g_DC	[-14:1:-3]	dB	R O	50	Ohm	board tl gamma0 a1 a2	[0 3.8206e-04 9.5909e-05]				
5-tap FFE	<u>f_z</u>	18.88	GHz	Rd	[ 50 50]	Ohm	board tI tau	5.790E-03	ns/mm			
Japine	f_p1	28 53.125	GHz GHz	Av	0.415	V	board Z c	[100 92.5]	Ohm			
	f_p2 g DC HP	[-3:1:0]	GHZ					[100 52:0]				
	f HP PZ	0.00025	GHz	A_fe	0.415	V						
	ffe_pre_tap_len	0	UI	A ne	0.6	V						
	ffe_post_tap_len	4	UI									
	Include PCB	1	logical	L	4	_ <b>_</b>						
	ffe_tap_step_size	0		м	32		COM Pass threshold	3	dB			
	ffe_main_cursor_min	0.7					ERL Pass threshold	10 F	dB			
	ffe_pre_tap1_max	0.3		Rx			ERL Pass threshold	10.5	uв			
	ffe_post_tap1_max	0.3 0.125		<b>NX</b>			DER 0	1.00E-05				
	ffe_tapn_max ffe_backoff	0.125	+	Cd: 1	OOFE	T r	6.16E-03	ns				
		ů – – – – – – – – – – – – – – – – – – –		Cu. I	UUIF		0.10E-03					
				Ls: 1	Hq00	FORCE_TR	1	logical				

Ls: 100pH Pkg: no PTH, 6mm, 92.5OHM

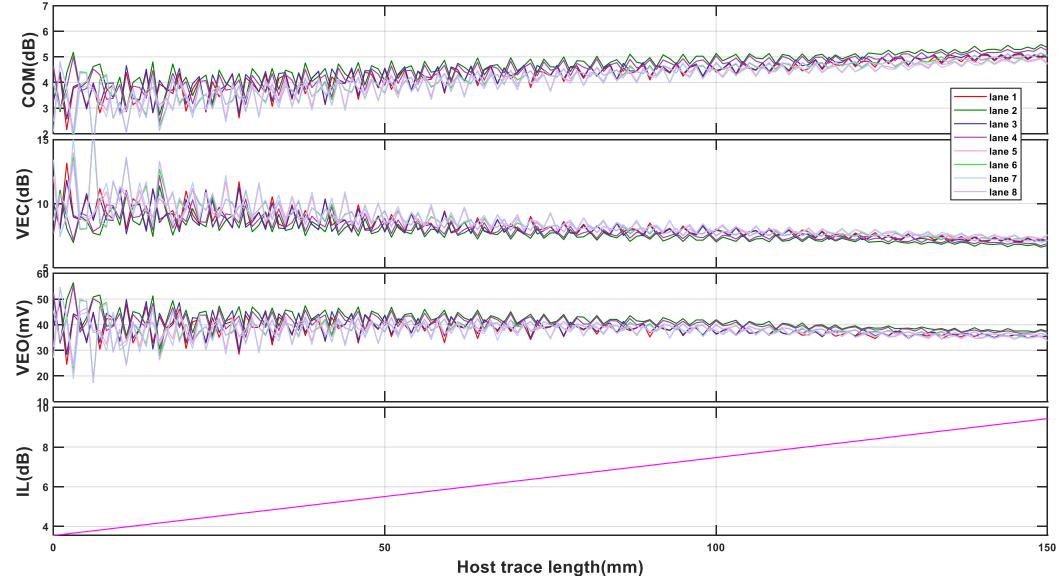
#### Back-up. Selected slides from Dudek\_3ck\_01\_0719

#### Effect of channel length, and connector lane, Capacitor Die model

## Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host

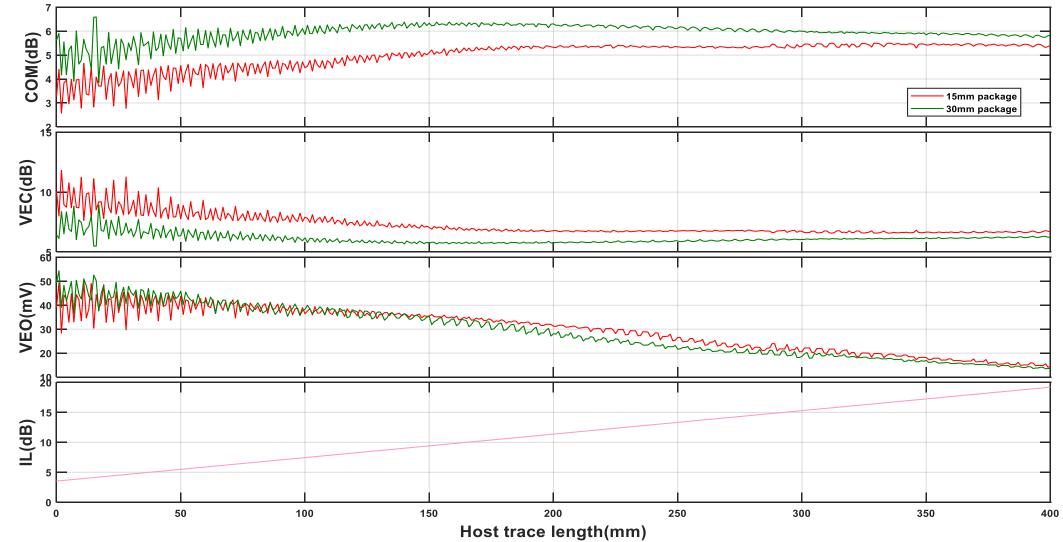


## Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



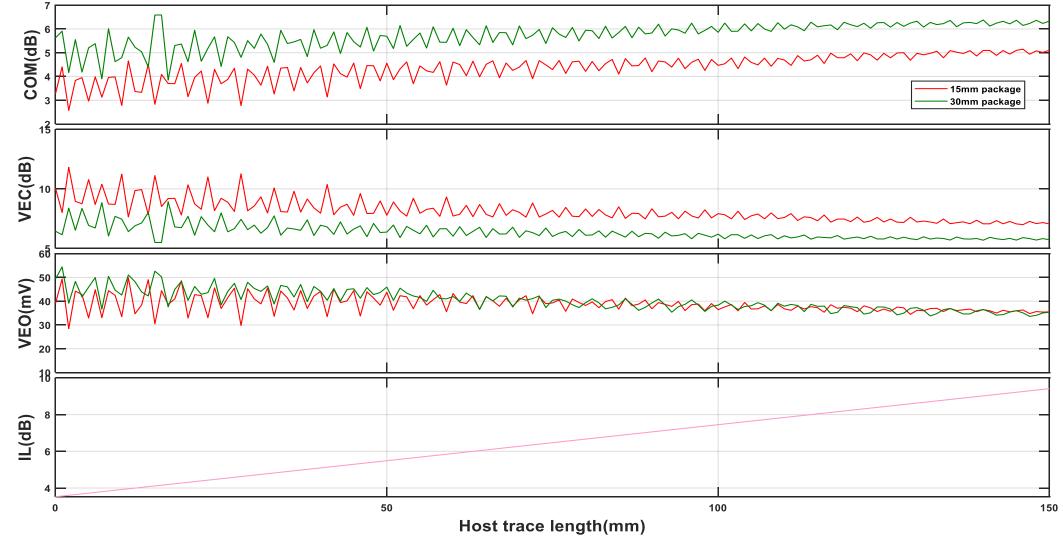
#### Effect of package length -Capacitor die model

## Cd 0.11pF Ls 0pH Cb 0pF 100ohm host



Longer package trace (more loss) is better for COM and VEC although slightly worse for VEO

# Cd 0.11pF Ls 0pH Cb 0pF 100ohm host

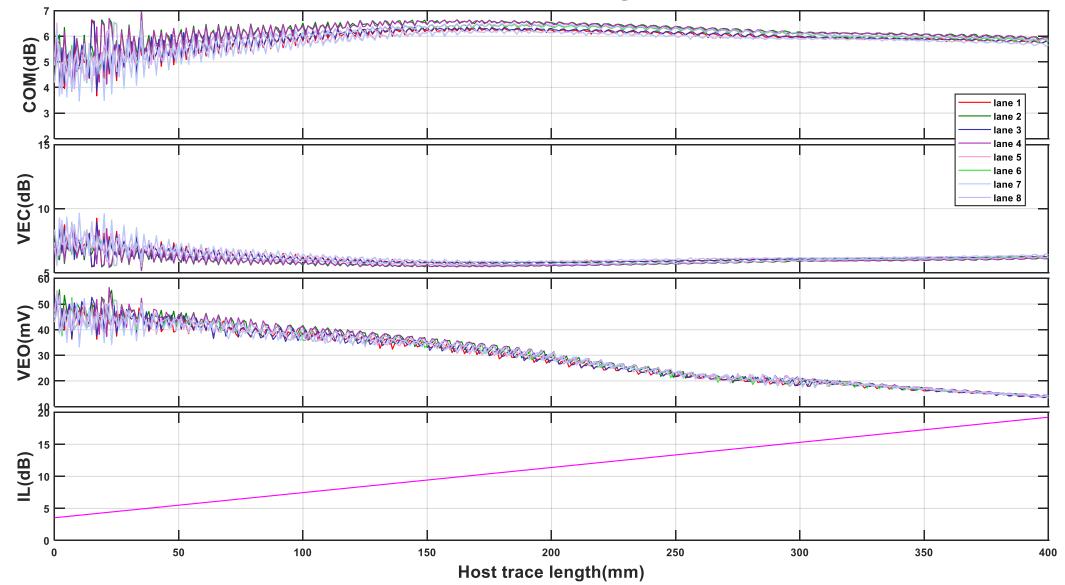


The "good" host trace lengths are different for different package lengths.

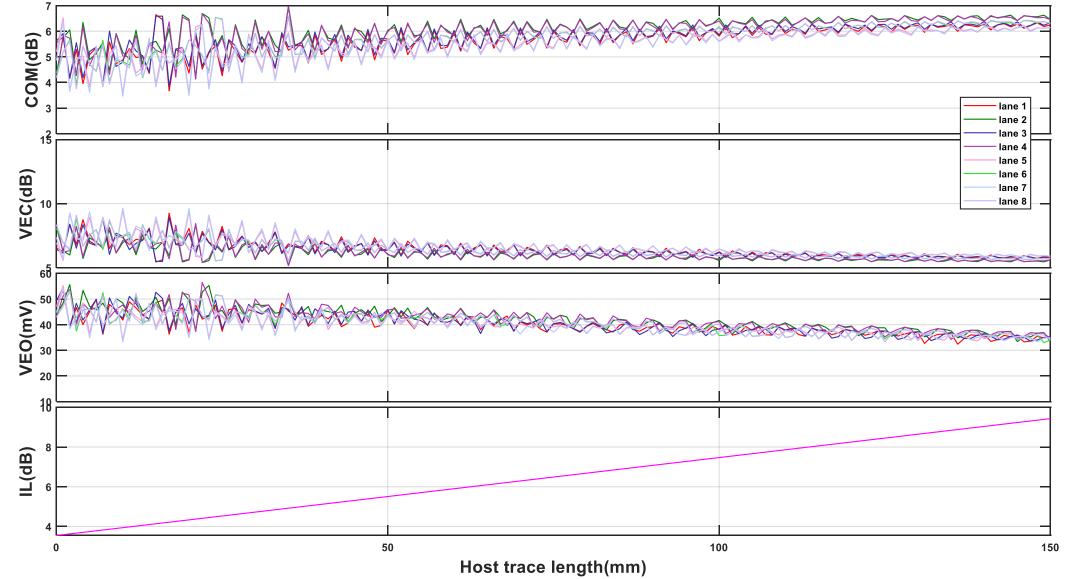
Dudek\_3ck\_01\_0919

#### Effect of channel length, and connector lane on 30mm package

#### Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host -contd



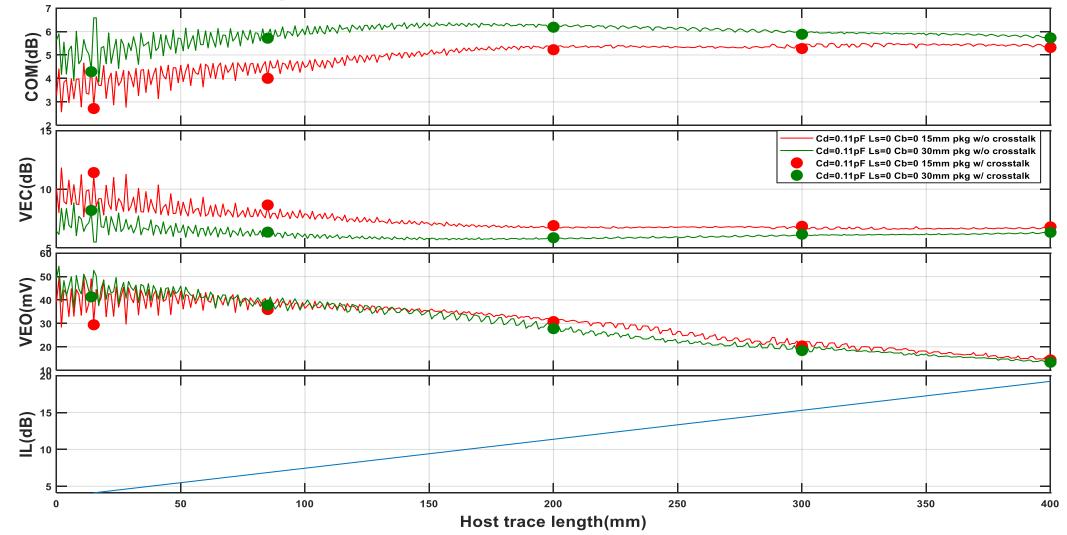
# Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host



#### Effect of crosstalk

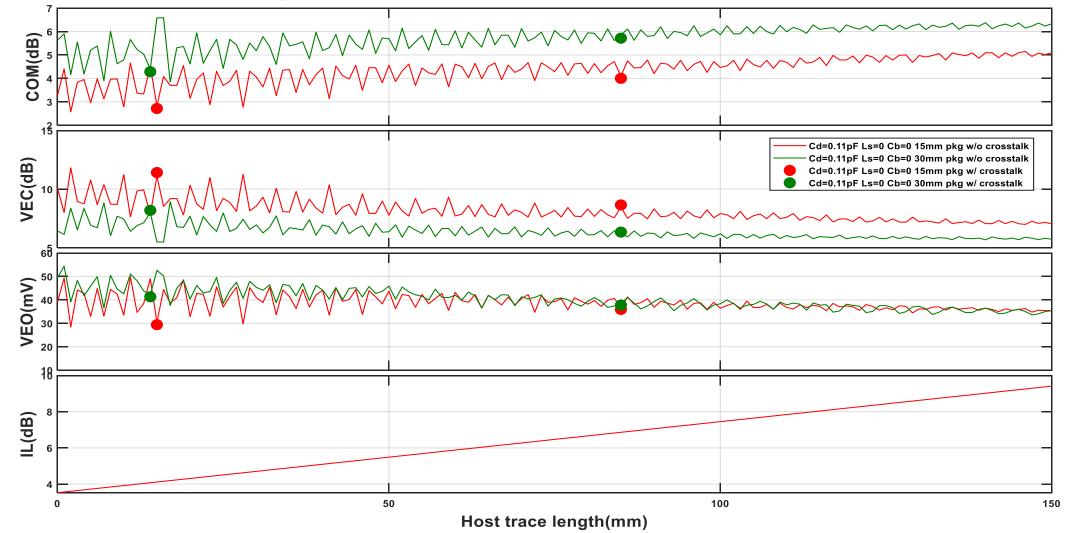
Performance was simulated just at some host lengths with connector crosstalk added

#### 100ohm host impedance



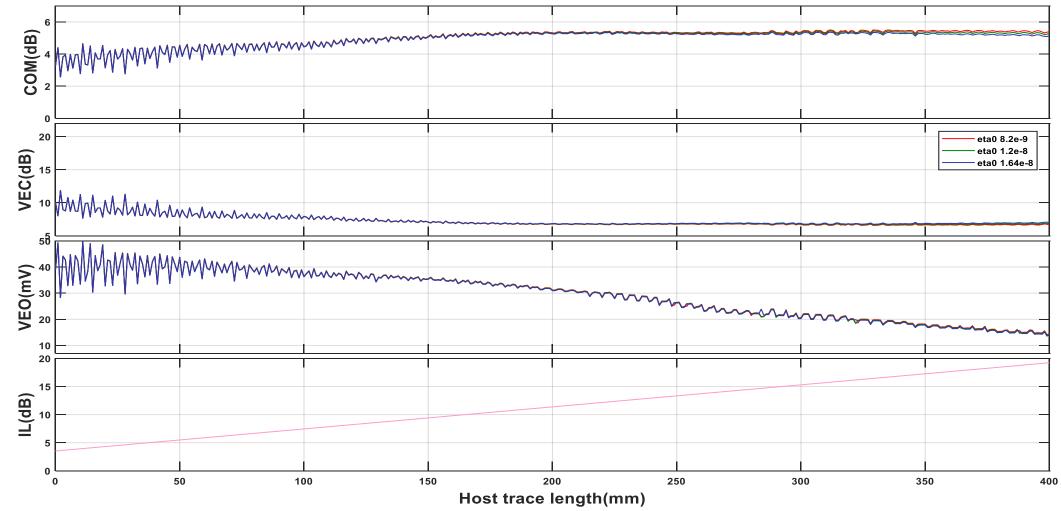
Crosstalk is not a significant degradation for this connector with these trace lengths.

## 100ohm host impedance



#### Effect of Eta0

Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host

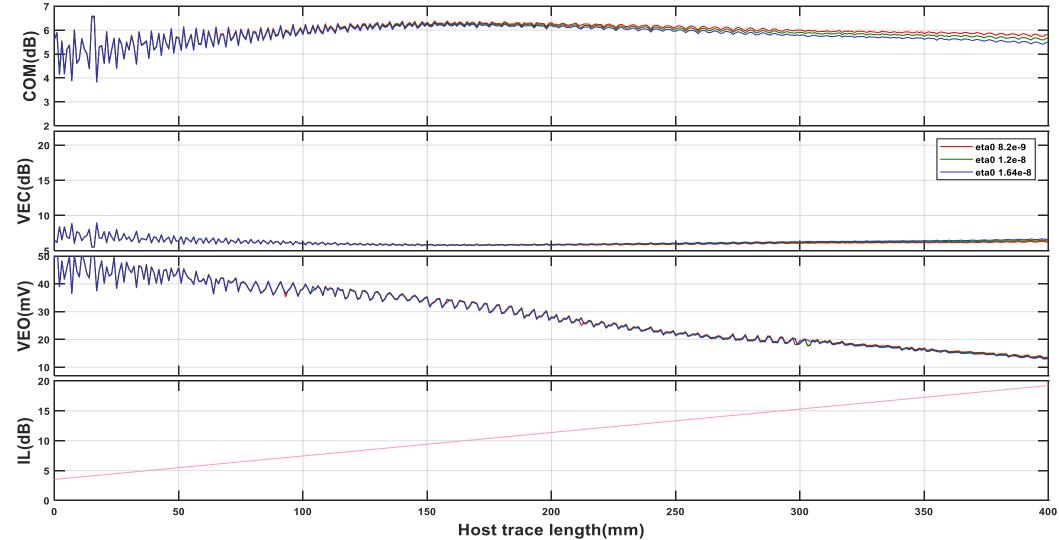


For the short package there is little effect in changing eta\_0 in this range. However the required value for eta\_0 to represent break-in needs to be evaluated.

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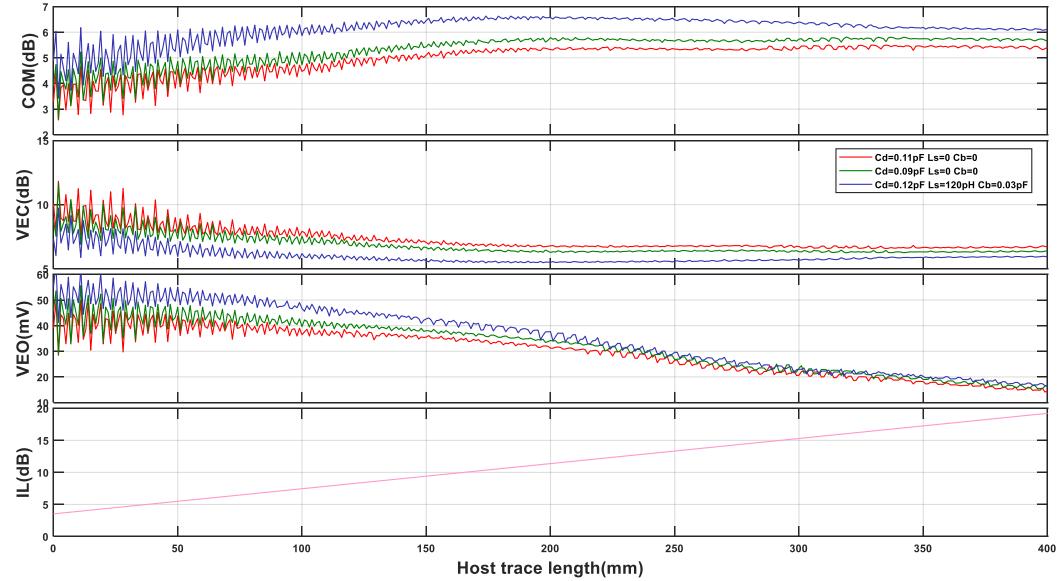
Dudek\_3ck\_01\_0919

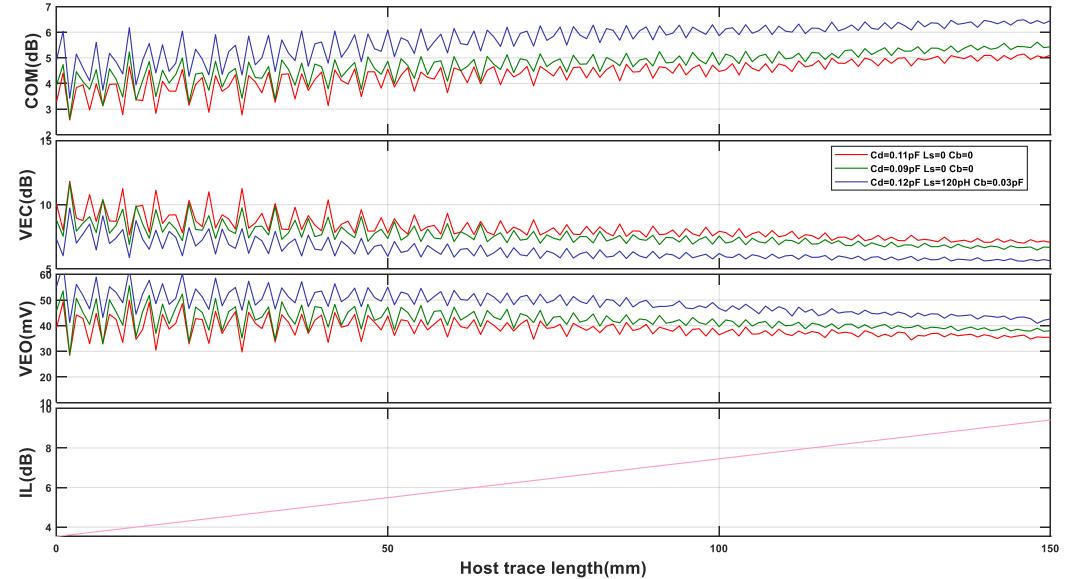
# Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host

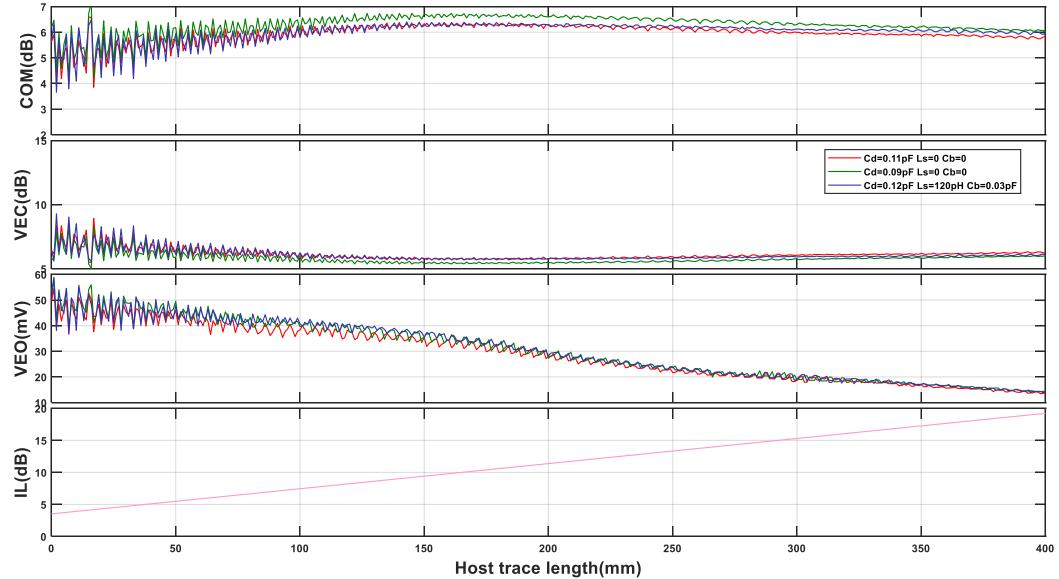


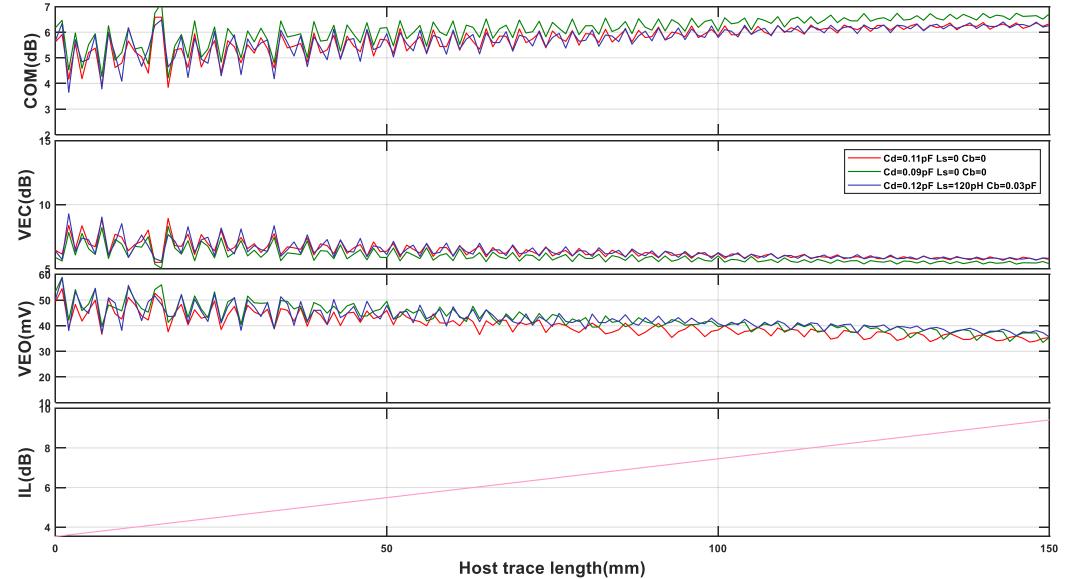
For the longer package changing eta0 in the range evaluated is still not significant even for the higher loss hosts

#### Effect of die model









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