C2M COM Analysis on Short and Long Channels

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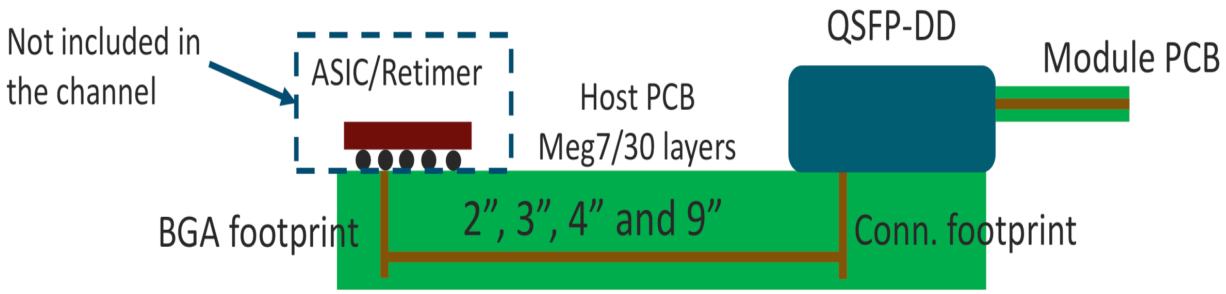
Overview

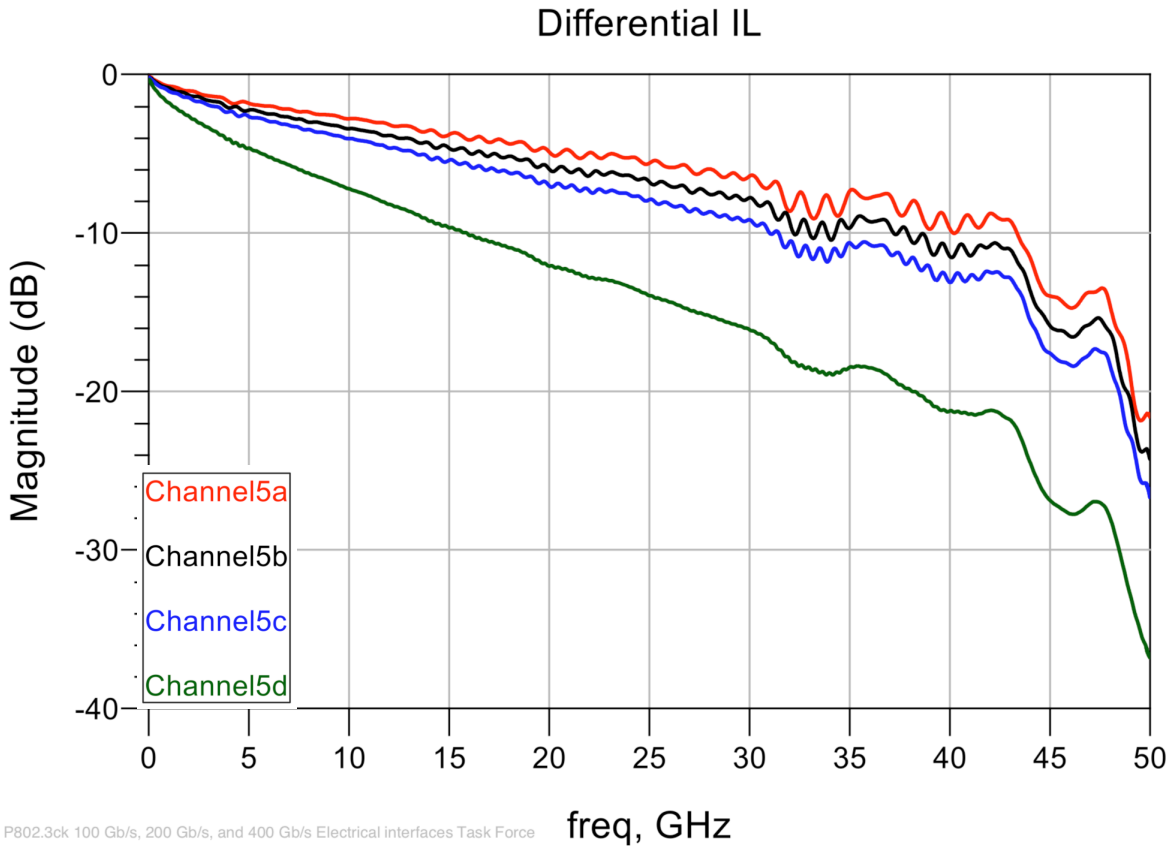
- **Updated analysis uses T-coil model for both host ASIC and module CDR**
  - ASIC and CDR T-coil inductor Ls=0.12 nf
  - ASIC Cd=120 ff but CDR Cd=100 ff
  - Previous COM analysis used T-coil only for ASIC on earlier Lim channels
    - See ghiasi_3ck_02_0719
- **This analysis uses updated lim_3ck_adhoc_02_073119 channels**
  - COM analysis at TP1a/Slicer and TP5/Slicer on min/max loss channels with Lim channels
  - COM analysis at TP4 and TP5 with Yamaichi QSFP56 mated board
- **Best choice for reference equalizer**
- **Summary.**

C2M Channels for Updated Analysis

- **Channel based on [im_3ck_adhoc_02_073119] as shown**
  - 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector with host PCB footprint
  - PCB stackup is 30 layers, 150 mils thick, based on Meg7 material
  - PCB via stub length is modeled as 10 mils
  - Diff pair trace width/spacing is 4.5 mils /8.5 mils
  - ASIC and retimer footprint are simulated with actual BGA ball-out using the same PCB stackup.



- **This analysis uses min loss channel 5a and max loss channel 5d.**



COM Code 2.70 Host-Module TP1a

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[13 31; 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	232	mm
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	232	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	232	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	1										

COM Code 2.70 Host-Module Slicer Input

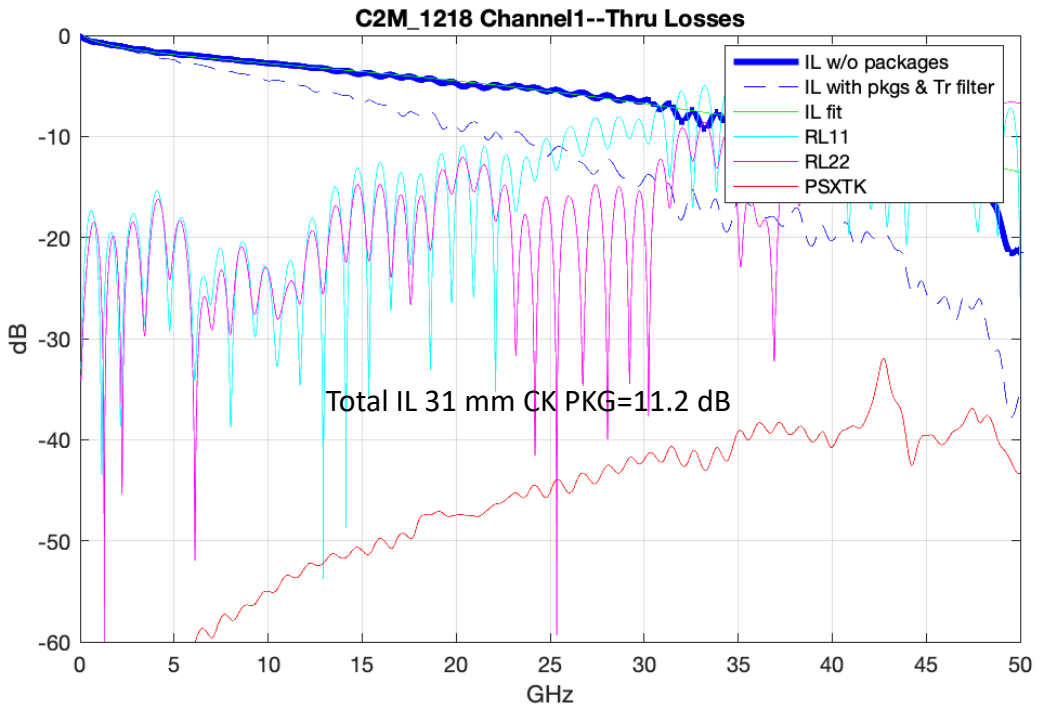
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 1e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0.12]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[13 31; 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	50	mm
z_p (RX)	[2 8 ; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	50	mm
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.9	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.35										
ffe_post_tap1_max	0.35										
ffe_tapn_max	0.2										
ffe_backoff	1										

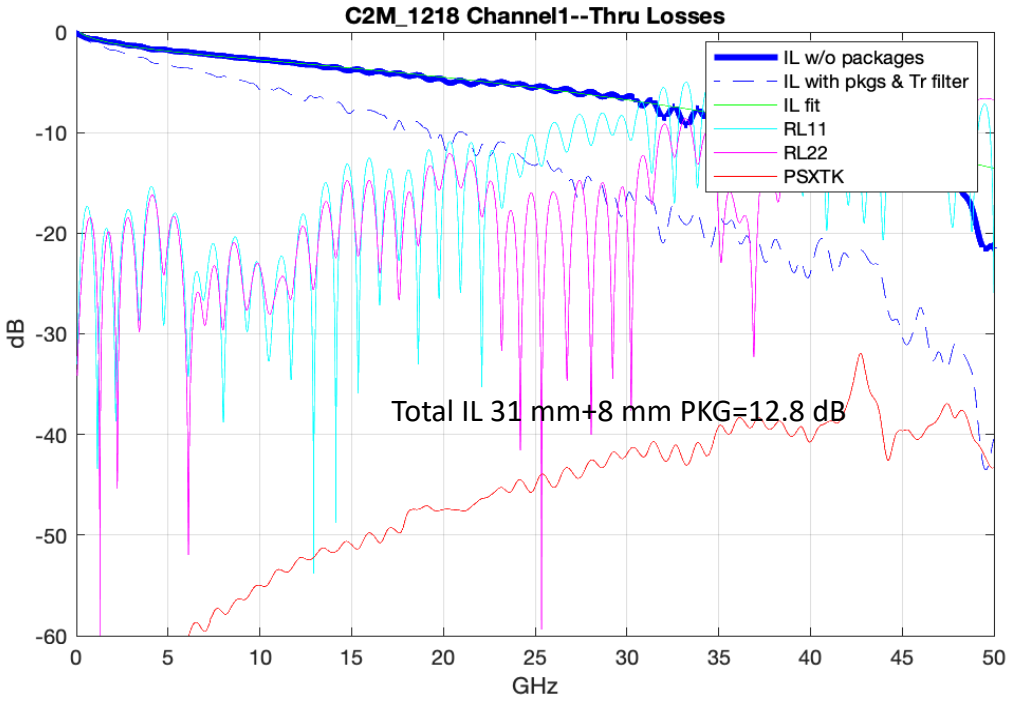
COM Analysis on Lim Channel1 – ASIC to Module

- **Include BGA foot print+(mid length via)+2” host PCB+QSFP-dd connector (new pair) + Legacy QSFP-dd + module PCB.**

TP1a FOM_ILD=0.16, ICN=3.7 mV, ICR=38 dB, ERL11=12.3 dB, ERL22=9.3 dB
5T FFE: COM=2.7 (6.0) dB, EH=21.4 (31.3) mV, VEC=11.5 (6.0) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
5T FFE(4 post)+1DFE: COM=2.4 (5.8) dB, EH=24.9 (37.9) mV, VEC=12.9 (6.2) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
4DFE: COM=2.4 (5.8) dB, EH=24.4 (38) mV, VEC=12.3 (6.2) dB
TX FIR [0.0, -0.08, 0.92, 0] Optimum

Slicer Input FOM_ILD=0.13, ICN=1.44 mV, ICR=38, ERL11=16 dB, ERL22=11.4
5T FFE: COM=1.8 (4.5) dB, EH=11.7 (22.4) mV, VEC=14.6 (7.9) dB
TX FIR [0.04, -0.18, 0.76, 0.02] Optimum
5T FFE(4 post)+1DFE: COM=1.8 (4.6) dB, EH=17.3 (29) mV, VEC=14.6 (7.7) dB
TX FIR [0, -0.1, 0.9, 0] Optimum
4DFE: COM=1.9 (4.6) dB, EH=18 (29.3) mV, VEC=14.2 (7.7) dB
TX FIR [0.02, -0.14, 0.84, -0.02] Optimum





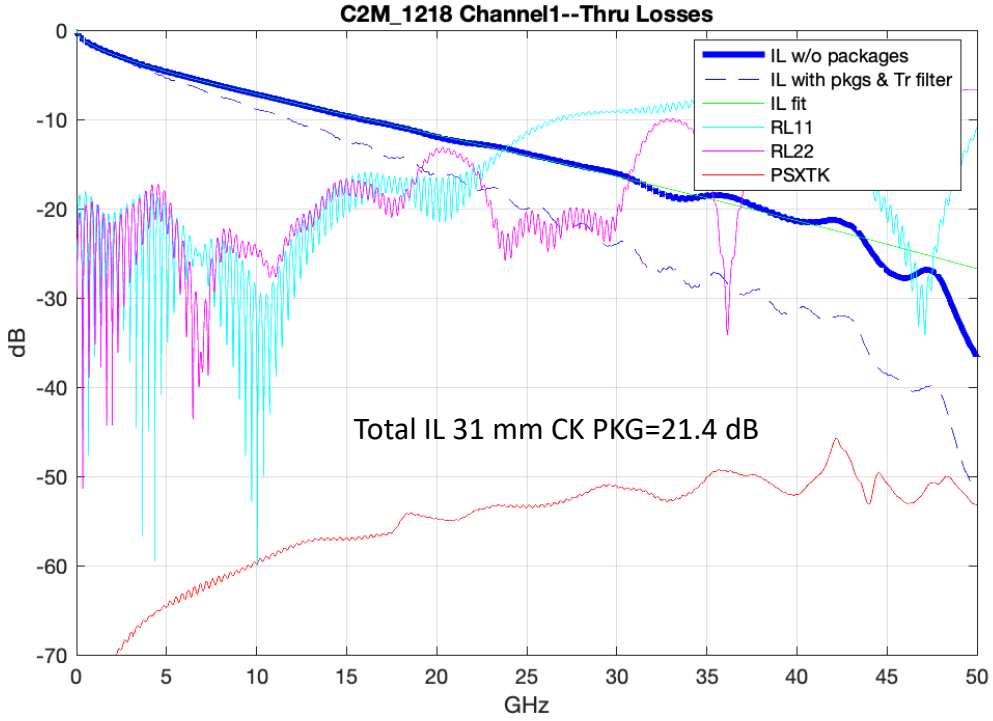
Result in x(y) are for 13(31) mm PKG.

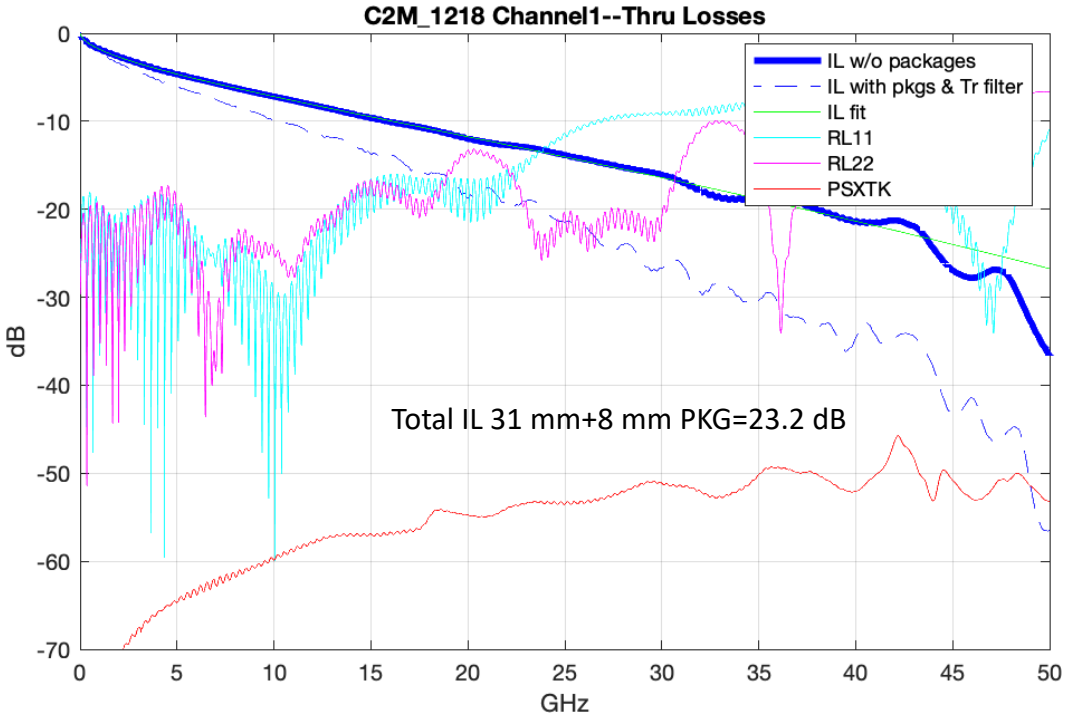
COM Analysis on Lim Channel4 – ASIC to Module

- **Include BGA foot print+(mid length via)+9” host PCB+QSFP-dd connector (new pair) + Legacy QSFP-dd + module PCB.**

TP1a FOM_ILD=0.13, ICN=1.4 mV, ICR=38, ERL11=16 dB, ERL22=11.4 dB
5T FFE: COM=3.0 (5.6) dB, EH=11.2 (14.2) mV, VEC=10.7 (6.4) dB
TX FIR [0.04, -0.18, 0.74, -0.04] Optimum
5T FFE(4 post)+1DFE: COM=4.7 (5.9) dB, EH=21.4 (21.6) mV, VEC=7.6 (6.9) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
4DFE: COM=4.3 (5.8) dB, EH=20.0 (17.1) mV, VEC=8.2 (6.3) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum

Slicer Input FOM_ILD=0.13, ICN=1.44 mV, ICR=38, ERL11=16 dB, ERL22=11.4
5T FFE: COM=2.4 (4.5) dB, EH=7.9 (9.7) mV, VEC=12.2 (7.9) dB
TX FIR [0.04, -0.18, 0.7, -0.08] Optimum
5T FFE(4 post)+1DFE: COM=4.4 (5.2) dB, EH=18.6 (16.9) mV, VEC=8.0 (6.9) dB
TX FIR [0.04, -0.18, 0.76, 0.02] Optimum
4DFE: COM=4.1 (5.0) dB, EH=16.1 (13.6) mV, VEC=8.6 (7.2) dB
TX FIR [0.02, -0.2, 0.76, 0] Optimum





Result in x(y) are for 13(31) mm PKG.

COM 2.70 Module to Host TP5 T-Coil Model (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[1e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	215	mm
z_p (RX)	[0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	215	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	215	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

COM 2.70 Module to Host at Slicer T-Coil Model (CDR PKG 2-8 mm)

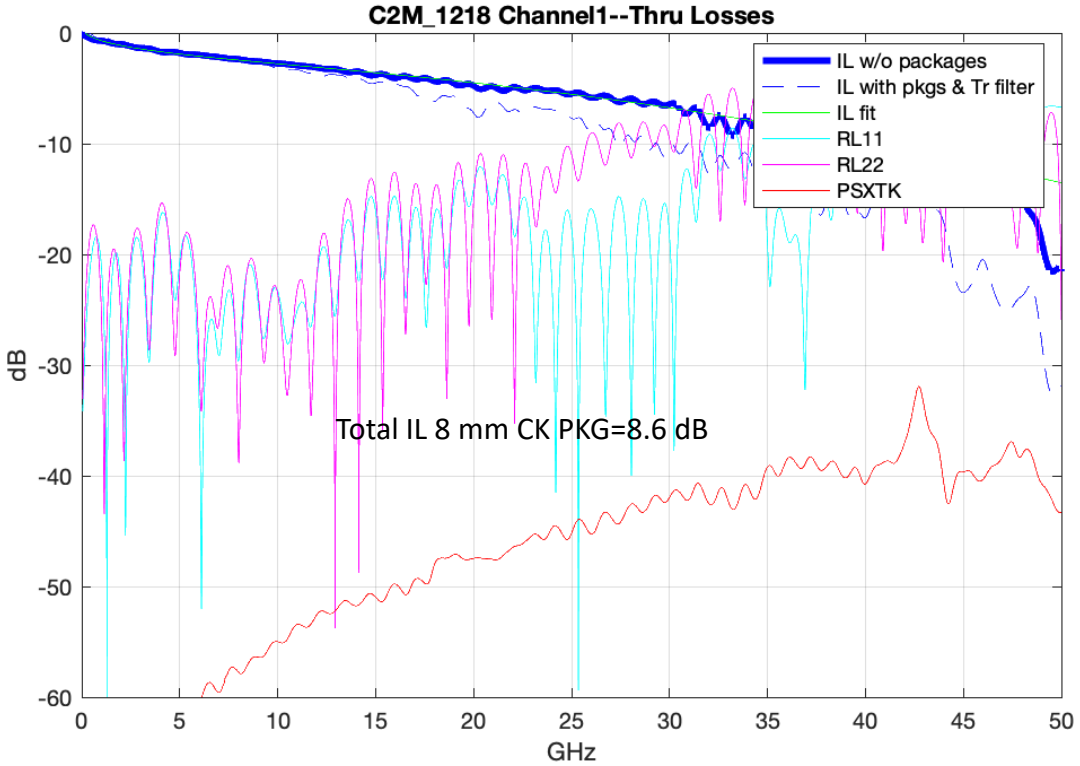
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm
C_d	[1e-4 1.2e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.1 0.12]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8; 0.01 0.01]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8; 0.01 0.01]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8; 0.01 0.01]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	215	mm
z_p (RX)	[13 29; 1.8 1.8]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	215	mm
C_p	[0.65e-4 0.87e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	215	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.8	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	4	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.2										
ffe_backoff	1										

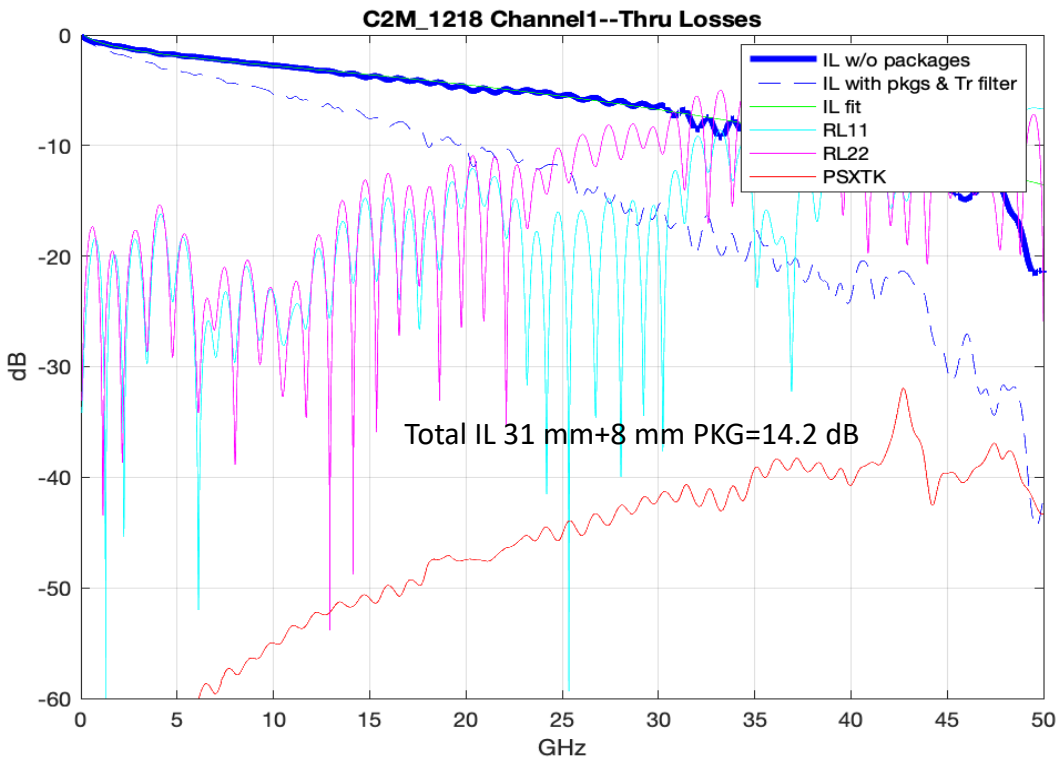
COM Analysis on Lim Channel1 – Module to ASIC at TP5/Slicer

- **Include BGA foot print+(mid length via)+2” host PCB+QSFP-dd connector (new pair) + Legacy QSFP-dd + module PCB.**

TP5 FOM_ILD=0.16, ICN=3.7 mV, ICR=37.8 dB, ERL11=12.3 dB, ERL22=9.3 dB
5T FFE: COM=5.5 (6.0) dB, EH=49.7 (47.5) mV, VEC=6.6 (6.4) dB
TX FIR [0.02, -0.14, 0.82, -0.02] Optimum
5T FFE(4 post)+1DFE: COM=5.0 (5.3) dB, EH=51.6 (50.7) mV, VEC=7.1 (6.7) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
4DFE: COM=5.0 (5.8) dB, EH=51.1 (50.7) mV, VEC=7.1 (6.8) dB
TX FIR [0.02, -0.014, 0.84, 0] Optimum

Slicer Input FOM_ILD=0.16, ICN=3.7 mV, ICR=37.8, ERL11=11.2 dB, ERL22=10.5
5T FFE: COM=1.8 (4.5) dB, EH=12.8 (26.5) mV, VEC=14.4 (7.2) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
5T FFE(4 post)+1DFE: COM=1.7 (5.7) dB, EH=16.4 (32.2) mV, VEC=14.9 (7.1) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
4DFE: COM=1.7 (5.1) dB, EH=16.4 (32.2) mV, VEC=14.9 (7.1) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum





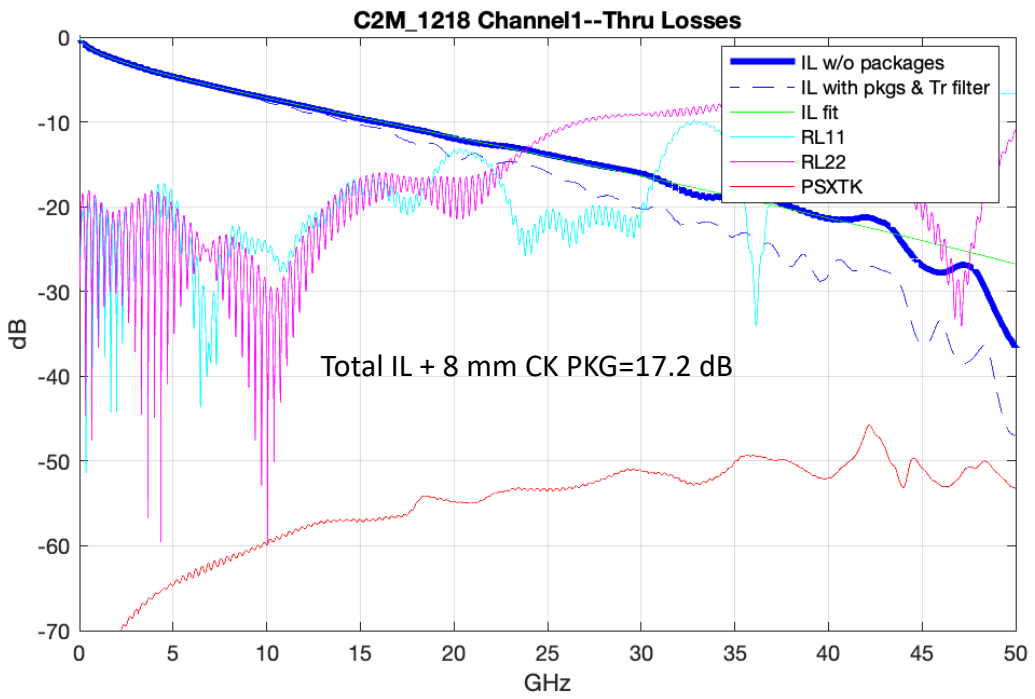
Result in x(y) are for 13(29) mm PKG.

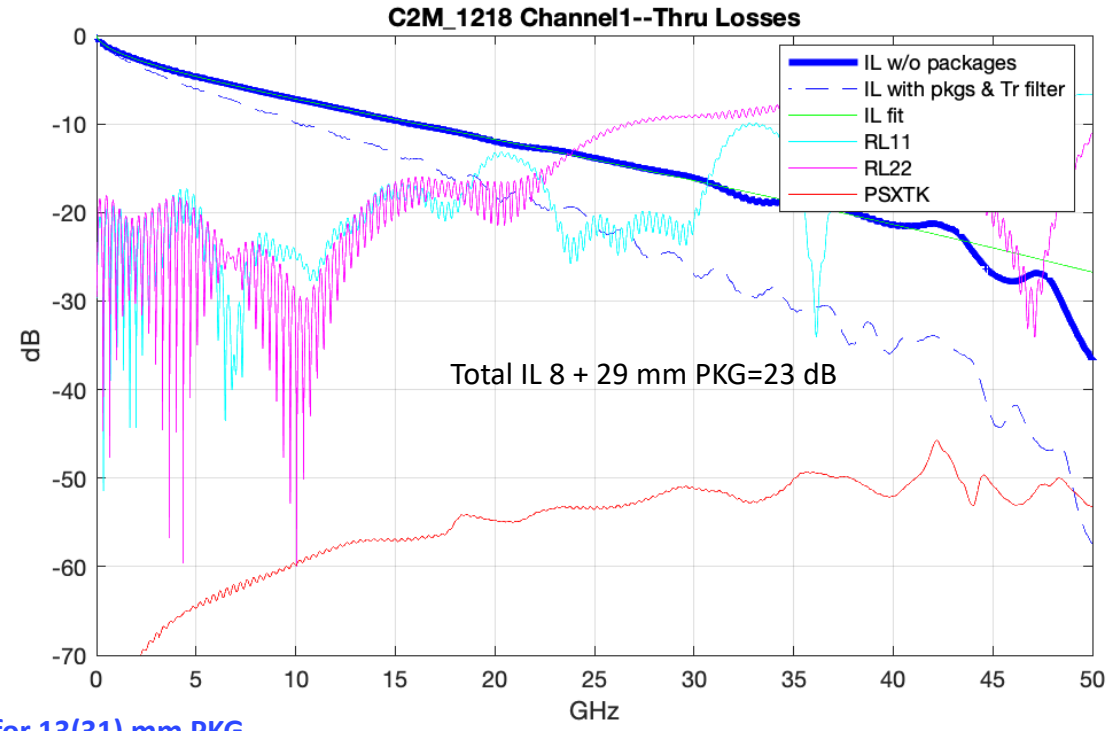
COM Analysis on Lim Channel4 – Module to ASIC at TP5/Slicer

- **Include BGA foot print+(mid length via)+9” host PCB+QSFP-dd connector (new pair) + Legacy QSFP-dd + module PCB.**

TP5 FOM_ILD=0.13, ICN=0.5 mV, ICR=38, ERL11=11.7 dB, ERL22=14.2 dB
5T FFE: COM=5.8 (5.5) dB, EH=20.8 (22.4) mV, VEC=6.2 (6.5) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
5T FFE(4 post)+1DFE: COM=6.3 (5.9) dB, EH=30.2 (26.0) mV, VEC=5.7 (6.1) dB
TX FIR [0.04, -0.18, 0.76, -0.02] Optimum
4DFE: COM=6.2 (5.9) dB, EH=28.2 (24.7) mV, VEC=5.8 (6.1) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum

Slicer Input FOM_ILD=0.13, ICN=1.44 mV, ICR=38, ERL11=11.8 dB, ERL22=15.1
5T FFE: COM=2.5 (5.1) dB, EH=8 (12.7) mV, VEC=11.9 (7.0) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
5T FFE(4 post)+1DFE: COM=4.5 (5.8) dB, EH=18.6 (17.1) mV, VEC=7.6 (6.3) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum
4DFE: COM=4.1 (5.6) dB, EH=16.9 (14.1) mV, VEC=8.5 (6.5) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum



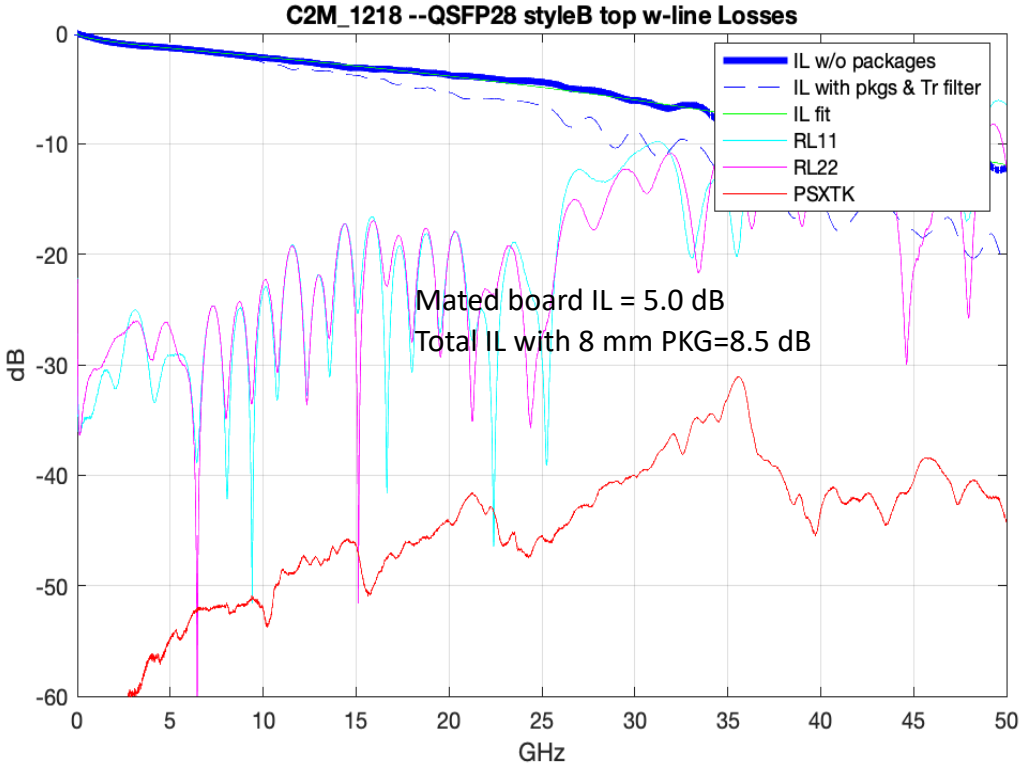


Result in x(y) are for 13(31) mm PKG.

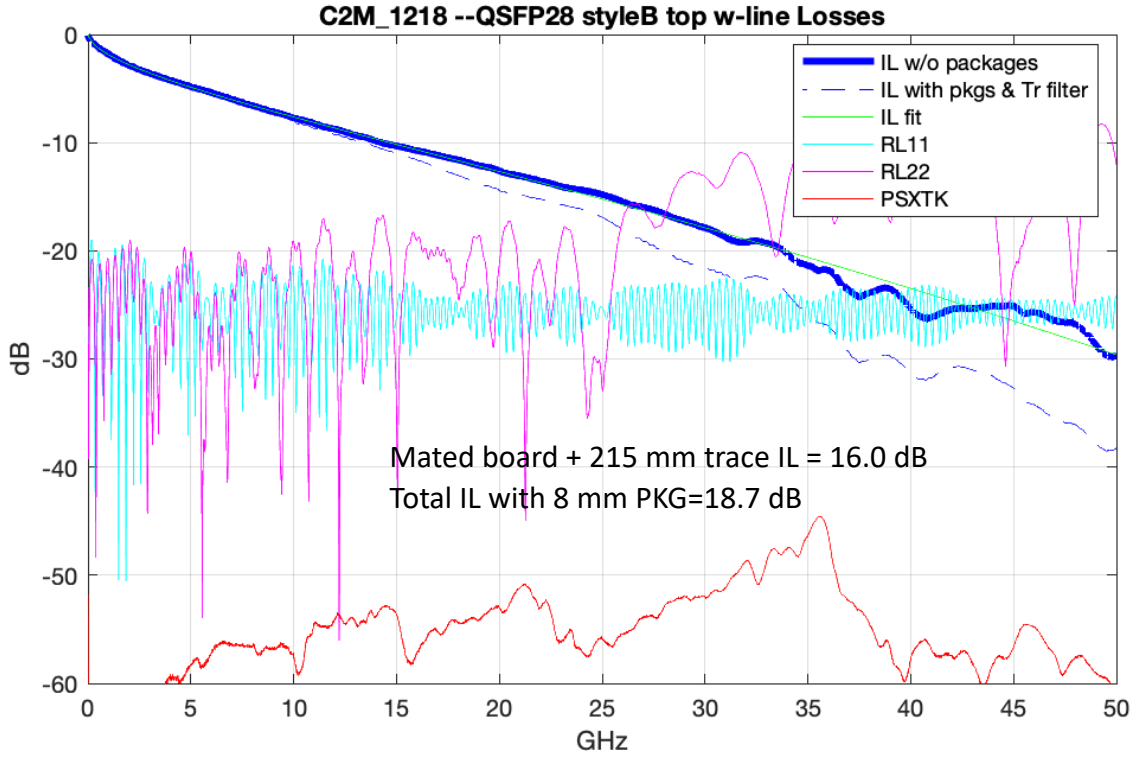
Module-Host Analysis Based on Yamaichi QSFP-56 Mated Boards

- **COM at TP4 channel loss 5.0 dB channel and at TP5 with 215 mm PCB trace has loss of 16 dB.**
  - COM results below with T-Coil model have improved by about 1 compare to RC model shared in ghiasi_3ck_02_0719.

TP4:Min Loss, ILD=0.18, ICN=5.2 mV, ICR=39.5 dB, ERL11=14.6, ERL22=10.9
5T FFE(4 post): COM=5.8 (6.0) dB, EH=53.2 (53.0) mV, VEC=6.3 (6.1) dB
5T FFE+1T DFE: COM=5.2 (5.4) dB, EH=55.1 (53.3) mV, VEC=6.9 (6.7) dB
4T DFE: COM=5.2 (5.4) dB, EH=55.1 (53.0) mV, VEC=6.9 (6.7) dB



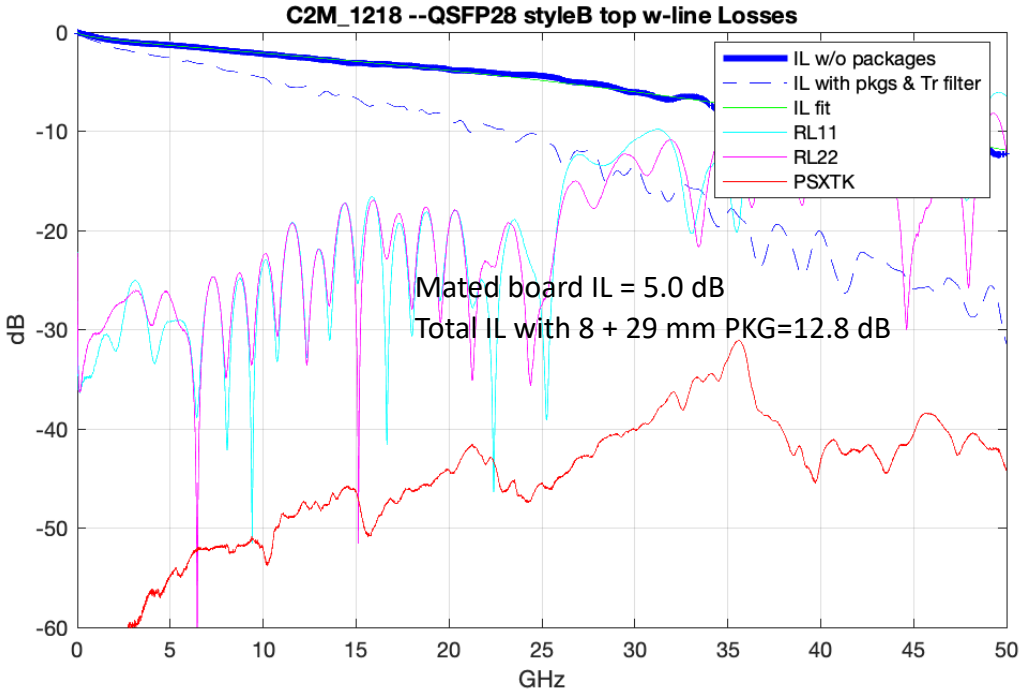
TP5:Max Loss, ILD=0.17, ICN=1.6 mV, ICR=39.1 dB, ERL11=14.6, ERL22=10.7
5T FFE(4 post): COM=6.8 (6.3) dB, EH=21.0 (18.0) mV, VEC=5.3 (5.7) dB
5T FFE+ 1T DFE : COM=6.9 (6.6) dB, EH=19.1 (15.9) mV, VEC=6.3 (6.4) dB
4T DFE: COM=7.0 (6.6) dB, EH=24.2 (26.1) mV, VEC=5.2 (5.5) dB



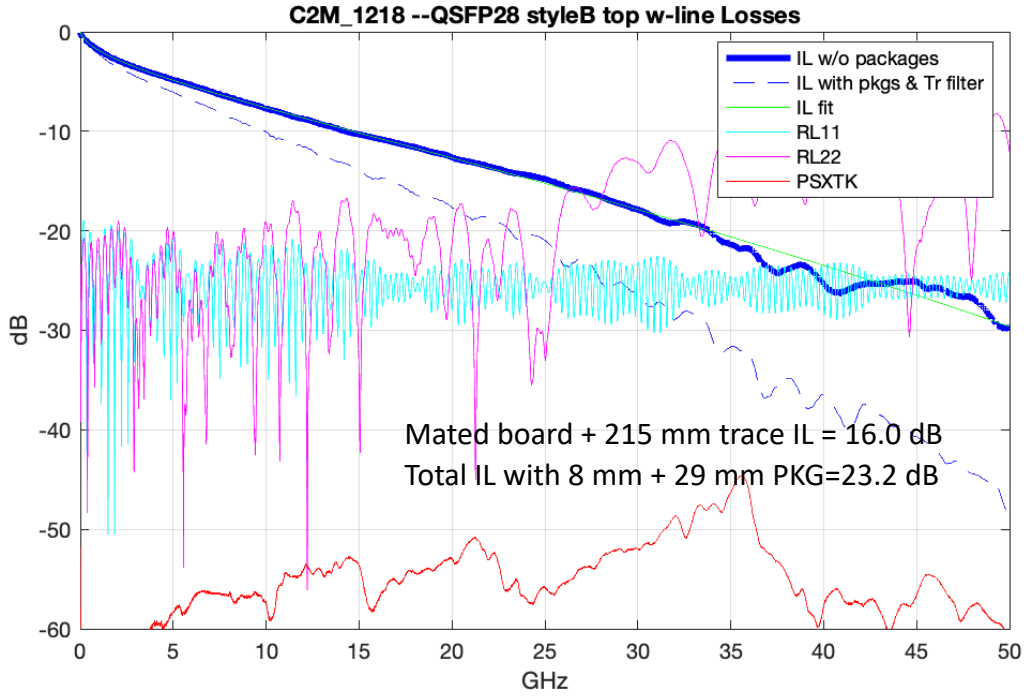
Module-Host Analysis Based on Yamaichi QSFP-56 Mated Boards

- **COM at slicer for min loss (5 dB) channel and max loss channel (16 dB) with addition of 215 mm PCB trace.**

Min Loss, ILD=0.18, ICN=5.2 mV, ICR=39.5 dB, ERL11=14.6, ERL22=11.4
5T FFE(4 post): COM=4.0 (5.3) dB, EH=36.2 (28.0) mV, VEC=8.6 (6.7) dB
5T FFE+1T DFE: COM=3.9 (5.4) dB, EH=35.4 (38.1) mV, VEC=8.8 (6.6) dB
4T DFE: COM=5.2 (5.4) dB, EH=55.1 (53.0) mV, VEC=6.9 (6.7) dB



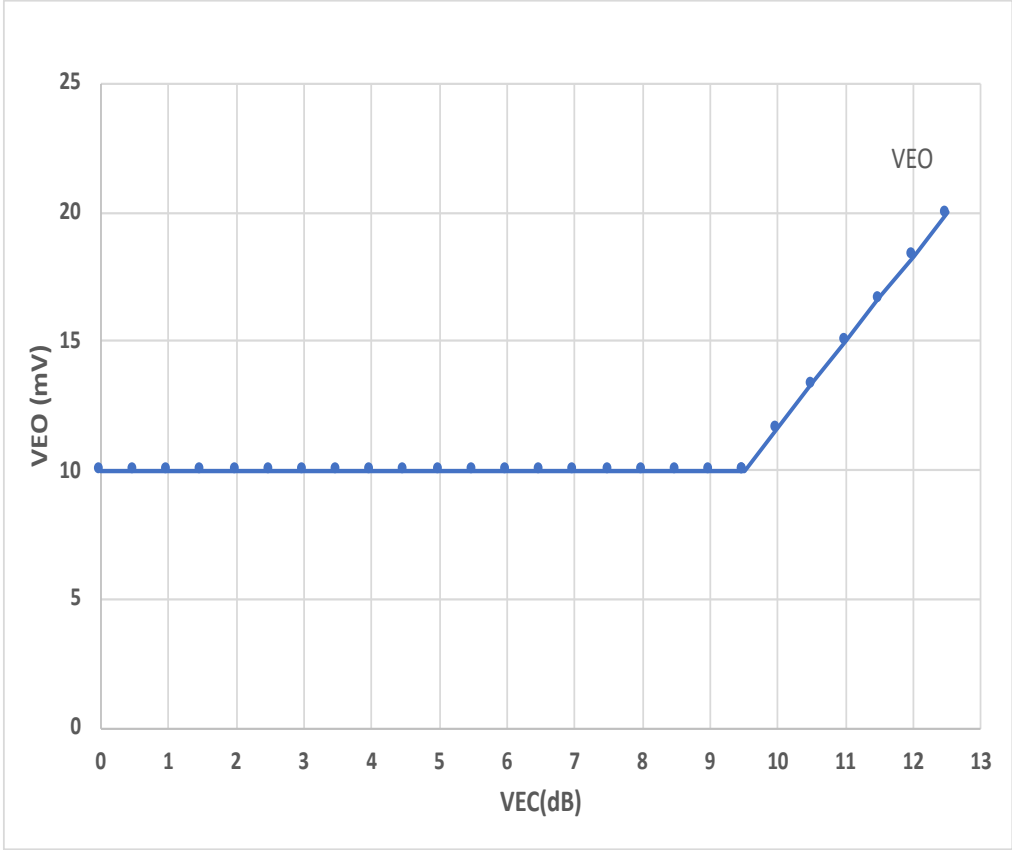
Max Loss, ILD=0.17, ICN=1.6 mV, ICR=39.1 dB, ERL11=14.6, ERL22=11.4
5T FFE(4 post): COM=4.1 (5.1) dB, EH=10.9 (11.4) mV, VEC=8.5 (7.0) dB
5T FFE+ 1T DFE : COM=5.1 (5.9) dB, EH=19.3 (17.5) mV, VEC=7.0 (6.1) dB
4T DFE: COM=4.9 (5.7) dB, EH=18.6 (13.5) mV, VEC=7.3 (6.4) dB



How to Deal with Short Reflective Channels?

- **Short reflective channel can result in a VEC of 12.5+ dB**
  - On the short reflective channels 5T FFE performs as good as 4T DFE and 5T FFE+1TDFE
  - Reducing VEC to a more comfortable range like < 10 dB would require significantly constraining the channel or use 8+ T equalizer, which is beyond C2M power envelope
  - But one these short reflective channels VEC ~12.5 dB the VEO is very large 20+ mV
  - A well designed receiver should be able to operate with couple of dB higher VEC for double of the signal
  - Propose to define min VEO as function of VEC

$$\text{VEO}= \begin{cases} 10\ mV & VEC \le 9.5\ dB \\ VEC\ \frac{10}{3} - 21.667\ mV, & VEC > 9.5\ dB \end{cases}$$



How to Choose C2M Observation Equalizer

- **The observation equalizer needs to be a weak equalizer where the real receiver may have additional capabilities**
  - The 5 tap T spaced is already required by 802.3bs and 802.3cd PAM4 optical PMDs
  - 5 tap T spaced (4 post) is a versatile weak equalizer ideal for signal observation
  - 5 tap FFE already implemented by Keysight and Tek for TDECQ algorithm and can be borrowed for C2M VEO/EW/VEC
  - It Why not duplicate the optics CDR core with 5 tap FFE (+ 1T DFE?) on the electrical side?
- **5T FFE Observation signal equalizer is only to observe TP1a, TP4, and TP5 signals, but real receiver maybe one of several option listed below:**
  - 5T FFE could be used as the real receiver if operating with VEC of ~12.5 dB is acceptable
  - 4T DFE and 5T FFE+1T DFE used as real receiver on most channel will operate with higher margin but on short channels may need to operate with ~ 12.5 dB VEC
  - One may implement 8+ tap FFE or DFE to further lower VEC on short channels but would be power hungry
  - Alternatively one may use 5T FFE with some tail DFE to cancel some of the reflections on short channel
- **FFE inherently preserves the analog signal and will provide better direct correlation than the clipped signals DFE will provide at observations points!**

Summary

- **Receiver considered for this study are 5T FFE, 4T DFE, and 5T FFE+1T DFE**
- **Summary of Lim 7/19 channels simulations at TP1a/TP5 and at slicer input**
  - Updated results are with ASIC and CDR both having T-Coil
  - COM results have improved by ~ 1 dB with T-Coil TX/RX models
  - With improved TX/RX models the 9” channel (~14.8 dB) passes with excellent margin even for weaker 5T FFE
  - Even with improved TX/RX model the 2” channel (~5.9 dB) 3 dB COM fails for all 3 equalizer considered here
- **Given that constraining the channel will be too restrictive need to allow receiver to operate with higher VEC if a minimum eye opening is met**
  - The alternative of defining an equalizer long enough to deal with short channels would be too power hungary
- **As the result in this contribution shows the 4T DFE is not any better than lower power 5T FFE on reflective channels**
  - Given that adopting 8+ tap equalizer is not an option for C2M and 4T DFE offers no advantage on reflective channel the task force should adopt the lower power 5T FFE
  - Some implementation may choose to operate with higher VEC and other may choose longer 8+ taps equalizer to better handle reflective channels
- **C2M TP1, TP4, and TP5 recommended limits based on 5T FFE (4 post) scope reference equalizer**
  - TP1a EH=f(VEC) see page 14, VEC=12.5 dB, EW=TBD
  - TP4 EH=40 mV, VEC=7 dB, EW=TBD
  - TP5 EH=16 mV, VEC=9.5 dB, EW=TBD.