Module on-die termination model for COM

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Supporters

- Please let us know if you wish to support this
- Tom Palkert, MACOM
- Phil Sun, Credo
- Piers Dawe, Mellanox

Overview

- This presentation includes information that has been presented to the small group working on C2M and updates from the August 29th presentation to the small group.
- Aim is to get consensus for a new die termination model for the module chip (CDR/DSP/Retimer)
- Various values for C_d and L_d have been simulated and presented to the small group
 - This presentation focuses on the latest values presented where consensus is closer
 - C_d = 85 fF or 100fF
 - L_d = 100 pH or 120 pH

Motivation

- The die termination model for the ASIC has been updated to include some inductance
 - Gives better COM channel performance without reducing Cd significantly
 - See healey_3ck_adhoc_01_061219
- Apply the same approach in the module on-die termination
- Improve the COM channel performance to keep the reference equalizer simple and low power
- Keep die termination reasonably model simple
- Model does not reflect an actual implementation
 - Actual implementation should give better performance to allow for design margin

Current module on-die termination

- Simple model
- Current values
 - C_d = 85 fF
 - C_p = 75 fF
 - Package trace
 - $Zo = 92.5\Omega$ differential
 - Length 2 8 mm
- C_d includes contributions from die-package interface, bond pad, ESD diodes, output transistors, etc
 - C_d is lower than reality to account for T-coil implementations



Proposed on-die termination

- As per healey_3ck_adhoc_01_061219, split out fraction of C_d that represents die-package interface
- Improve bandwidth and return loss by compensating excess on-die capacitance with an inductor
- Simpler than full T-coil model
- Actual implementation should still give better performance allowing some design margin
- Proposed in healey_3ck_adhoc_01_061219 and presently in COM 2.70 are:





Termination	Rd	Cd	Ls/Ld	Cb	Comment
Host ASIC (slide 4 of healey_3ck_adhoc_061219)	50 Ω	120 fF	120 pH	30 fF	Implemented in COM ver 2.70

Transmission line model



COM TRL parameters (same as COM version 2.70)



• TRL loss is ~ 0.108 dB/mm

m1

freq=26.56GHz

- Same α_1, α_2 , and τ parameters as present COM host package TRL model

Table 93A–3 parameters				
Setting	Units			
0 0.0009909 0.0002772]				
6.141E-03	ns/mm			
87.5 87.5 ; 92.5 92.5]	Ohm			
	Table 93A–3 parame Setting 0 0.0009909 0.0002772] 6.141E-03 [87.5 87.5 ; 92.5 92.5]			

Die Termination Only Simulation Circuit



- Three cases were considered:
 - 1. $C_d = 85$ fF and sweeping L_d from 0 150 pH in steps of 25 pH
 - 2. $C_d = 100 \text{ fF}$ and sweeping L_d from 0 150 pH in steps of 25 pH
- L_d having values > 150 pH becomes challenging and likely not required from a performance perspective
 - Needs a more complex model

Simulated S21 and S22 Performance with Cd=85fF



S22 Response

- For C_d = 85 fF case L_d in range of 100 125 pH is suitable depending upon targeted performance parameter
- Lower L_d values (i.e. L_d in 50 75 pH range) do provide higher bandwidths but have other undesirable effects

Simulated S21 and S22 Performance with Cd=100fF



- For $C_d = 100$ fF case $L_d = 100 150$ pH is suitable depending upon targeted performance parameter
- L_d lower than 75 pH are not recommended although termination bandwidth would be larger

Complete Package Model



- Four termination cases simulated
 - C_d = 85 and 100 fF
 - $L_d = 100 \text{ and } 120 \text{ pH}$
- For each of the termination cases:
 - TRL lengths of 2mm to 8mm were considered in steps of 2mm
 - TRL had 92.5 Ω nominal impedance with α_1 = 9.909E-4 and α_2 = 2.772E-4

Package simulations for Cd = 85 fF (1/2)



Package + Die simulations for Cd = 85 fF





Package simulations for Cd = 100 fF (1/2)





Package + Die simulations for Cd = 100 fF

Package + Die simulation observations (1/2)

2 mm CDR package + die performance:

4 mm CDR package + die performance:

6 mm CDR package + die performance:

8 mm CDR package + die performance:

Case	Cd (fF)	Ls (pH)	Bandwidth (GHz)	10 dB Return Loss Range (GHz)	ERL (dB)
1	85	100	55.7 GHz	f < 24.2 GHz	15.3
2	85	120	54.3 GHz	f < 24.1 GHz	15.2
3	100	100	54.2 GHz	f < 23.3 GHz	15.1
4	100	120	52.8 GHz	f < 23.2 GHz	15.0
Case	Cd (fF)	Ls (pH)	Bandwidth (GHz)	10 dB Return Loss Range (GHz)	ERL (dB)
1	85	100	49.9 GHz	f < 16.7 GHz	12.3
2	85	120	49.3 GHz	f < 17.2 GHz	12.3
3	100	100	48.9 GHz	f < 16.0 GHz	12.0
4	100	120	48.3 GHz	f < 16.3GHz	12.1
Case	Cd (fF)	Ls (pH)	Bandwidth (GHz)	10 dB Return Loss Range (GHz)	ERL (dB)
1	85	100	47.2 GHz	f < 22.4 GHz	12.6
2	85	120	46.8 GHz	f < 22.4 GHz	12.8
3	100	100	46.5 GHz	f < 22.0 GHz	12.0
4	100	120	36.5 GHz	f < 22.0 GHz	12.7
Case	Cd (fF)	Ls (pH)	Bandwidth (GHz)	10 dB Return Loss Range (GHz)	ERL (dB)
1	85	100	37.5 GHz	f < 18.2GHz	13.8
2	85	120	37.8 GHz	f < 18.4 GHz	14.0
3	100	100	36.7 GHz	f < 17.7 GHz	13.4
	100	120	26.7.011-	f < 17.9 CH-	1 4 1

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Correlation of ERL to 10dB Return Loss Range (2/2)



- ERL values are correlated with RL ranges for the shorter 2mm and 4mm packages
- No evidence of strong correlation of ERL with bandwidth

Time domain simulations

- Source eye diagram
 - Generated by a Gaussian filter with 800mV output swing (resulting in $t_{r/f}(20-80) \approx 6$ ps)
 - Source driving into 100Ω ideal termination with no Rx equalization
 - No observation filter at receiver (e.g. neither Bessel-Thomson nor Butterworth)



Case	TRL (mm)	Cd (fF)	Ls (pH)	EH (mV)	VEC (dB)	EW (UI)
Tx eye	0	0	0	262	0.09	0.745

Case 1 Time domain simulations ($C_d = 85$ fF, $L_s = 100$ pH)



Case 2 Time domain simulations ($C_d = 85$ fF, $L_s = 120$ pH)



Case 3 Time domain simulations ($C_d = 100 \text{ fF}$, $L_s = 100 \text{ pH}$)

<u>3a</u>

<u>3c</u>



Case	TRL (mm)	Cd (fF)	Ls (pH)	EH (mV)	VEC (dB)	EW (UI)
За	2	100	100	93	9.15	0.465
3b	4	100	100	71	11.5	0.370
3c	6	100	100	90	9.43	0.475
3d	8	100	100	142	5.47	0.405

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Case 4 Time domain simulations ($C_d = 100 \text{ fF}$, $L_s = 120 \text{ pH}$)



Case						
4a	2	100	120	87	9.73	0.510
4b	4	100	120	89	9.53	0.430
4c	6	100	120	113	7.46	0.480
4d	8	100	120	126	6.51	0.435

Time domain simulation observations

- $C_d = 85$ fF provides more eye height and eye width than $C_d = 100$ fF
 - While still giving a reasonable residual capacitance value
- L_d = 120 pH provides a more consistent eye shape across the package sizes than L_s = 100 pH
 - Likely to be associated with better impedance matching through the package model
- For eye width 2mm package was generally best followed by the 6mm package
- Eye height is not well correlated to package size
- The 4mm case appears significantly different most likely due to reflections aligning around the eye centre

Host-to-module whole-link simulation

 $L_{d} = 120 \text{ pH}$



- TX FIR is set by TP1a Reference receiver C2
- Module RX is assumed to be 4-tap DFE for whole-link simulation.
- TX package length is 13 mm, the worst for TP1a VEC.
- Existing short channel models are harder to whole link.
- Worst whole-link COM varies with module package length.

Courtesy of Phil Sun

Summary

- Approach used in healey_3ck_adhoc_01_061219 for the ASIC termination has been applied to the module die termination
- Case 2 (C_d = 85 fF with L_d = 120 pH) is best performing
 - Total die + die bump = 85 fF + 30 fF = 115fF
- Case 4 (C_d =100 fF with L_d = 120 pH) is second best performing
 - Total die + die bump = 100 fF + 30 fF = 130fF
- Propose adoption of Case 2 for further analysis
 - Further analysis of TP1a + end-to-end channels

Termination	Rd	Cd	Ld	Cb	Comment
Host ASIC (slide 4 of healey_3ck_adhoc_061219)	50 Ω	120 fF	120 pH	30 fF	Implemented in COM ver 2.70
Proposed Module Die Term	50 Ω	85 fF	120 pH	30 fF	

Backup

COM settings for ERL calculation

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[12]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.39	v	vp/vf=.694
A_fe	0.39	v	vp/vf=.694
A_ne	0.578	v	
L	4		
м	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.5		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	0		[min:step:max]
c(-3)	0		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0.85		
b_max(2N_b)	0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	<pre>.\results\100GEL_KR_{d ate}\</pre>	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	[1 3 2 4]
RUNTAG	KR_eval_	
COM CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	1	logical
TR_TDR	0.01	ns
Ν	3000	
beta_x	2.53E+09	
rho_x	0.25	
fixture delay time	0	s
TDR_W_TXPKG	0	
N_bx	4	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters 5.2dB at 26.56GHz		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	6.200E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	102.7	mm
z_bp (NEXT)	102.7	mm
z_bp (FEXT)	102.7	mm
z_bp (RX)	102.7	mm

Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	0	taps per group
N_f	0	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps

yellow indicates WIP

ffe_pre_tap_len	0	UI
ffe_post_tap_len	4	UI
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.125	
ffe_backoff	0	

Specific ERL-relevant COM parameters

T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	1	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	0.25	
fixture delay time	0	S
TDR_W_TXPKG	0	
N_bx	4	UI