

Baseline Proposal for “100 Gb/s, 200 Gb/s, and 400 Gb/s Chip-to-Chip Attachment Unit Interface (100GAUI-1, 200GAUI-2, and 400GAUI-4)”

IEEE 802.3ck Task Force
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Ali Ghiasi, Ghiasi Quantum
Mike Peng Li, Intel

100GAUI-1, 200GAUI-2, 400GAUI-4 C2C Baseline Document Supporters

Contributors and Supporters

Mike Peng Li, Intel

Ali Ghiasi, Ghiasi Quantum

Ted Sprague, Infinera

Rick Rabinovich, Keysight

Richard Mellitz, Samtec

Mike Dudek, Marvell

Phil Sun, Credo

Matt Brown, Independent

Jane Lim, Cisco

Pirooz Toyserkani, Cisco

Purpose

- Present a baseline specification proposal for 100GAUI-1, 200GAUI-2, and 400GAUI-4 C2C electrical interface in support of the 100 Gb/s, 200 Gb/s, and 400 Gb/s Chip-to-Chip (C2C) electrical interfaces operating with end-to-end FEC (without the need for segmented FEC) in support of ASIC/FPGA-ASIC/FPGA and ASIC/FPGA-retimer applications.
- To fulfill following Task Force objectives:
 - Define a single-lane 100 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications
 - Define a two-lane 200 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications
 - Define a four-lane 400 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications.

C2C Technology Choice Highlights

- Channel equalization based on a transceiver having TX FIR and RX CTLE/DFE
- Levering clause 120D structure with double the baud rate, COM 2.70, and updated package model
 - COM spreadsheet included see page 12 and 13
- Leverage P802.3ck adopted reference package specification (see walker_3ck_01d_0719.pdf)
- Optional link training per CL 120D
- Operating with end-to-end FEC without the need to terminate the FEC on C2C link
- Pre-FEC BER $\leq 1E-5$
- End-to-end post FEC link BER for 100 GbE $\leq 1E-12$
- End-to-end post FEC link BER for 200 GbE and 400 GbE $\leq 1E-13$
- Informative/recommend maximum channel insertion at Nyquist: 20 dB* .

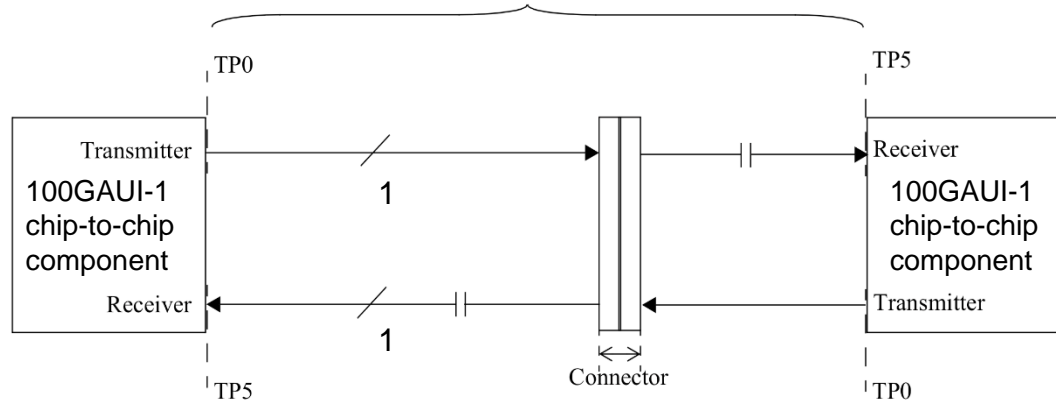
* Max informative recommended loss value is place holder and require further investigation.

C2C Technology Choice Highlights, Cont.

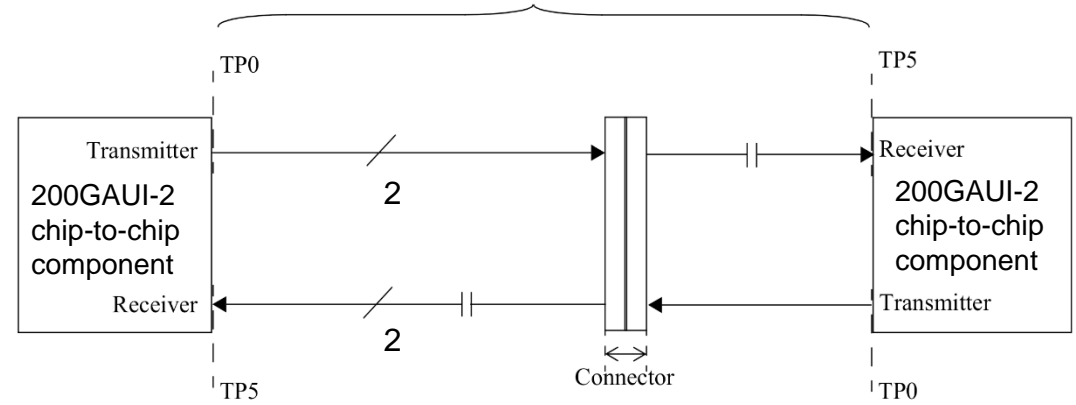
- Reuse clause 82 PCS and clause 91 RS(544,514) FEC for 100 GbE
 - Including, Gray mapping, PAM4 encoding, and optional precoding
 - If the Task force decides to go with 100 GbE interleaved FEC it will be transparent to C2C interface
- Reuse clause 118/119 PCS/FEC for 200GbE/400 GbE
 - Including, Gray mapping, PAM4 encoding, and optional precoding
- Reuse clause 120D.3.2.2 for Receiver jitter tolerance
- Transmitter equalization feedback (optional) - Clause 120D.3.2.3.

C2C Link Topology

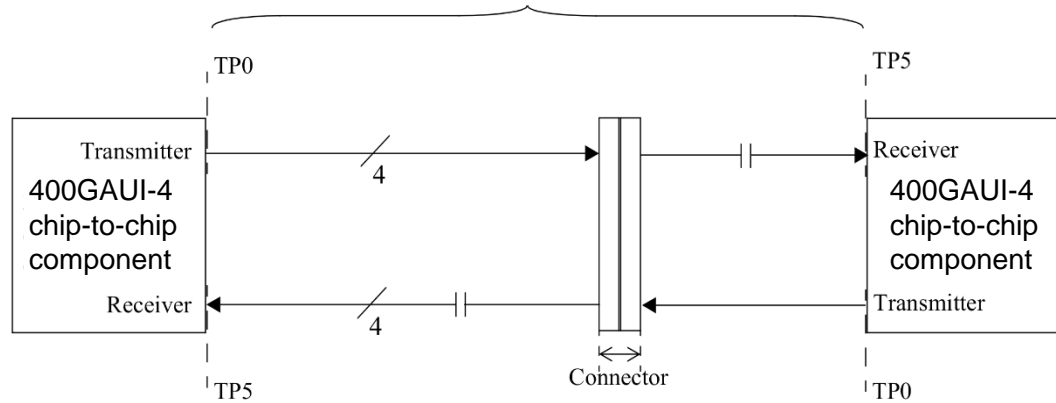
100GAUI-1 chip-to-chip channel



200GAUI-2 chip-to-chip channel



400GAUI-4 chip-to-chip channel

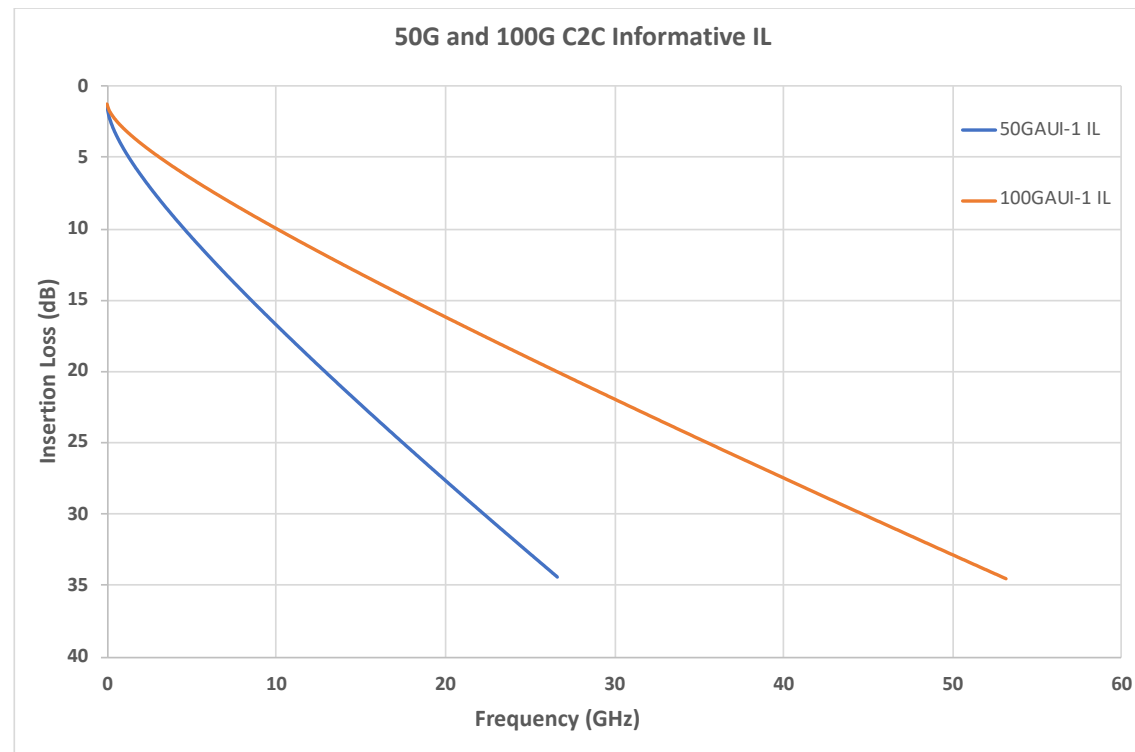


C2C Maximum Recommended Insertion Loss (IL)

- Informative max recommended IL scaled from equation (120D-1) assuming 20 dB* loss at Nyquist is given by equation:

– Max IL= $1.083 + 1.444 \times \sqrt{f} + 0.432 \times f$, for $0.01 \leq f \leq 53.125$ GHz.

* Max informative recommended loss value is place holder and require further investigation.



100GAUI-1, 200GAUI-2, and 400GAUI-4 C2C Transmitter characteristics at TP0a

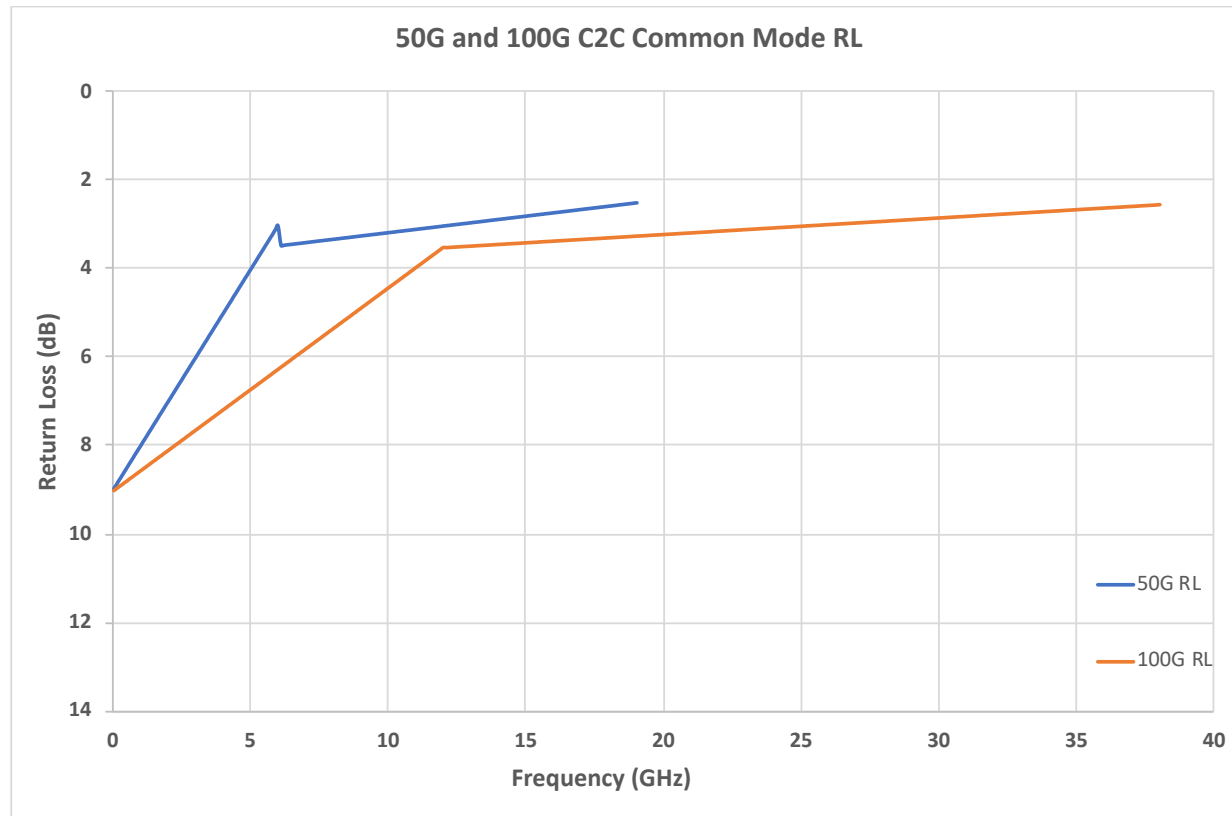
Parameters	Reference	Value	Units
Signaling rate per lane (range)		53.125	GBd
Differential Voltage	93.8.1.3		mV
TX disabled		35	
TX enabled		1200	
DC Common Mode output Voltage (max)	93.8.1.3	1.9	V
DC Common Mode output Voltage (min)	93.8.1.3	0	V
AC Common Mode output Noise (rms)		30	mV
Differential output return loss (informative)		See Page 9	dB
Effective return loss (ERL) (min.)		TBD	dB
Common-mode output return loss		See Page 9	dB
Output waveform			
Level separation mismatch ratio RLM (min) Steady state voltage v_f (max)	120D.3.1.2	0.95	—
Steady state voltage v_f (min)	120D.3.1.4	0.6	V
Linear fit pulse peak (min)	120D.3.1.4	0.4	V
Pre-cursor equalization	120D.3.1.5	TBD $\times v_f$	V
Post-cursor equalization	120D.3.1.5	Table 120D-2*	—
		Table 120D-3*	—
Signal-to-noise-and-distortion ratio SNDR (min)	120D.3.1.6	TBD	dB
Transmitter Output residual ISI SNR_{ISI} (min)	120D.3.1.7	TBD	dB
Output jitter			
JRMS (max)	120D.3.1.8	0.023	UI
J4u (max)	120D.3.1.8	0.118	UI
Even-odd jitter (max)	120D.3.1.8	0.019	UI

*Need to be updated for C(-2) and C(-3) to be aligned with slide 12

Common Mode Return Losses

- Common mode return loss is scaled from 93-4.

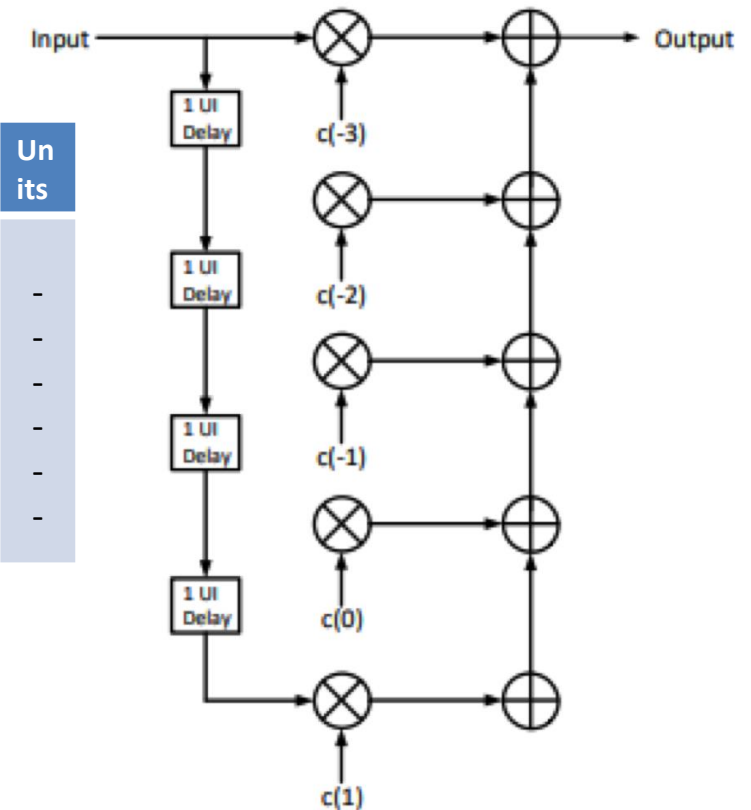
$$RL \geq \begin{cases} 9.05 - 0.4605 \times f, & 0.05 \leq f \leq 12 \text{ GHz} \\ 3.98 - 0.0375 \times f, & 12 \leq f \leq 38 \text{ GHz} \end{cases} \text{ dB}$$



Transmit Equalizer

- Transmit functional is based on 4 or 5 taps FIR, with $C(-3)$ as defined in clause 163
 - If $C(-3)$ proven to have no value, then will be removed.

Parameters	Reference	Value	Units
Transmitter output waveform			
abs step size for $c(-3)$, $c(-2)$, $c(-1)$, $c(0)$, and $c(1)$ (min.)	136.9.3.1.4	0.005	-
abs step size for $c(-3)$, $c(-2)$, $c(-1)$, $c(0)$, and $c(1)$ (max.)	136.9.3.1.4	0.02	-
value at minimum state for $c(-3)$, $c(-1)$ and $c(1)$ (max.)	136.9.3.1.4	-0.06/-0.34/-0.1	-
value at maximum state state for $c(-2)$ (min.)	136.9.3.1.4	0.12	-
	&walker_3ck_01d_0719		-
			-



Transmitter Test

- **Transmitter linearity 120D.3.1.2**
- **Measurement of mean signal levels 120D.3.1.2.1**
- **Linear fit to the measured waveform 120D.3.1.3**
- **Steady-state voltage and linear fit pulse peak 120D.3.1.4**
- **Transmitter equalization settings 120D.3.1.5 and updated range provided on previous page**
- **Transmitter output noise and distortion 120D.3.6**
- **Output jitter and test patterns 120D.3.8**
- **J_{4u} and J_{RMS} jitter 120D.3.1.8.1**
- **Even-odd Jitter 120D.3.1.8.2**

C2C COM Parameters

Parameter	Symbol	Value	Units
Signaling rate	fb	53.125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model			
Single-ended device capacitance	C_d	1.2e-4	nF
Single-device series inductance	L_s	0.12	nH
Single-ended capacitance at the device-to-package interface	C_b	0.3e-4	nF
Transmission line length, Tx Test 1, 2	Z_p	[13 31]	mm
Transmission line length, Rx Test 1, 2	Z_p	[11 29]	mm
Transmission line 2 length	Z_{p2}	1.8	mm
Single-ended package capacitance to package-to-board interface	C_p	0.87x10-4	nF
Package transmission line nominal characteristic impedance	Z_c	87.5	Ω
Package transmission line 2 nominal characteristic impedance	Z_{c2}	92.5	Ω
Single-ended reference resistance	R_o	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	fr	$0.75 \times fb$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.54	—
Transmitter equalizer, pre-cursor coefficient, Minimum value Maximum value step size	$c(-1)$	-0.34 0 0.02	—
Transmitter equalizer, pre-cursor coefficient, Minimum value Maximum value step size	$c(-2)$	0 0.12 0.02	—
Transmitter equalizer, pre-cursor coefficient, Minimum value Maximum value step size	$C(-3)$	-0.06 0 0.02	---
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	-0.1 0 0.05	—

C2C COM Parameters, cont.

Parameter	Symbol	V alue	Units
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	-20 0 1	dB
Continuous time filter DC gain2 Minimum value Maximum value Step size	g_{DC2}	-4 0 1	dB
Continuous time filter, zero frequencies	f_z	$fb/2.5$	GHz
Continuous time filter, pole frequencies	$fp1\ fp2$	$fb/2.5\ fb$	GHz
Continuous time filter, low frequency pole/zero	f_{LF}	$fb/80$	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	A_v A_{fe} A_{ne}	0.413 0.413 0.608	V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	RLM	0.95	
Transmitter signal-to-noise ratio	$SNRTX$	33	dB
Number of samples per unit interval	M	32	—
Equalizer	N_b	TBD	UI
Normalized DFE coefficient magnitude limit, for $n = 1$ to N_b	$b_{max}(n)$	TBD	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	ADD	0.02	UI
One-sided noise spectral density	n_o	8.2×10^{-9}	V ² /GHz
Target detector error ratio	$DERO$	10^{-5}	

Receiver Characteristics

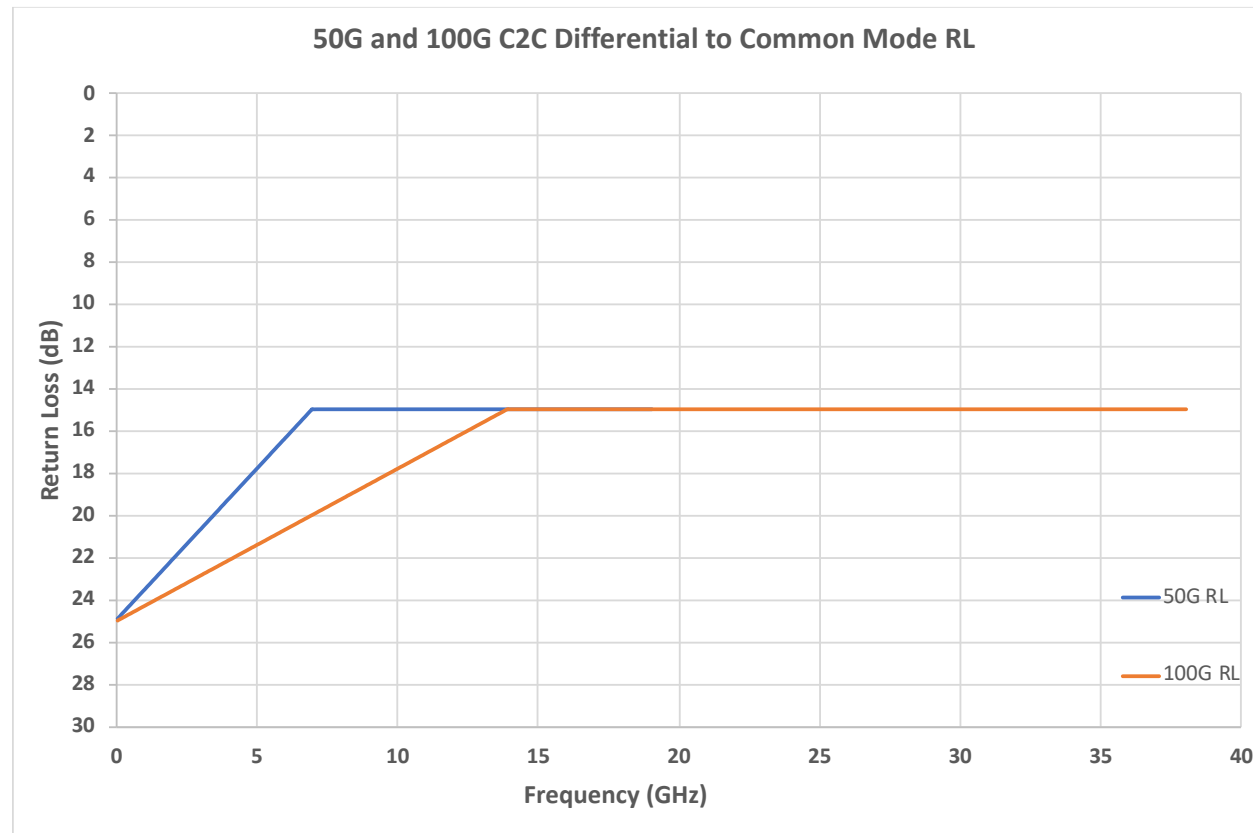
- A 100GAUI-1, 200GAUI-2 or a 400GAUI-4 chip-to-chip receiver shall meet the specifications given in Table below.

Parameter	Reference	Value	Units
Effective return loss (ERL) (min.)		TBD	dB
Differential to common mode input return loss		See Page 15	dB
Interference tolerance	120D.3.2.1	Table 120D–6 See page 15	—
Jitter tolerance	120D.3.2.2	Table 120D–7	—

Common Mode Return Losses

- Common mode return loss is scaled from 93-5.

$$RL \geq \begin{cases} 25 - 0.72 \times f, & 0.05 \leq f \leq 13.9 \text{ GHz} \\ 15, & 13.9 \leq f \leq 38 \text{ GHz} \end{cases} \text{ dB}$$



Receiver Interference Tolerance

- Based on clause 120D.3.2.1
 - Exception paragraph J replace 33 GHz 3 dB BT4 filter with 53 GHz BT4 filter.

Parameter	Test 1 (low loss)			Test 2 (high loss)			Units
	Min	Max	Target	Min	Max	Target	
PCS FEC Symbol error ratioa	—	10 ⁻⁴	—	—	10 ⁻⁴	—	—
Insertion loss at 26.5625 GHz	9.5	10.5	—	19.5*	20.5*	—	dB
RSS_DFE4	TBD	—	—	TBD	—	—	—
COM including effects of broadband noised	—	—	3	—	—	3	dB

* Max informative recommended loss value is place holder and require further investigation.

Summary

- This contribution provide C2C baseline in support of P802.3ck task force objective
- The C2C baseline address ASIC/FPGA-ASIC/FPGA or ASIC/FPGA-retimer applications with up to **20 dB*** insertion loss
- The contribution does not address following items as they require further study:
 - The maximum recommended insertion loss of the channel (≥ 20 and ≤ 24 dB)
 - The benefits of Tx FIR C(-3) and determine if it can be removed
 - Reference receiver DFE tap length and coefficients
 - Details on the interference tolerance test.