FEC Latency and Power/Area Tradeoffs for 100G KR/CR

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Summary

- An interleaved RS(544,514) FEC has been proposed in gustlin_3ck_01_0119 for mitigating potential burst error issues in 100G KR/CR systems based on multi-tap DFE Rx architectures. A 4-lane version was proposed in nicholl_3ck_01b_0519
- Concerns on system latency and complexity for interleaved FEC were raised in several presentations, including lu_3ck_adhoc_01_022719 and lyubomirsky_3ck_01a_0119, while simulations in lyubomirsky_3ck_01a_0319 and anslow_3ck_adhoc_01_041019 (slide 8) showed precoding provides sufficient burst error mitigation for multi-tap DFE receivers on realistic physical channels
- The interleaved FEC proposal was modified in gustlin_3ck_01_0719 for dual FEC modes, where AN is used to select between Clause 91 FEC and interleaved FEC. Some complexity tradeoffs for dual FEC mode were discussed in lu_3ck_02_0719
- In this work, we provide an analysis on the engineering tradeoffs for Clause 91 versus the proposed interleaved FEC in terms of latency and power/area

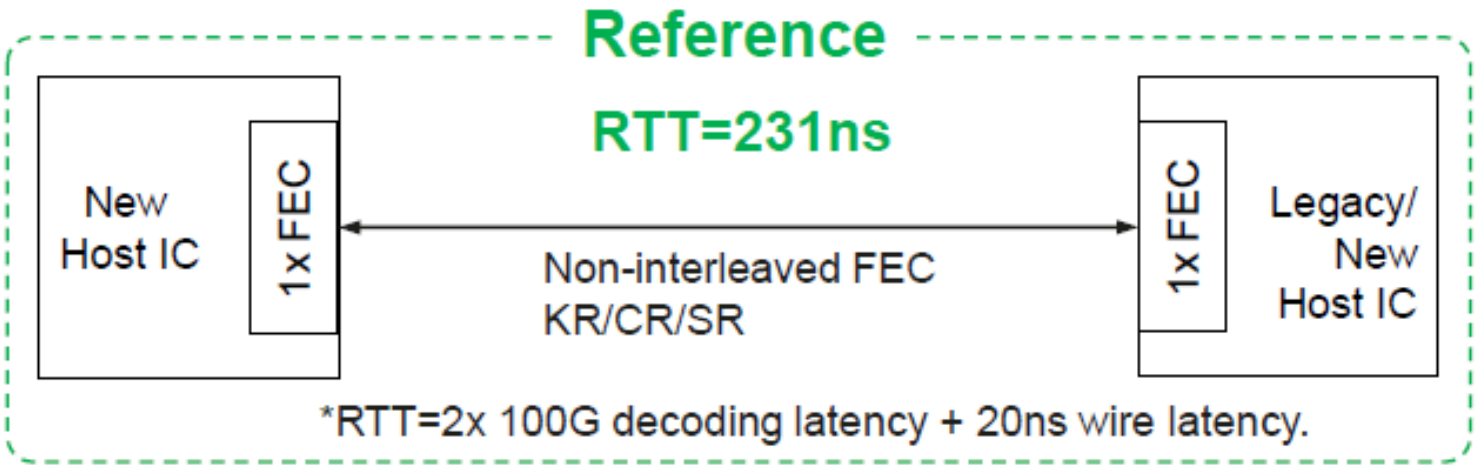
Decoder Latency Comparison

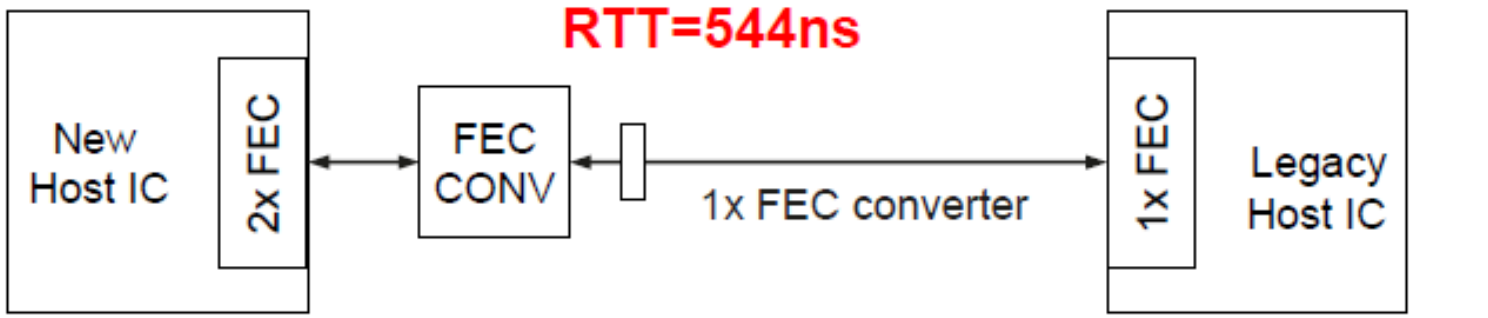
	Clause 91 RS(544,514) FEC	Interleaved RS(544,514) FEC
Block Time	51 ns	102 ns
Processing	100 ns	100 ns
Interleaving/de-interleaving	0	10 ns
Total	**151**	**212**

=> 61 ns increase in latency for interleaved FEC

Latency Impact for Retimer/FEC Converter

From lu_3ck_adhoc_01_022719





*RTT=2x 50G decoding latency + 2x 100G decoding latency + 20ns wire latency.

Decoder Complexity Comparison for Power/Area Impact

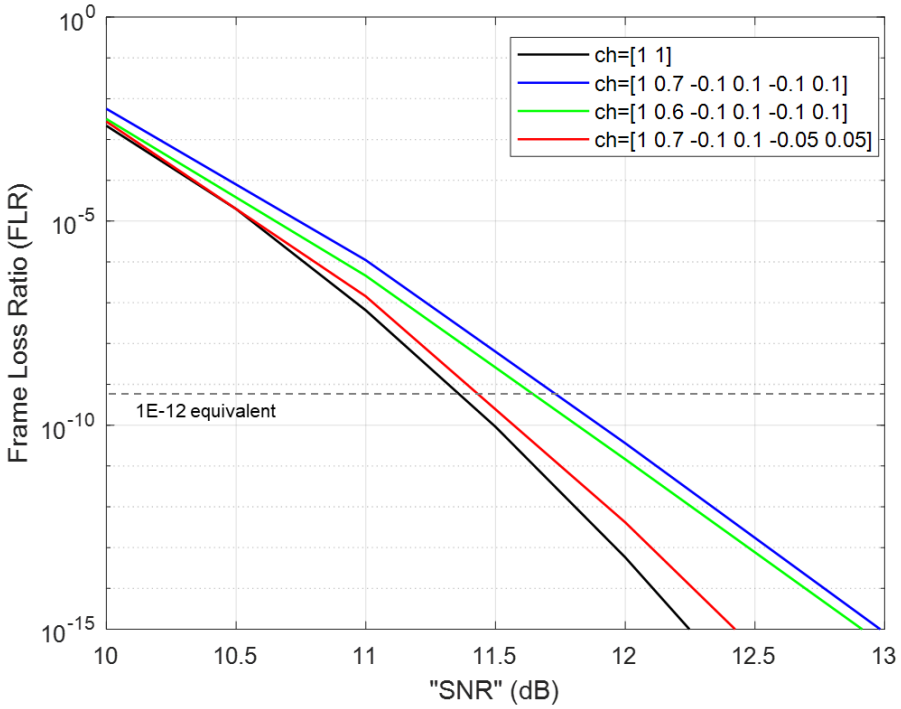
Reference: Prof. Shu Lin, Cathy Liu, and Michael Steinberger, DesignCon 2015 Tutorial

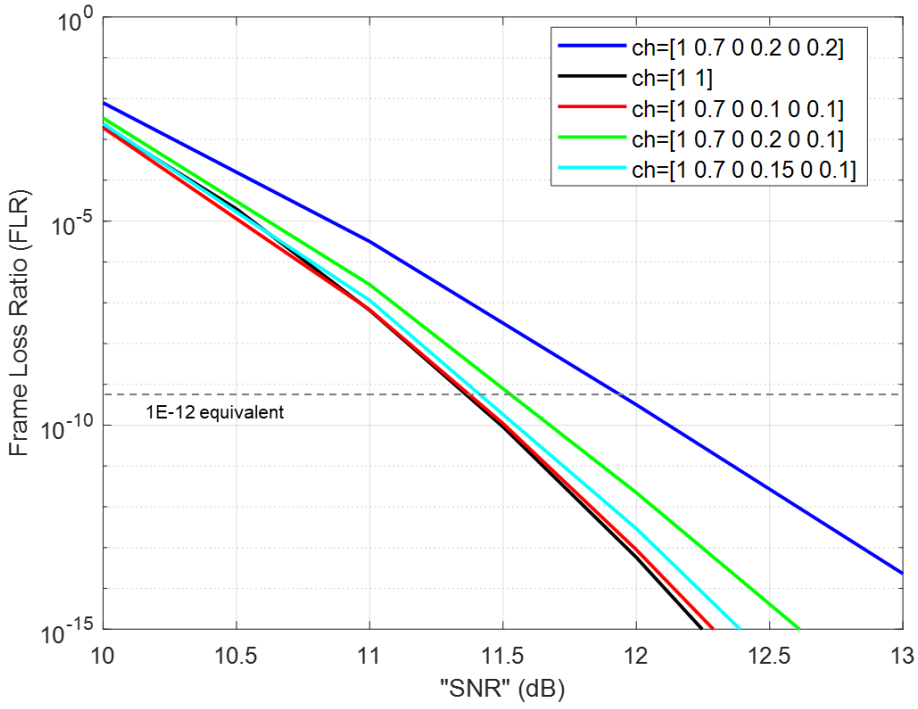
	Clause 91 RS(544,514) FEC	**Interleaved RS(544,514) FEC**	**Comment**
Syndrome	S = 20%	S = 20%	
KES	K = 35%	2 x K = 70%	To keep lowest achievable latency
Chien Search	C = 25%	C = 25%	
Forney	F = 20%	F = 20%	
Interleaver/de-interleaver	I = 0 (none)	I = 5%	
Total	100%	140%	

=> 40% increase in complexity for interleaved FEC

DFE Burst Error Impact for Non-Interleaved RS(544,514)

Simulation results from lyubomirsky_3ck_01a_0319.pdf





- DFE Tap statistics on 115 channels (sun_3ck_02a_0119.zip) show taps drop off to ≤ 0.1 for tap 5 and above; very small negative taps
- Constraining DFE taps to physical values can be effective to mitigate burst error penalties
- See lyubomirsky_3ck_01a_0319 for more detailed analysis

DFE Tap	Max	Mean	Min
1	0.85	0.78	.40
2	0.3	0.24	0.04
3	0.26	0.16	-0.03
4	0.18	0.11	-0.05
5	0.12	0.08	-0.03

Conclusions

- Interleaved FEC would burden 100GBASE-KR/CR system designs by significantly increasing FEC latency, as well as power/area
- Interleaved FEC shows very limited benefit for physical channels; difficult channels can be handled by imposing constraints on DFE tap values and/or implementing Rx architectures which are not prone to burst error problems
- A dual mode FEC with AN is not attractive due to significantly increased and unnecessary system complexity
- Recommendation: Clause 91 FEC is the best solution for 100GBASE-KR/CR