C2M TP1a Criteria Considering Both Long and Short Host Traces

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Introduction

- sun_3ck_01_0719 analyzed 20 benchmark channels contributed to 802.3ck project and concluded 4-tap DFE or even 3-tap FFE (with different thresholds) can be used as reference receivers for the channels under discussion, which are relatively long C2M channels.

- sun_3ck_adhoc_01_081419 simulated TP1a and host-to-module whole-link for 4 short channels from Jane Lim with 2”, 3”, 4”, 9” host trace lengths, and confirmed short package and channel may result in bad signal quality due to bad reflections.

- This contribution reviews short channel simulation results and evaluates TP1a criteria to cover both long and short channels.

- Simulation is performed with COM tool v270. Both host and module are with inductor termination models.

Reference Receiver and TP1a Threshold Review

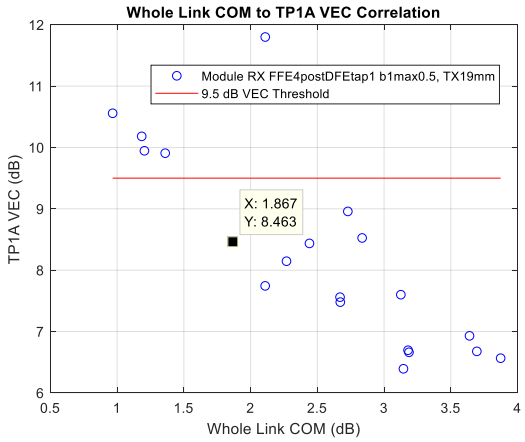
- Reference Receivers (sun_3ck_01_0719):

Higher Performance

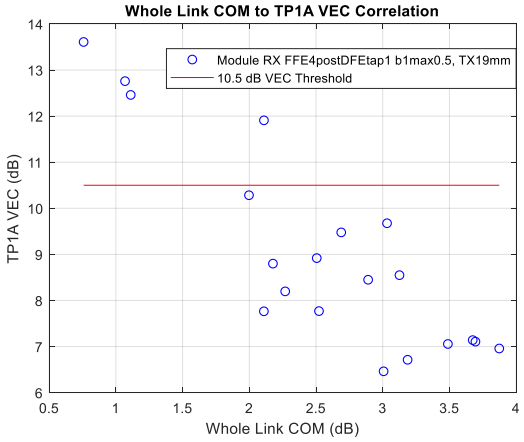
DFE-Based	**A** **4-tap DFE** **(tap 1-4, b1max=0.5)**	**D** **3-tap DFE** **(tap 2 - 4)**	**D2** **1-tap DFE** **(tap 2 only)**
FFE-Based	**B** **5 tap FFE + 1-tap DFE** **(post 1-4, b1max=0.5)**	**C** **5-tap FFE** **(post 1-4)**	**C2** **3-tap FFE** **(post 1-2)**

Less Complexity

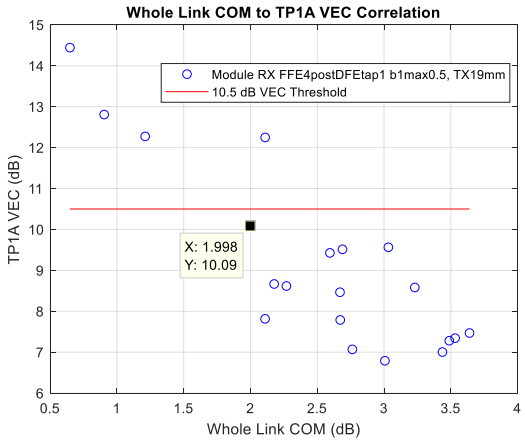
Whole-Link and TP1a Correlation for Long Channels



TX FIR is set by RX C. TP1a VEC threshold is 9.5 dB



TX FIR is set by RX C2. TP1a VEC threshold is 10.5 dB



TX FIR is set by RX D2. TP1a VEC threshold is 10.5 dB

- Whole-link receiver is receiver B (FFE4postDFEtap1).
- Host package is 19 mm with inductor model.
- Worst performance module package length is selected for each channel. Module is with inductor termination model.

sun_3ck_01_0719

Possible Thresholds:

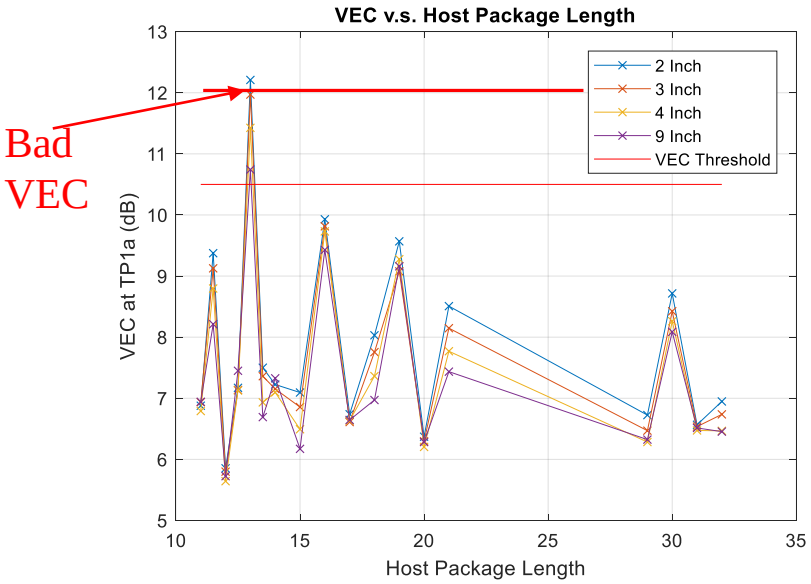
Reference Receiver	A, B	C, D	C2, D2
VEC Threshold (dB)	8	9 to 9.5	10.5 to 12
VEO Threshold (mV)	12.5	8	8

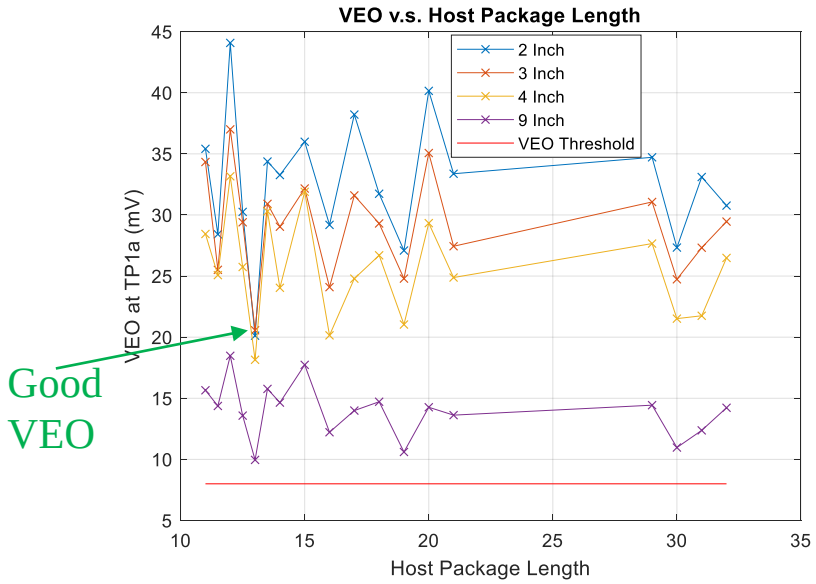
Short Channel Overview with Inductor Termination

ID	Channel Description	IL (dB)	ERL11 (dB)	ERL22 (dB)	ICN (mV)	ILD (dB)
1	host PCB trace 2”	5.67	11.93	13.01	3.52	0.16
2	host PCB trace 3”	6.94	12.69	14.62	3.05	0.15
3	host PCB trace 4”	8.22	13.31	16.07	2.65	0.14
4	host PCB trace 9”	14.55	15.17	21.20	1.34	0.13

- Parameters highlighted in red are worse than 10.5dB ERL, 2.5mV ICN, or 0.35 dB ILD.
- ERL is reported with Nbx=4. ERL11 is for channel only. ERL22 is at TP1a including TX package.

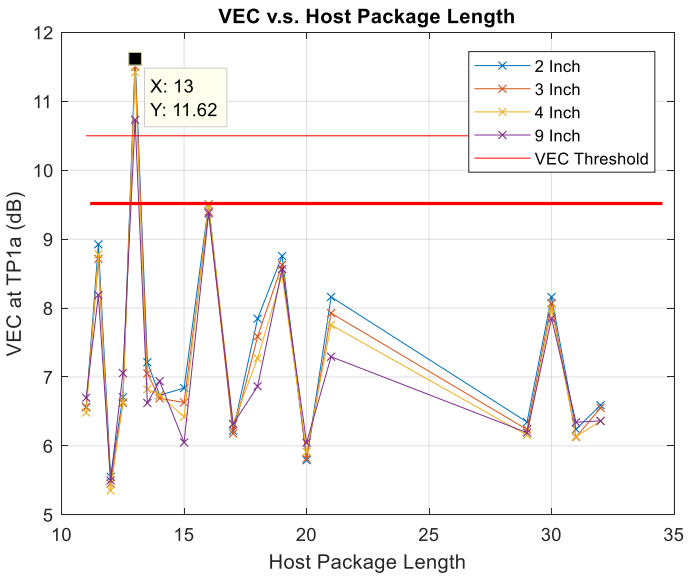
Short Channel TP1a VEC with RX C2

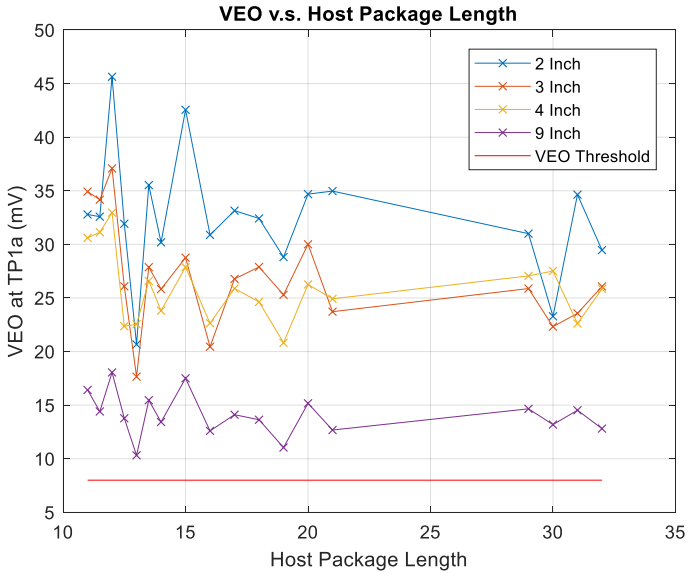




- With Reference receiver C2 – 2 post-tap FFE. Host package between 11 to 32 mm is plotted. Spikes with 7 and 10 mm are slightly worse.
- The VEC spike with 13 mm short package is about 2 dB worse than all the other cases.
- The pike with 13 mm package is close to 12 dB VEC threshold. 12 dB VEC seems promising for both short and long channels.
- Considering VEO for long channel is above the 8mV threshold while VEO for short channels are above 16 mV, is the following OK as an alternative TP1a specification?
  - VEC = 12.0 dB if VEO is above 20 mV
  - VEC=10.5+0.125*(VEO-8) dB for VEO is between 8 and 20 mV.

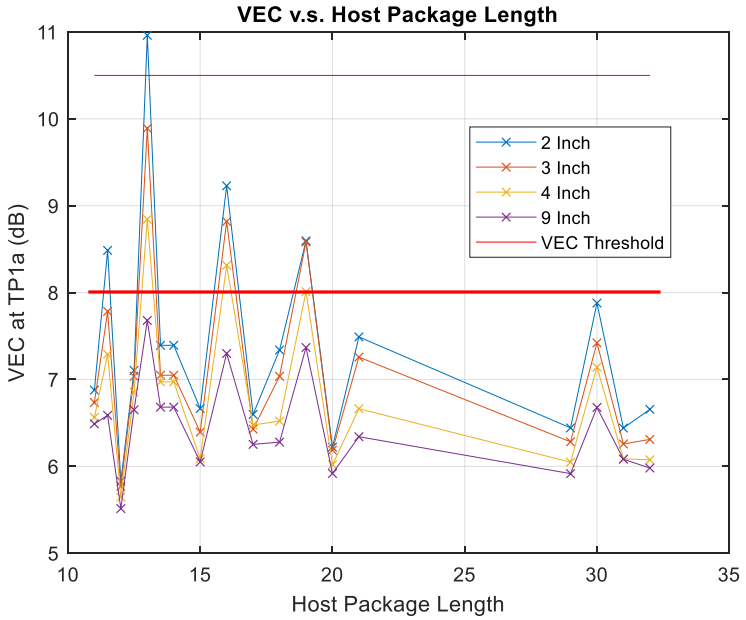
Short Channel TP1a VEC with RX C

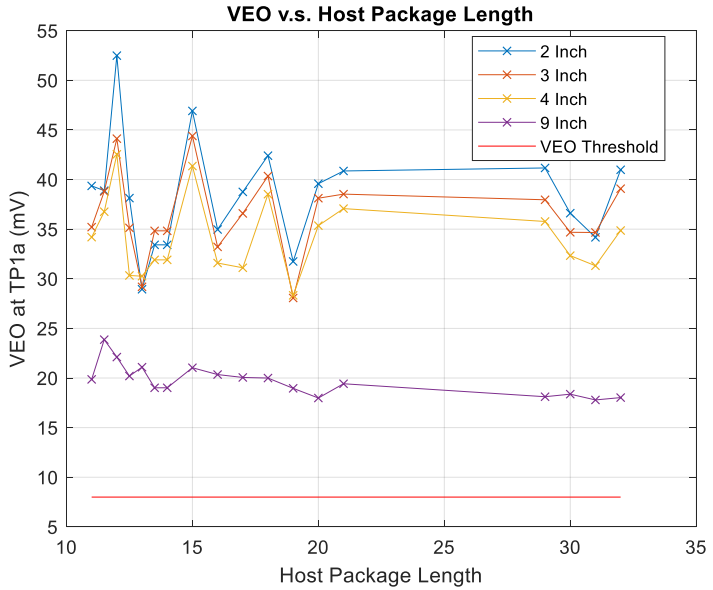




- With Reference receiver C – 4 post-tap FFE
- Short channel VEO is above 16 mV. But VEC is about 11.5dB.
- Possible threshold:
  - VEC = 11.4 dB if VEO is above 20 mV
  - VEC=9+0.2*(VEO-8) dB for VEO is between 8 and 20 mV.

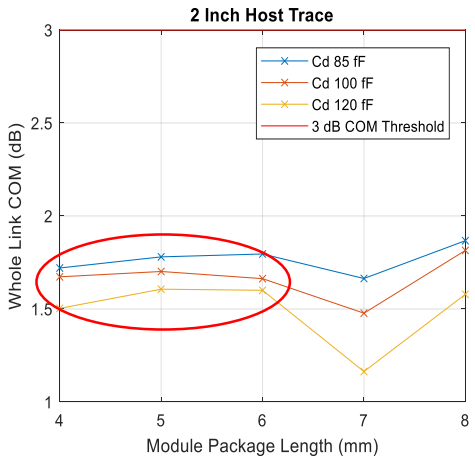
Short Channel TP1a VEC with RX A

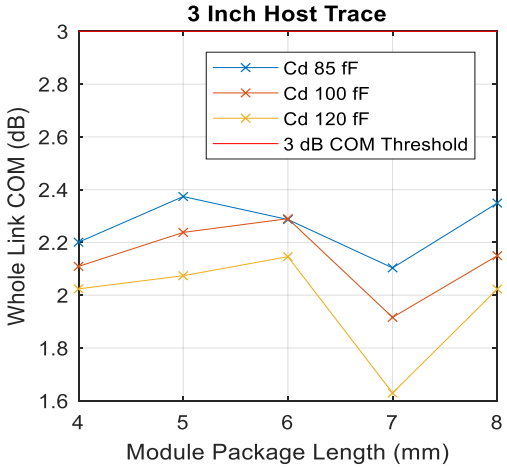


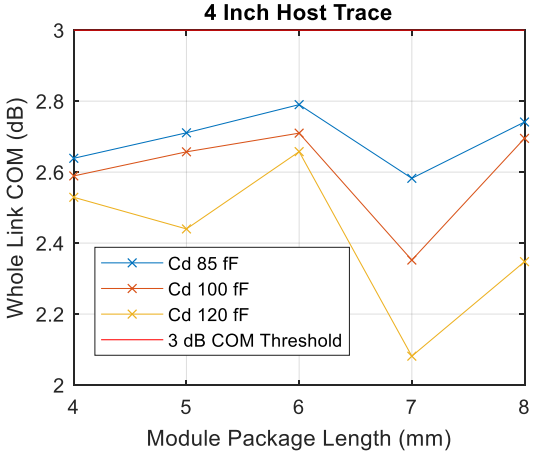


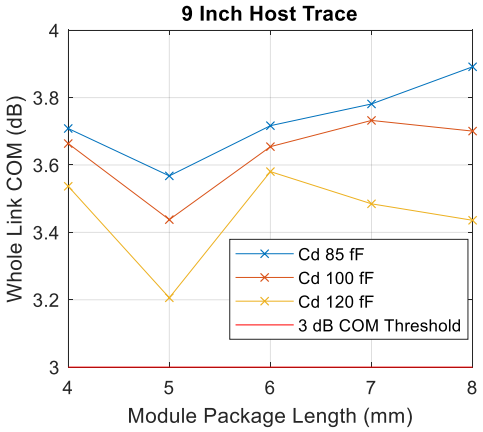
- With Reference receiver A – 4 tap DFE
- The spike with 13 mm package fails 8dB VEC threshold.
- 9” channel VEC meets 8 dB threshold.
- Short channels fail VEC while VEO is above 28 mV.
- Assuming 2” channel needs some improvement, possible TP1a specification:
  - VEC = 10.5 dB if VEO is above 30 mV
  - VEC=8+0.1429*(VEO-12.5) dB for VEO is between 12.5 and 30 mV.

Host-to-module Whole-link Simulation



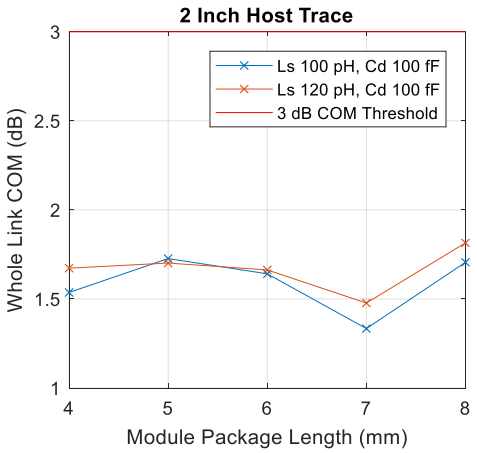


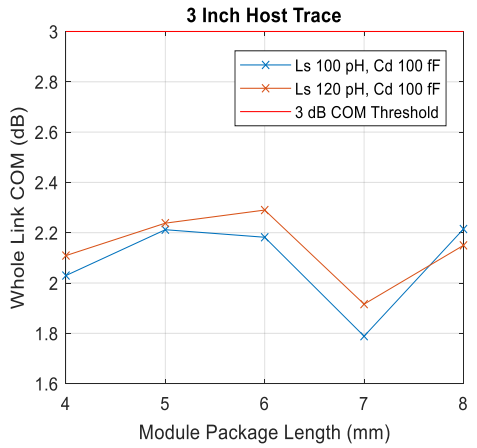


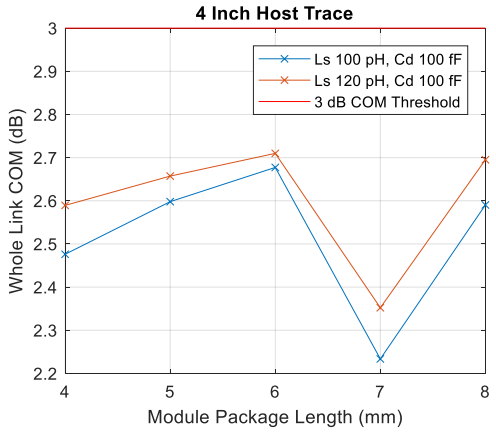


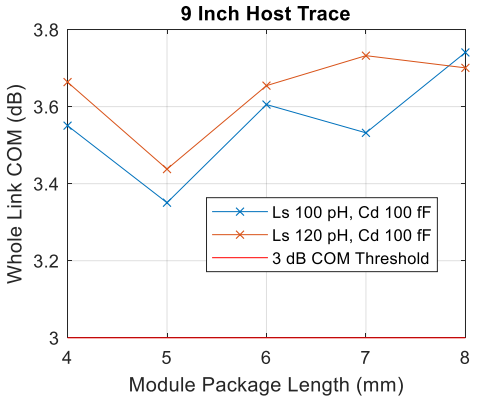
- Module series inductor Ls is set to 120 pH.
- TX FIR is set by TP1a Reference receiver C2
- Module RX is assumed to be 4-tap DFE for whole-link simulation.
- TX package length is 13 mm, the worst for TP1a VEC.
- Short channel whole-link COM has a dip at 7 mm module package.
- Whole link COM with 2” host trace is worse than 2 dB even when module trace is less than 6 mm.
  - TP1a VEC for 2” host trace slightly fails 12 dB as well. Improvement on package or host trace is possible?

Module Series Inductor Comparison



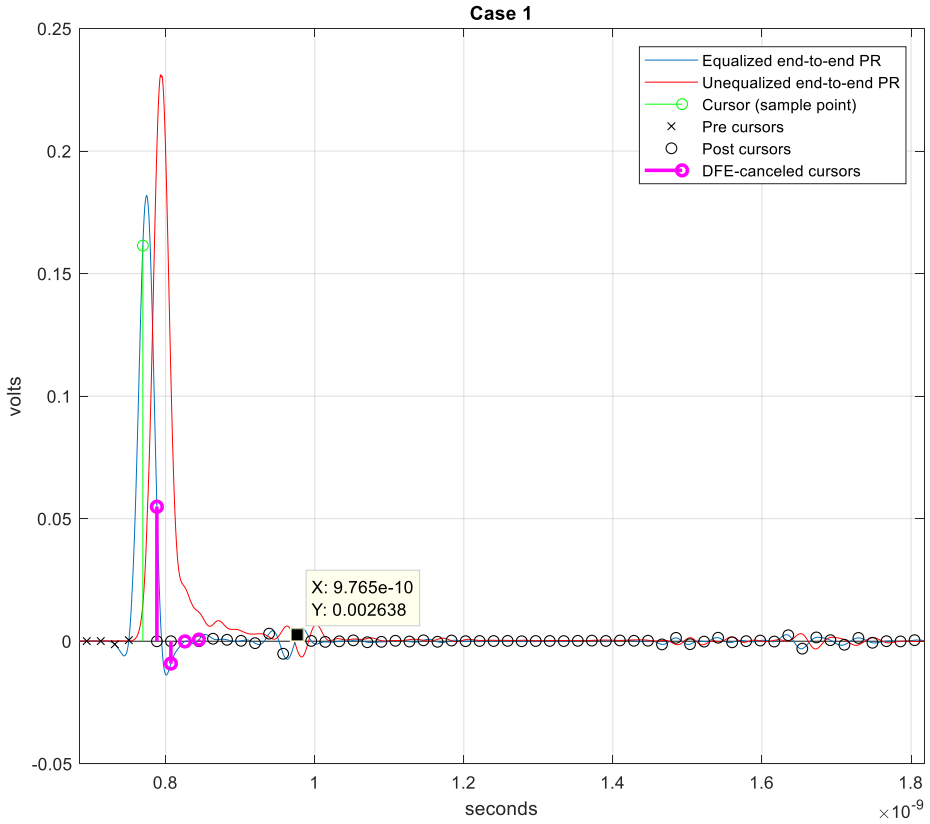






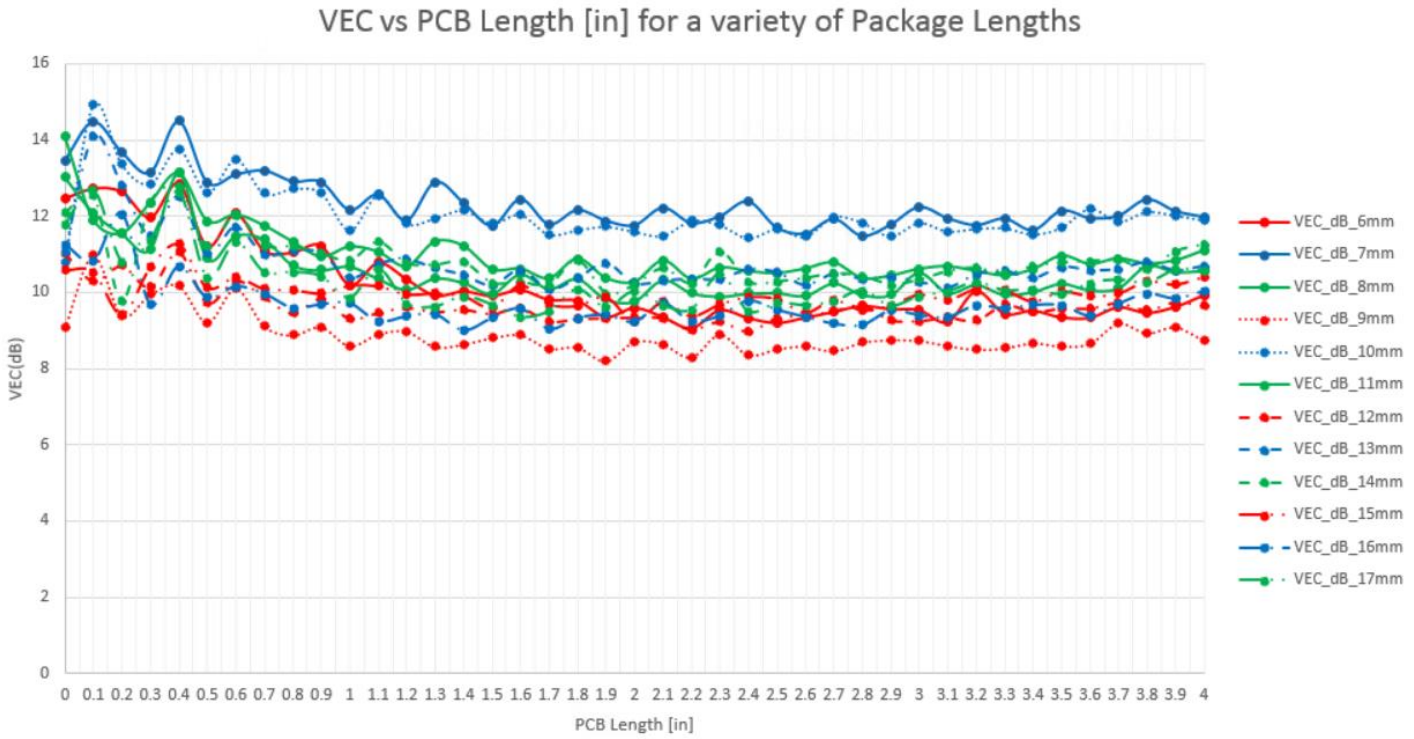
- Ls=120 pH performs slightly better (~0.1 dB) than 100 pH.

Pulse Response Analysis



- With 13 mm package and 2” host trace, reflections are observed at about postcursor 12.

Apply TP1a Criteria on More Simulation Results



- TP1a simulation from Femi Akinwale. Reference receiver is D2.
- 12 dB VEC threshold is OK if package and host trace loss can be controlled. For example,
  - Limit Minimum PCB loss (2” or 1.5” equivalent).
  - Can 7 mm package be avoided?

Summary

- When short package is paired with short host trace, TP1a VEC can be dramatically degraded at certain package/host trace length combinations.
- TP1a criteria such as RX C2/D2 with 12 dB VEC and 8 mV VEO thresholds seem promising to cover both long and short channels.
  - With the low-loss host package model and 12 mm minimum package length assumption, only 2" channel marginally violated 12 dB VEC threshold for Lim channels.
- Combining VEC and VEO may be another choice (relax VEC if VEO is really good).
- With these possible solutions, reference receivers do not need to be more than 5 taps (5 UI span).
- How much the observed short channel reflections can be improved?
  - 100G requires improvements of SERDES as well as channels, packages, and design methodologies. It is preferred if we can avoid increasing module complexity just for the corner cases of short channels.
  - The periodic sharp VEC spikes are real. Is it as dramatic as shown by the models in reality?
  - Can bad reflections of short packages/host traces be alleviated by adding package/board design constraints, e.g., minimum host trace loss?

COM Spread Sheet – TP1a With Ref RX D2

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\TestCaseFloatingBank\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 , 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	testPkg			Parameter	Setting	
z_p select	[1]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[16 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[16 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	119	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.391	V	vp/vf=.694		TDR and ERL options						
A_fe	0.391	V	vp/vf=.694		TDR	1	logical				
A_ne	0.489	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	400					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.6		min		beta_x	0.00E+00					
c(-1)	[-0.3:0.02:0]		[min:step:max]		rho_x	0.32					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0	enter sec				
c(-3)	[-0.04:.02:0.0]		[min:step:max]		TDR_W_TXPKG	1					
c(1)	[-0.1:0.05:0]		[min:step:max]		N_bx	4	UI				
N_b	2	UI			Receiver testing						
b_max(1)	0				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter						
f_z	18.88	GHz			sigma_RJ	0.01	UI				
f_p1	28	GHz			A_DD	0.02	UI				
f_p2	53.125	GHz			eta_0	8.20E-09	V^2/GHz				
g_DC_HP	[-3:1:0]		[min:step:max]		SNR_TX	33	dB				
f_HP_PZ	1.328125	GHz			R_LM	0.95					
ffe_pre_tap_len	0	UI									
ffe_post_tap_len	0	UI									
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	0										

COM Spread Sheet – Whole Link Ref RX A

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\TestCaseFloatingBank\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 , 1.0e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12, 0.12]	nH	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	testPkg			Parameter	Setting	
z_p select	[1]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[13 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[6 8; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
z_p (RX)	[6 8; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	119	mm
C_p	[0.87e-4 0.75e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.391	V	vp/vf=.694		TDR and ERL options						
A_fe	0.391	V	vp/vf=.694		TDR	1	logical				
A_ne	0.489	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	400					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.6		min		beta_x	0.00E+00					
c(-1)	[-0.3:0.02:0]		[min:step:max]		rho_x	0.32					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0	enter sec				
c(-3)	[-0.04:.02:0.0]		[min:step:max]		TDR_W_TXPKG	1					
c(1)	[-0.1:0.05:0]		[min:step:max]		N_bx	4	UI				
N_b	4	UI			Receiver testing						
b_max(1)	0.5				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter						
f_z	12.58	GHz			sigma_RJ	0.01	UI				
f_p1	20	GHz			A_DD	0.02	UI				
f_p2	28	GHz			eta_0	8.20E-09	V^2/GHz				
g_DC_HP	[-3:1:0]		[min:step:max]		SNR_TX	33	dB				
f_HP_PZ	1.328125	GHz			R_LM	0.95					