Host to Module Short Channel Issue and Possible Solutions

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IEEE 802.3ck Task Force

Contributors

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Outline

- Background
- COM Settings for Analysis
- Whole Link Analysis
  - DFE
    - Sensitivity to PTH length & on-die impedance
  - DFE without 1st tap
  - DFE with floating-tap
- TP1a to Whole Link Correlation
- Summary

Background – H2M Short Channel Issue

- Performance fluctuates a lot for different host trace lengths, which were disclosed in
  - li_3ck_02a_0519, dudek_3ck_01_0719
- Jane Lim provided four Host-to-Module (H2M) channels for analysis
  - lim_3ck_adhoc_01_073119
- Some analysis of 'short channel issue' were included in
  - sun_3ck_adhoc_01_081419 – Phil proposed to avoid this issue by adding package/host trace design constraints?
  - akinwale_3ck_adhoc_01a_08282019 – Femi analyzed this issue by Intel's H2M channels

Analysis and Conclusions

- We addressed
  - Whole-link & TP1a analysis for Jane's channels
    - host trace length from 5 to 36 mm
    - total 4 * 29 = 116 CH+PKG test cases
  - 3 different RX with sweeping tap number
    - DFE
    - DFE without 1st post tap
    - DFE with floating-tap
- Observations
  - Root cause is 'reflection' due to host+module package
  - 'Floating-tap' is efficient to conquer the issue
    - Achieve 3 dB for all cases by 2-tap DFE plus 2-tap floating-tap spanned to 12-tap
    - Comparatively, it requires 9-tap DFE to achieve 3 dB
- Next steps
  - Verify on more H2M short channels
  - Adopt DFE with floating-tap as module-side referenced RX

Analyzed H2M Channels & RX

- 4 channels in lim_3ck_adhoc_01_073119 for analysis
  - PCB traces: 2'', 3'', 4'', 9''
  - In general, 9'' is with best performance due to
    - Lower crosstalk & higher ERL
- Sweep host trace length, z_p1(TX)
  - z_p1(TX) = [5:0.5:10 11:1:20 22:2:36]
- Total 4 * 29 = 116 CH+PKG cases
- Three different RXs
  - ***DFE***
  - ***DFE1***: DFE without 1st tap (set b_max[1] = 0)
  - ***DFEf***: DFE with floating (with N_bg, N_bf, N_f settings)

Channel	IL (dB)	ICN (mV)	ERL11 (dB)*1	ERL22 (dB)*1	ILD (dB)
5a=2''	5.67	3.52	14.04	11.07	0.16
5b=3''	6.94	3.05	15.38	11.92	0.15
5c=4''	8.22	2.65	16.51	12.68	0.14
5d=9''	14.55	**1.35**	**20.50**	**15.07**	0.13

1* z_p1(TX) = 10mm, z_p2(TX) = 1.8mm

RX	N_b	N_bg	N_bf	N_f
DFE	[3:1:6 8 9 **10** 14]	-	-	-
DFE1	[3:1:6 8 10 14]	-	-	-
DFEf	[1 2 **3** 4]	1	[1 **2** 3]	[6:10 **12** 15 20]

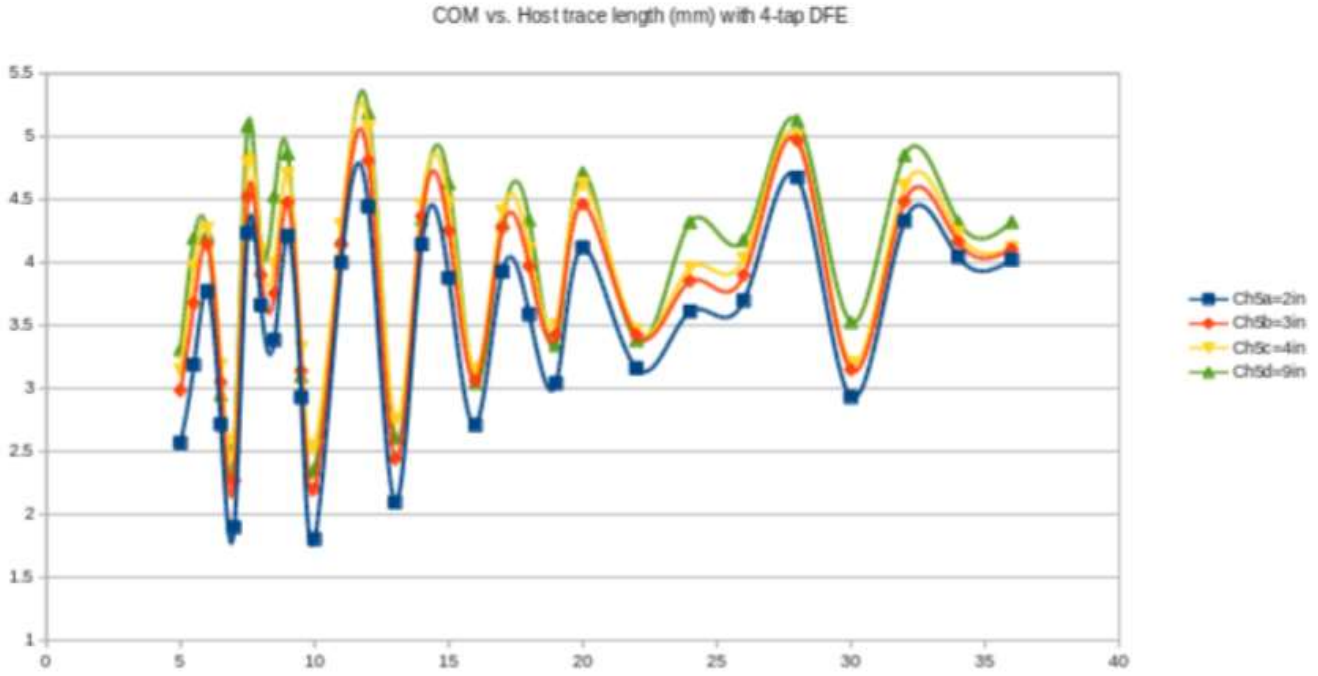
COM Parameter Settings

- COM 2.70
- Whole link: TX PKG + H2M Channels + RX PKG
  - On-die
    - Host [healey_3ck_adhoc_01_061219]
    - Module: Table 1
  - PKG
    - Host [baseline]
    - Module: Table 1
  - g_DC = [-14:1:0] dB
  - g_DC_HP = [-3:1:0] dB
- TP1a: TX PKG + H2M Channels
  - Set ‘zero’ to related RX PKG & on-die settings
- COM spread sheets in appendix

Table 1

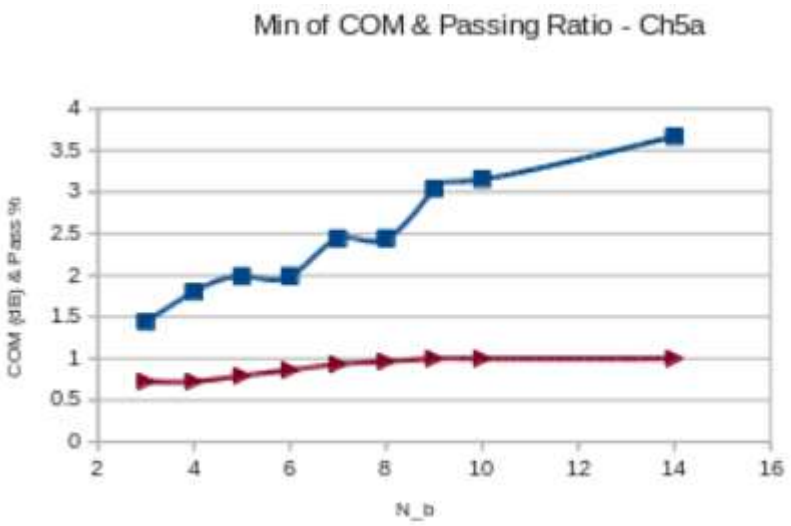
Spec	[Host, Module]	Unit
C_d	[1.2e-4 0.85e-4	nF
L_s	[0.12 0.12]	nH
C_b	[0.3e-4 0.3e-4]	nF
R_d	[50 50]	Ohm
C_p	[0.87 0.87]	nF
z_p(RX)	[8 0]	Ohm

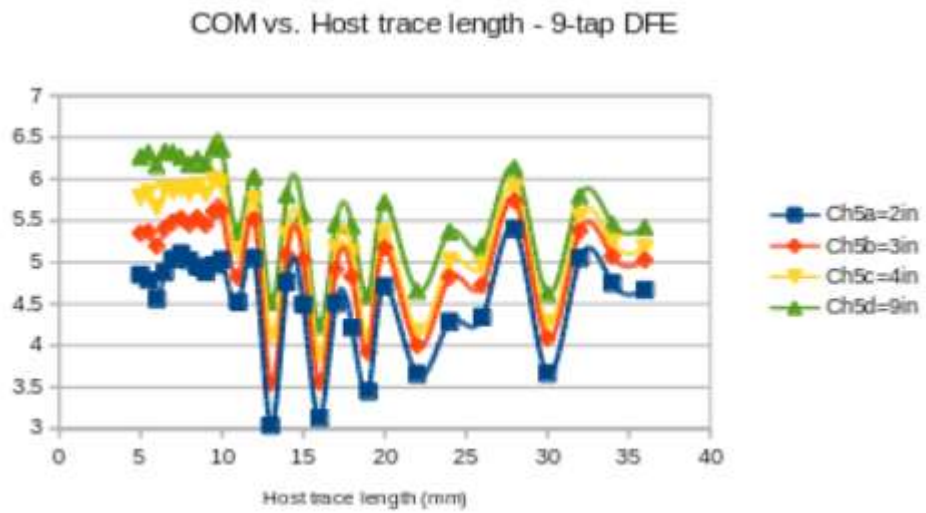
Whole Link COM – 4-tap DFE



- COM fluctuates largely (> 2 dB) when sweeping host trace lengths
  - Multiple valley found (7, 10, 13, & 16 mm) with COM < 3 dB
  - Change TX PTH length (z_p2(TX) = 1.8 → 0 ~ 1.2 mm) change values & positions of valley → still failed 3 dB [Link]
  - Detailed FOM analysis shown ISI is the major source for "fluctuation" due to "reflections" from package [Link]
- Q: How to improve it? By increasing DFE tap number

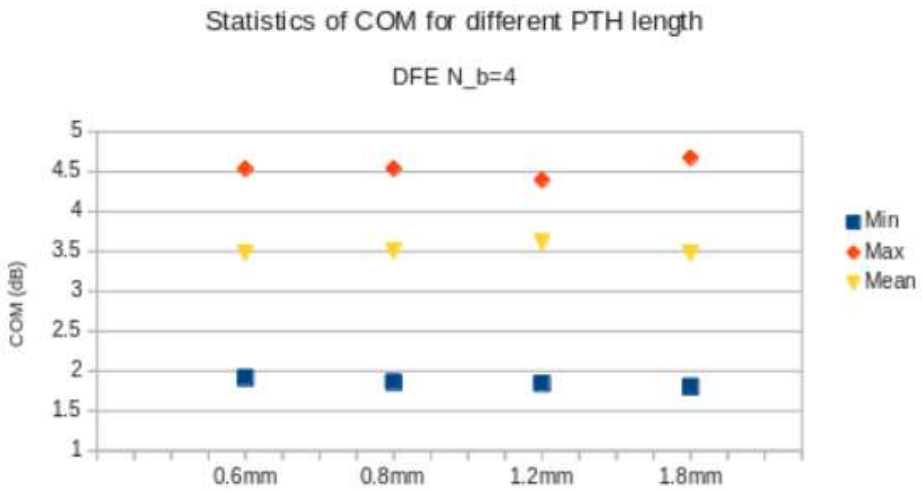
Whole Link COM – Increasing DFE Taps

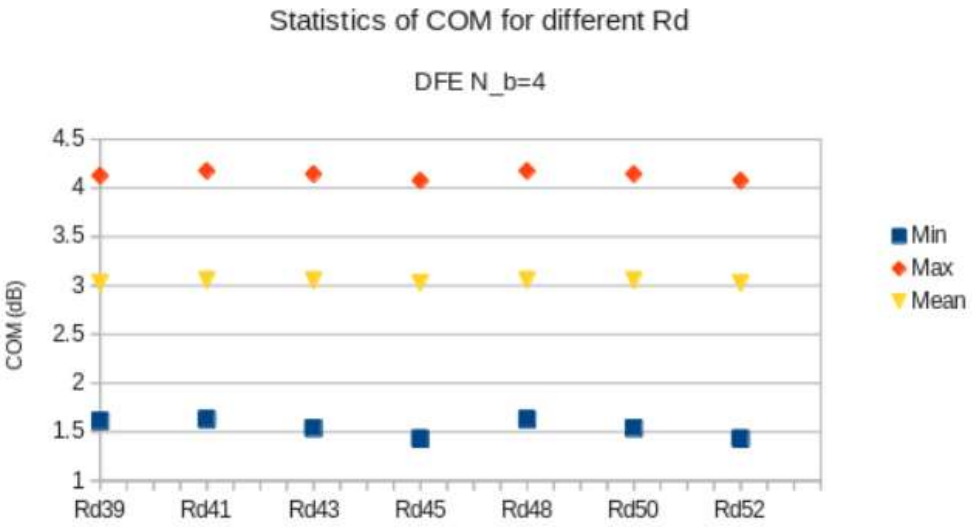




- COM improves by increasing DFE tap number – N_b
  - It requires **9-tap** to achieve 3 dB COM margins for all host trace length
  - 9-tap DFE can cancel "valley" up to 10 mm trace length
  - Each extra DFE tap can cover reflection caused by extra 1.5 mm trace length
- DFE tap without 1st-tap
  - Performance is worse than DFE [Link]
- Next: COM sensitivity to PTH length & R_d

PTH Length & R_d Exploration – DFE Nb=4

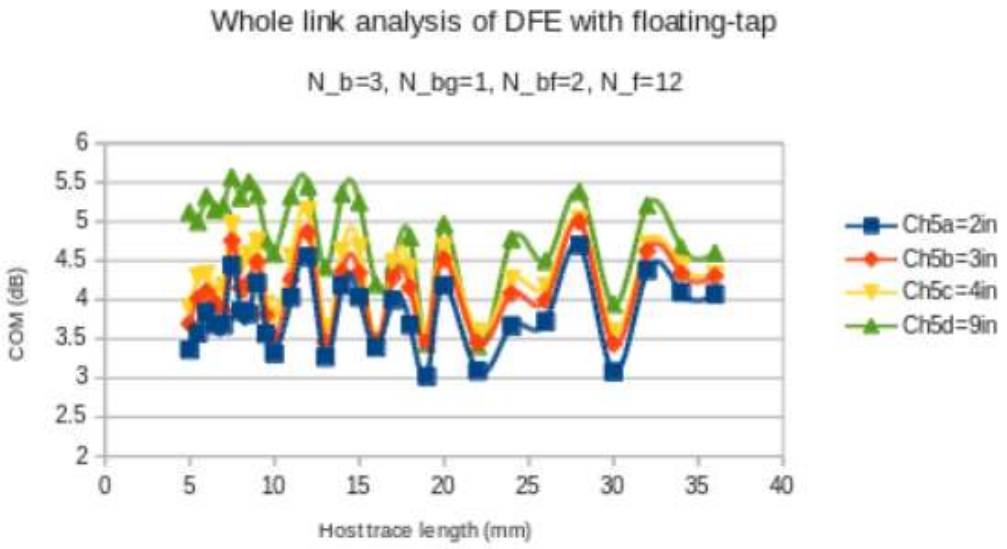




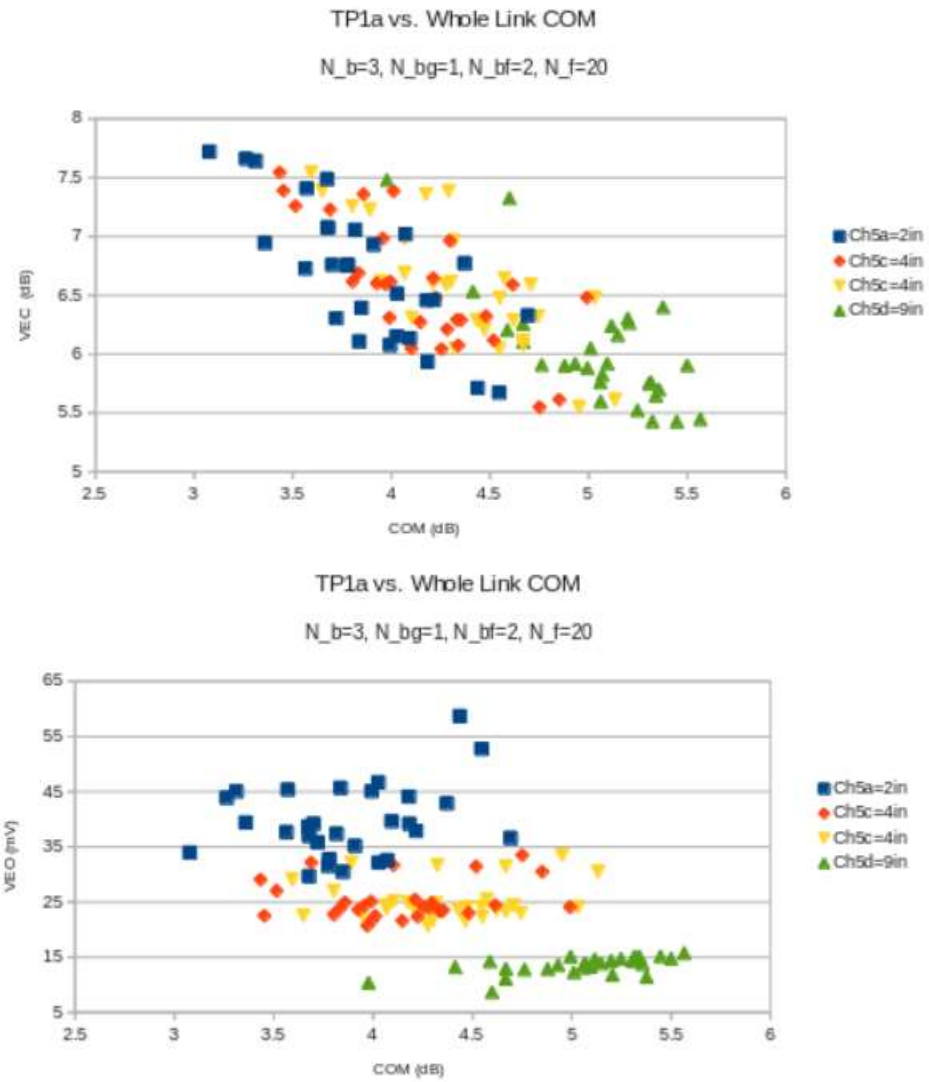
- COM is not sensitive to PTH length & R_d
  - We can't adjust R_d to conquer short channel issue
  - PTH depends on package size and may not be adjusted arbitrarily
- Next: Efficient reflection cancellation by "floating-tap"

DFEf: DFE with Floating-Tap

- DFE with floating-tap had been adopted as KR reference receiver in Vienna meeting [Motion #4 in minutes_3ck_0719_unapproved]
- Applied it to conquer C2M “short channel issue”
- 3 fixed-tap plus 1 bank with 2-tap in group spanning to 12 UI can achieve 3 dB COM [Link]
  - It only takes 2 floating taps to achieve 3 dB COM
  - Total 5-tap DFE
  - Spanning to 12 UI cover “reflection” due to 16 mm trace length



TP1a vs. Whole Link Correlation



- VEC (dB) is kind of correlated to COM in whole link analysis
  - Next: requires simulation of more C2M channels
- VEO (mV) is NOT correlated to COM in whole link analysis
  - More correlated to channel IL
  - Other receivers shared the same trend

Changing RX PKG Parameters

- By referring to contributions of Mike Li & Phil Sun
  - Table 2
  - Table 3
- Test for another PKG case
  - PKG1: Table 1a
  - PKG2: Table 1b
- Changes from 1a to 1b
  - C_p(RX) = 87fF → 65fF
  - z_p(RX) = 8mm → 5mm

Table 2: Module PKG in li_3ck_02a_0519

- Cd = 100fF
- Cp = 65fF
- Length: 2mm ~ 5mm T-line + 0mm PTH

Table 3: Module PKG in sun_3ck_01_0719

C_d	0.85e-4	nF
C_p	0.75e-4	nF
Package trace length Z_p	2-8	mm
Package PTH	0	mm

Table 1a: PKG1

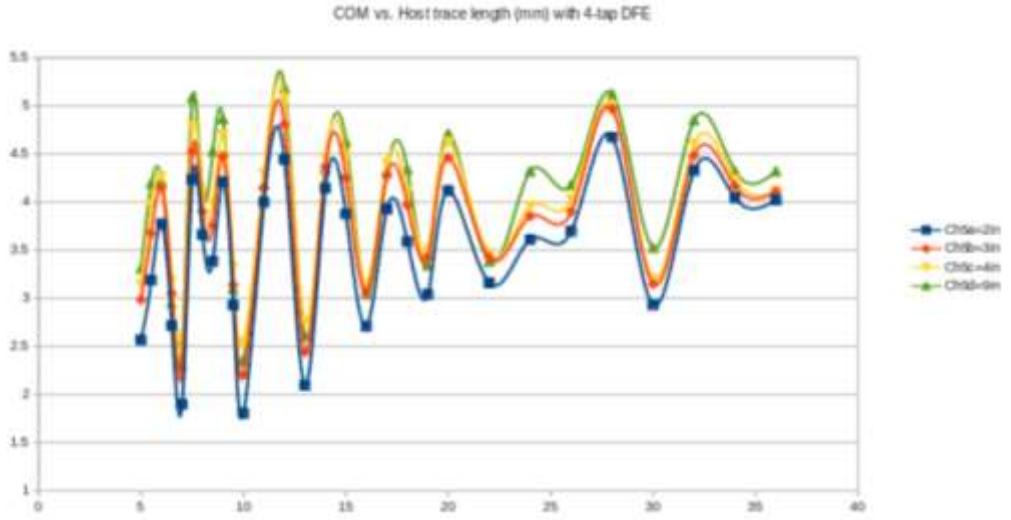
Spec	[Host, Module]	Unit
C_d	[1.2e-4 0.85e-4	nF
L_s	[0.12 0.12]	nH
C_b	[0.3e-4 0.3e-4]	nF
R_d	[50 50]	Ohm
C_p	[0.87 0.87]	nF
z_p(RX)	[8 0]	Ohm

Table 1b: PKG2

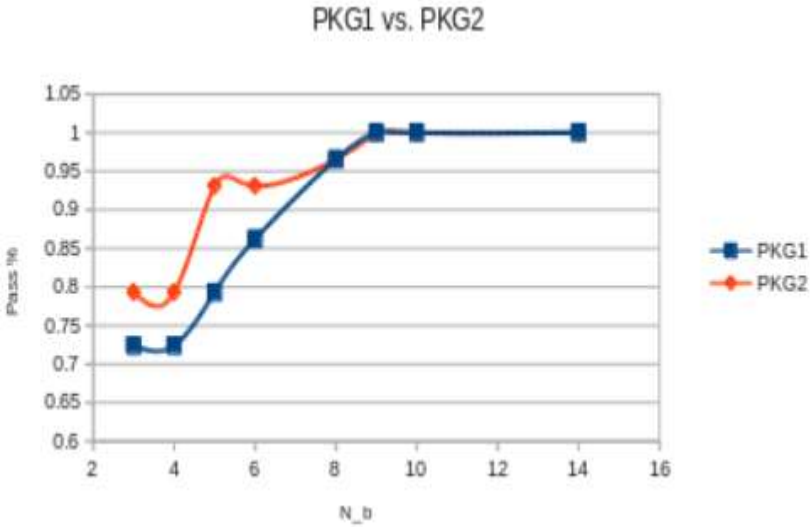
Spec	[Host, Module]	Unit
C_d	[1.2e-4 0.85e-4	nF
L_s	[0.12 0.12]	nH
C_b	[0.3e-4 0.3e-4]	nF
R_d	[50 50]	Ohm
C_p	[0.87 ~~0.87~~ → **0.65**]	nF
z_p(RX)	[~~8~~→**5** 0]	Ohm

Sweeping Host Trace Length

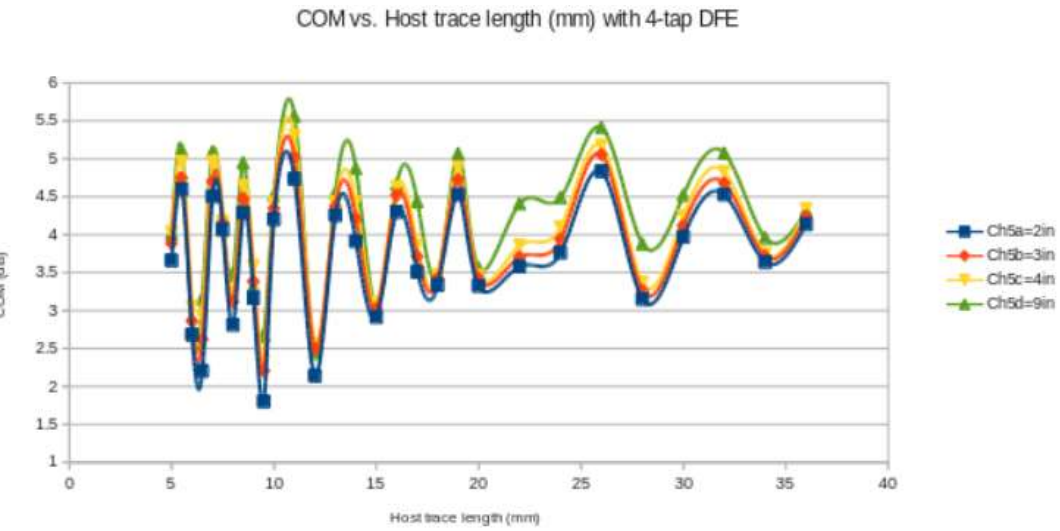
PKG1: C_p(RX)=87fF, zp_1(RX)=8mm



Ch5a: 2”



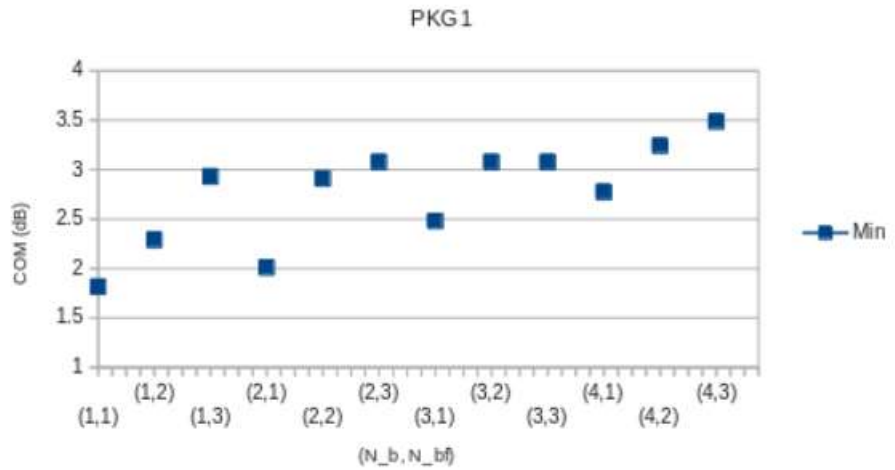
PKG2: C_p(RX)=65fF, zp_1(RX)=5mm

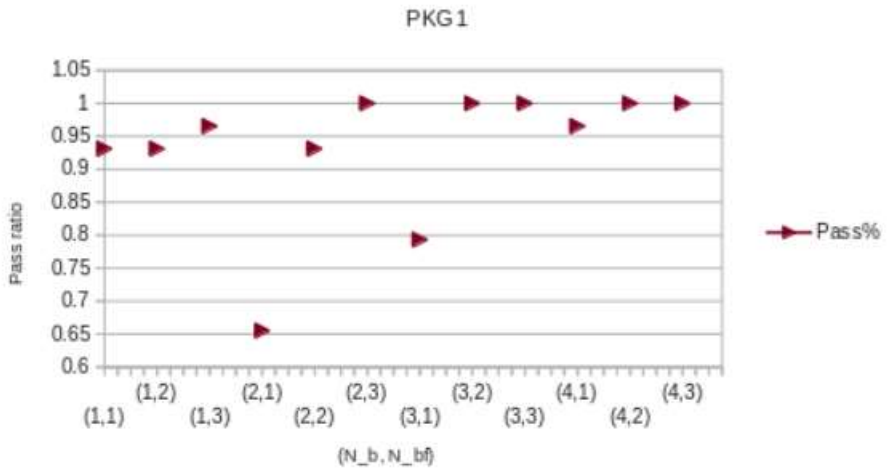


- Observing the change PKG1 to PKG2
- Location of valley
  - Slightly shift due to 8mm vs. 5mm
- COM values of valley
  - Slightly improve around 0.3 dB
- It still requires 9-tap DFE to pass 3 dB for all host trace lengths

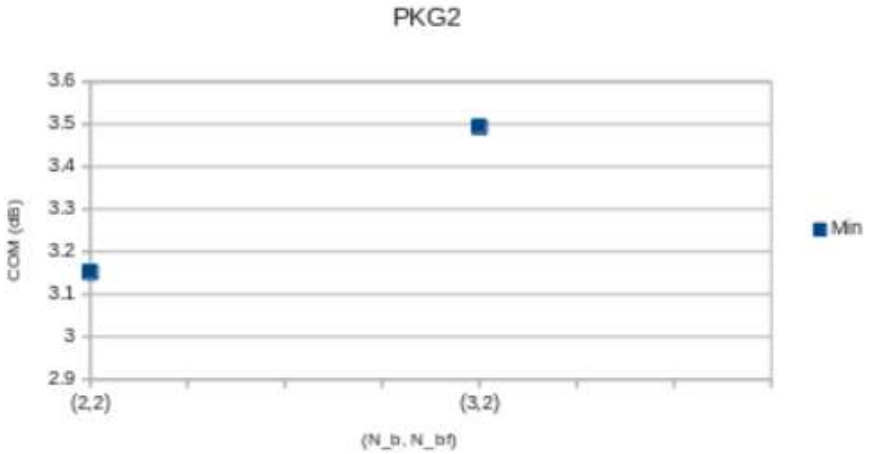
Min of COM & Pass Ratio, Floating – Ch5a

PKG1: C_p(RX)=87fF, zp_1(RX)=8mm





PKG2: C_p(RX)=65fF, zp_1(RX)=5mm



- It still requires total 4-tap (2-fixed + 2-float) DFE to pass 3 dB for all host trace lengths under PKG2
  - PKG1 requires total 5-tap

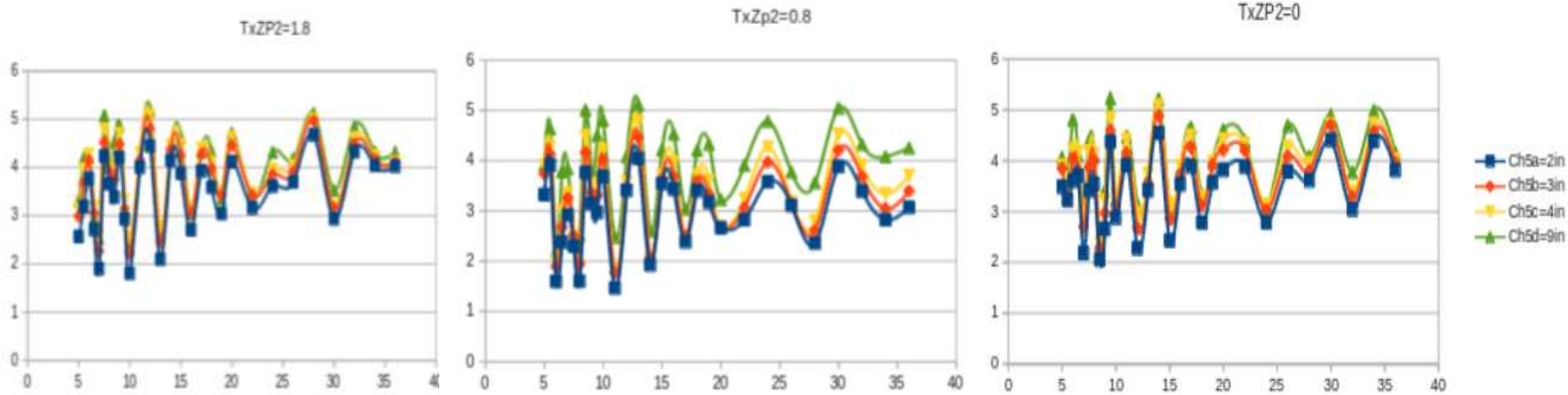
Summary

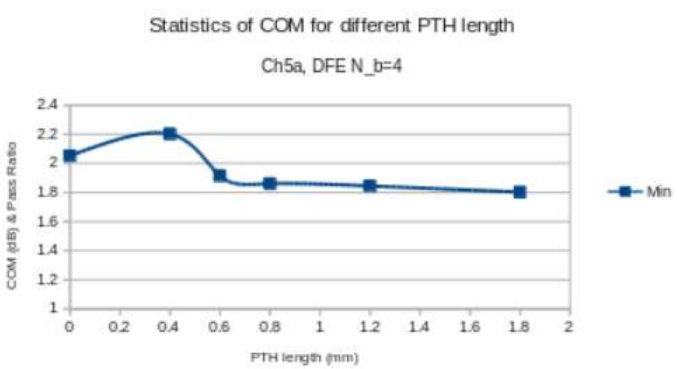
- Performance of host to module link with short channel is sensitive to Host trace length
  - Can't be conquered by adding design constraints on host trace length
  - Can't be conquered by adjusting PTH length or R_d
  - Could be conquered by floating-tap
- Total 5-tap DFE (3-fixed + 2-float) can make Jane's Channel 5a-5d pass 3 dB for 5 to 36 mm host trace length
  - 4-tap DFE (2-fixed + 2-float) by reducing module PKG settings
- Next
  - Need to check the results of other C2M channels

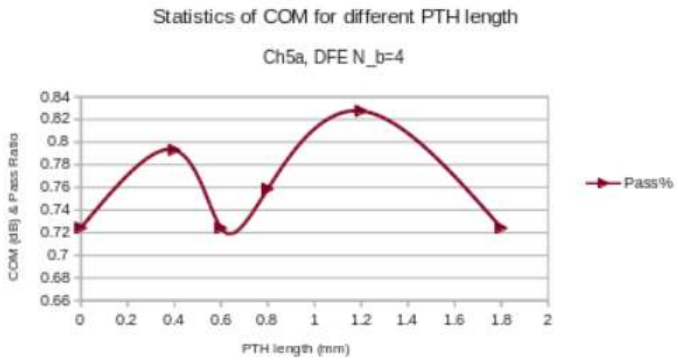
everyday genius

Changing z_p2(TX)

- RX = DFE 4-tap, COM (dB) vs. host trace length (mm)







FOM Analysis of Each Source

- Motivation
  - FOM is defined in Annex 93A to analyze impact from different sources
    - TX, ISI, Jitter, Crosstalk, Noise
- We defined FOM_TX as
  - FOM (dB) with others set to ‘zero’
- We defined FOM_ISI, FOM_J, FOM_XT, and FOM_N similarly
- We found ISI as key source for ‘fluctuation’ of COM
  - Details in next slide

$$\sigma_X^2 = \frac{L^2 - 1}{3(L-1)^2}$$

$$\sigma_{TX}^2 = [h^{(0)}(t_s)]^2 10^{-SNR_{TX}/10}$$

$$\sigma_{ISI}^2 = \sigma_X^2 \sum_n h_{ISI}^2(n)$$

$$\sigma_J^2 = (A_{DD}^2 + \sigma_{RJ}^2)\sigma_X^2 \sum_n h_J^2(n)$$

$$[\sigma_m^{(k)}]^2 = \sigma_X^2 \sum_n [h^{(k)}((m/M + n)T_b)]^2$$

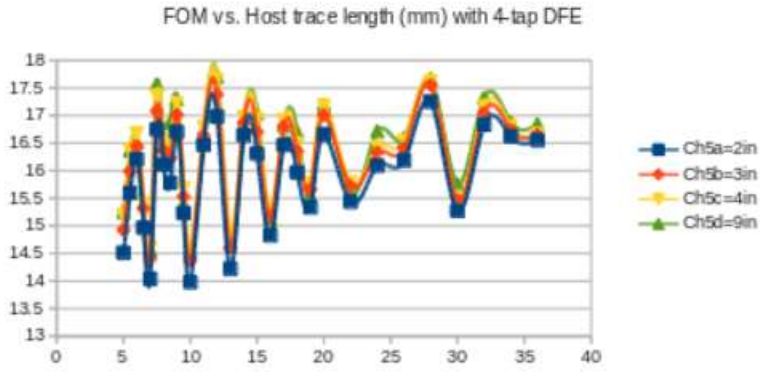
$$\sigma_{XT}^2 = \sum_{k=1}^{K-1} [\sigma_i^{(k)}]^2$$

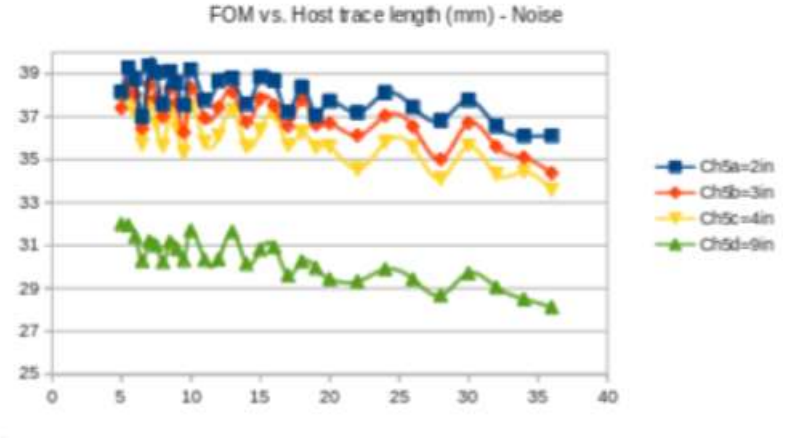
$$\sigma_N^2 = \eta_0 \int_0^\infty |H_r(f)H_{ctf}(f)|^2 df$$

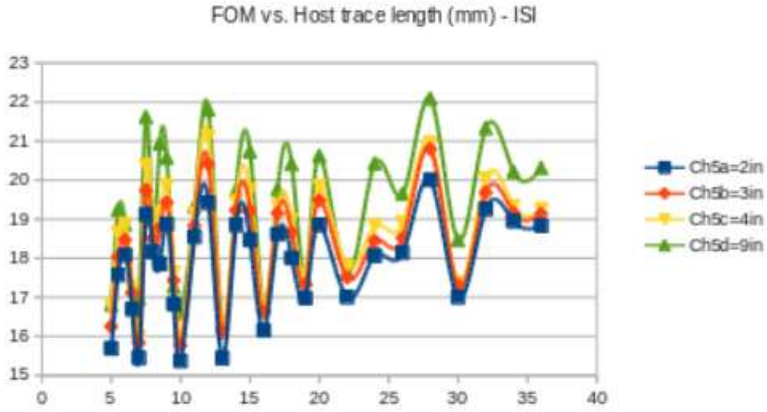
$$FOM = 10\log_{10}\left(\frac{A_s^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2}\right)$$

FOM Analysis

- RX = DFE 4-tap, FOM_x (dB) vs. host trace length (mm)



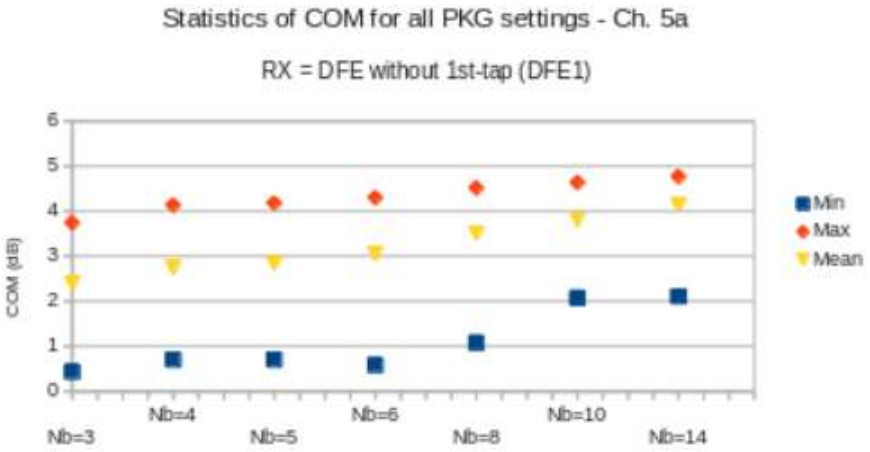


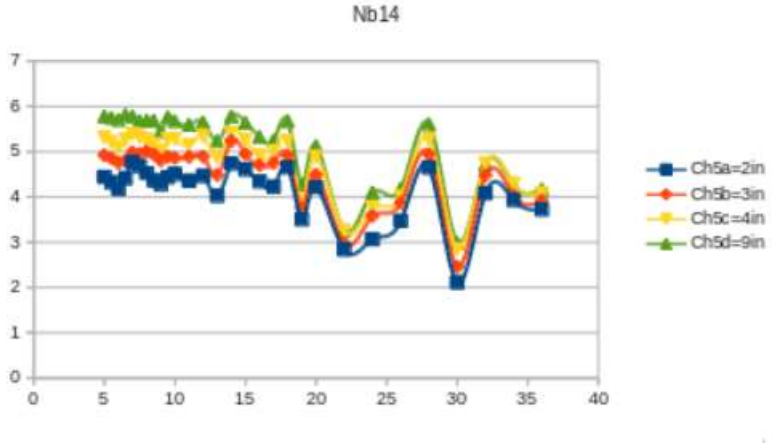


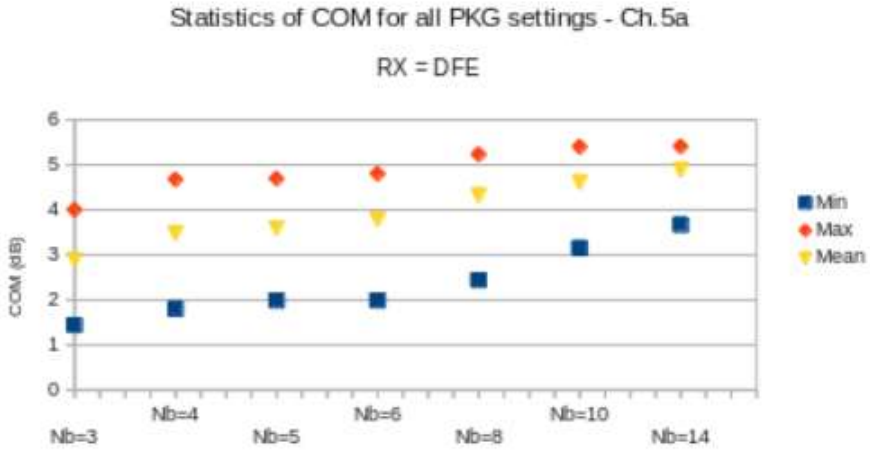
- ISI is key contributor to FOM
  - Sensitive to host trace length
  - Align to 'valley' among all range
  - Majorly due to 'reflections'
- Ch5d has higher noise, but noise level is small comparing to other sources
  - All above 27 dB
  - Not key contributors

Whole Link Performance – DFE1

- RX = DFE without 1st-tap, COM (dB) vs. host trace length (mm)

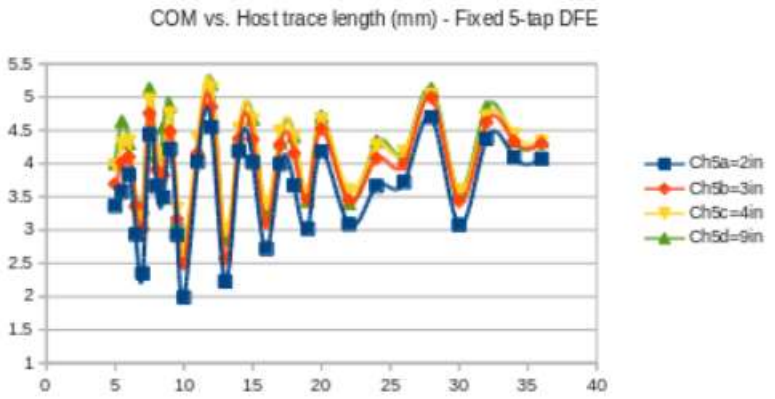


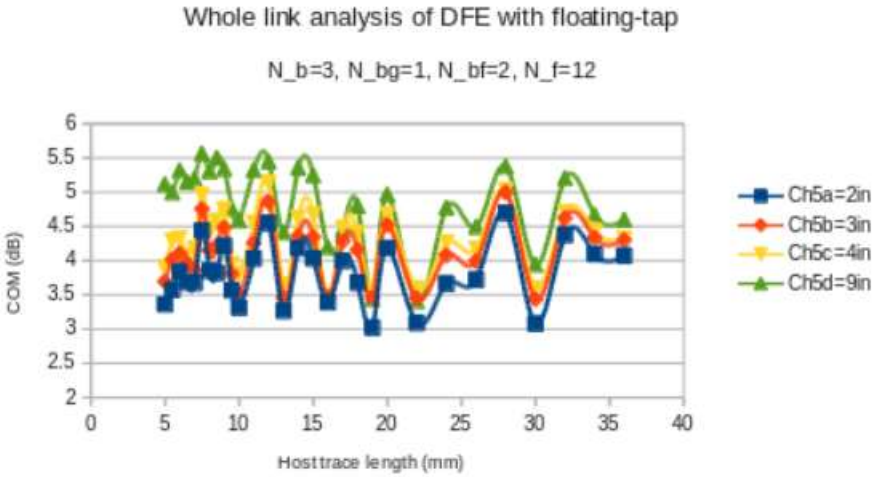


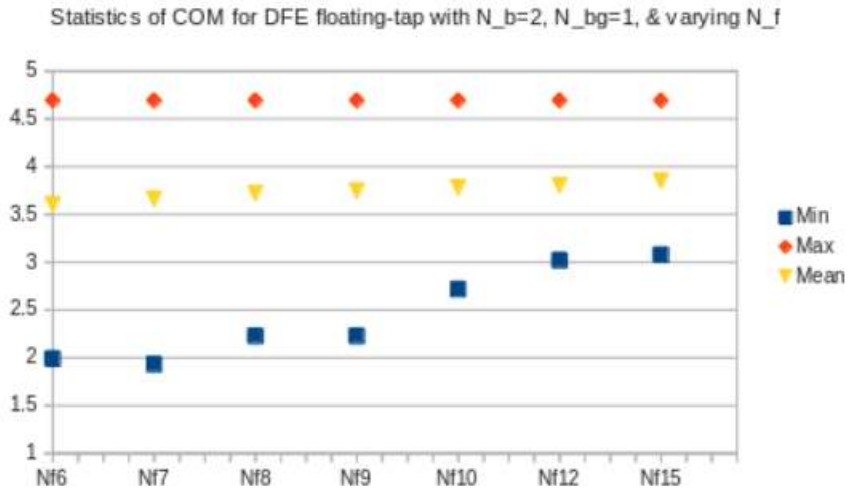


- Comparing to DFE, DFE1 is much worse
  - Around 0.5 ~ 1.0 dB COM loss
  - Even N_b=14 can't achieve 3 dB COM

Efficient Approach to Cancel Reflection







- Just 2 floating-tap can efficiently cancel "reflection" due to PKG
  - Floating-tap spanning to 12 UI can cancel "reflection" due to 16 mm host trace
  - COM improves up to 1 dB comparing to DFE with 5 fixed-tap
- COM sensitivity to floating-tap span (N_f)
  - N_f = 12 is the sweet point

COM Settings – Whole Link

le 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0.85e-4]	nF	[TX RX]
L_s	[0.12 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[2 8; 0 0]	mm	[test cases]
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]
z_p (RX)	[2 8; 0 0]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02:0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	3	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[2 1 4 3]	
RUNTAG	KR_eval	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include_PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	1	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma_BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92-12 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
N_f	40	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps

yellow indicates WIP

PS: Ran for test case 2 only

COM Settings – TP1a

le 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02:0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	3	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL KR {date}\	
SAVE_FIGURES	1	logical
Port Order	[2 1 4 3]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	1	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma_BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92-12 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
N_f	40	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps

yellow indicates WIP

PS: Ran for test case 2 only

Floating Tap – Mean/Min/Max