C2M TP1a VEC and ERL Test Specs

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IEEE 802.3ck Task Force

Outline

- Background
- Channels and COM Settings for Analysis
- TP1a VEC Spec
- ERL sensitivity to test fixture
- Summary

TP1a VEC and H2M Short Channel Issue

- There were a lot of previous contributions focusing on TP1a VEC spec
  - sun_3ck_01b_0119, sun_3ck_01_0319, sun_3ck_01_0519, li_3ck_01_0319, li_3ck_02a_0519, wu_3ck_01a_0919
- The followings proposed the ideas of combining VEC & VEO specs
  - ghiasi_3ck_02a_0919, sun_3ck_01b_0919, wu_3ck_adhoc_01_101619, sun_3ck_adhoc_02_103019
- Host-2-module short channel issue were discussed in the following contributions
  - li_3ck_02a_0519, dudek_3ck_01_0719, sun_3ck_adhoc_01_081419, akinwale_3ck_adhoc_01a_08282019, wu_3ck_01a_0919, dudek_3ck_01_0919, sun_3ck_01b_0919, wu_3ck_adhoc_02_101619
- C2M ERL spec was discussed in the following contributions
  - mellitz_3ck_02_0319, mellitz_3ck_adhoc_01a_032719, mellitz_3ck_adhoc_01a_042419, mellitz_3ck_02a_0519

Channel and Analysis

- Channel and reference receiver
  - Whole-link & TP1a analysis for total 19 IEEE C2M host-to-module channels
    - Sweep host package trace length, z_p1(TX)
      - z_p1(TX) = [5:0.5:10 11:1:20 22:2:36]
    - total 19 * 29 = 551 CH+PKG test cases
  - RX with sweeping tap number
    - DFE with 4 taps
- COM parameter settings [details in appendix]
  - COM 2.75
  - Whole link: TX PKG + H2M Channels + RX PKG
    - On-die
      - Host [healey_3ck_adhoc_01_061219]
      - Module: Table 1
    - PKG
      - Host [baseline]
      - Module: Table 1
    - g_DC = [-14:1:0] dB
    - g_DC_HP = [-3:1:0] dB
  - TP1a: TX PKG + H2M Channels
    - Set ‘zero’ to related RX PKG & on-die settings

Table 1

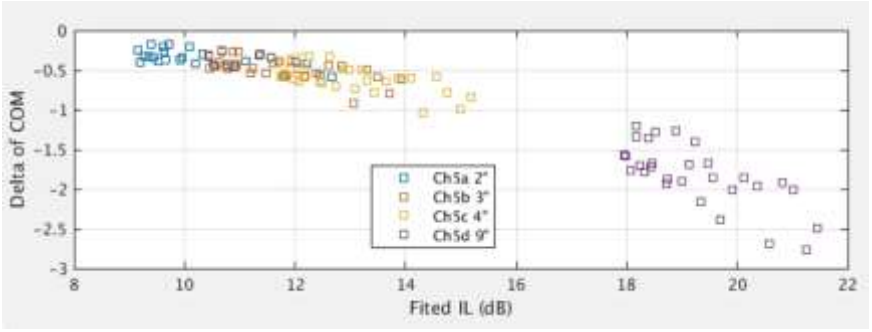
Spec	[Host, Module]	Unit
C_d	[1.2e-4 0.85e-4]	nF
L_s	[0.12 0.12]	nH
C_b	[0.3e-4 0.3e-4]	nF
R_d	[50 50]	Ohm
C_p	[0.87 0.65]	nF
z_p(RX)	[5 0]	Ohm

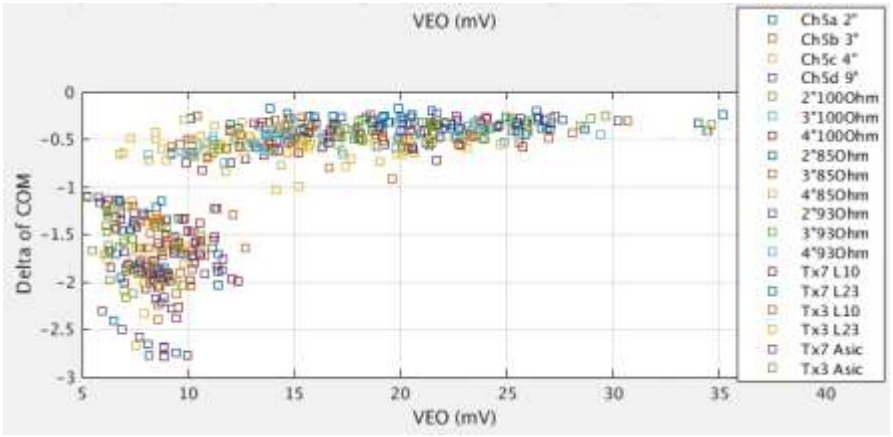
TP1a VEC and VEO Specs

- In wu_3ck_adhoc_01_101619, we explored VEC and VEO combined spec by exploring 19 channels with 29 host PKG trace lengths
  - Analyzed by considering false ratios by 3dB COM
- In sun_3ck_adhoc_02_103019, 2.6mV receiver noise had been added for whole-link COM simulation
  - Proposed EVEC based on simulation results
- We explored EVEC by 19 C2M channels
  - Add 2.0mV receiver noise with Effective COM (ECOM) >= 1.5 dB as criterion
    - Refer to wu_3ck_01a_0519 for receiver noise modeling
    - ECOM is the whole-link COM by adding 2.0mV RX noise
  - EVEC vs. COM gets better correlation
    - Refer to sun_3ck_adhoc_02_103019 or wu_3ck_adhoc_01_101619 for EVEC methodology
  - Proposed the following EVEC parameters

$$\mathrm{EVEC}(i) = \begin{cases} VEC(i), & if\ VEO(i) < 10mV \\ VEC(i) - 0.3333 \times (VEO(i) - 10)dB, & if 10mV \le VEO(i) < 25mV \\ VEC(i) - 5dB & otherwise \end{cases}$$

Impact of 2mV Receiver Noise

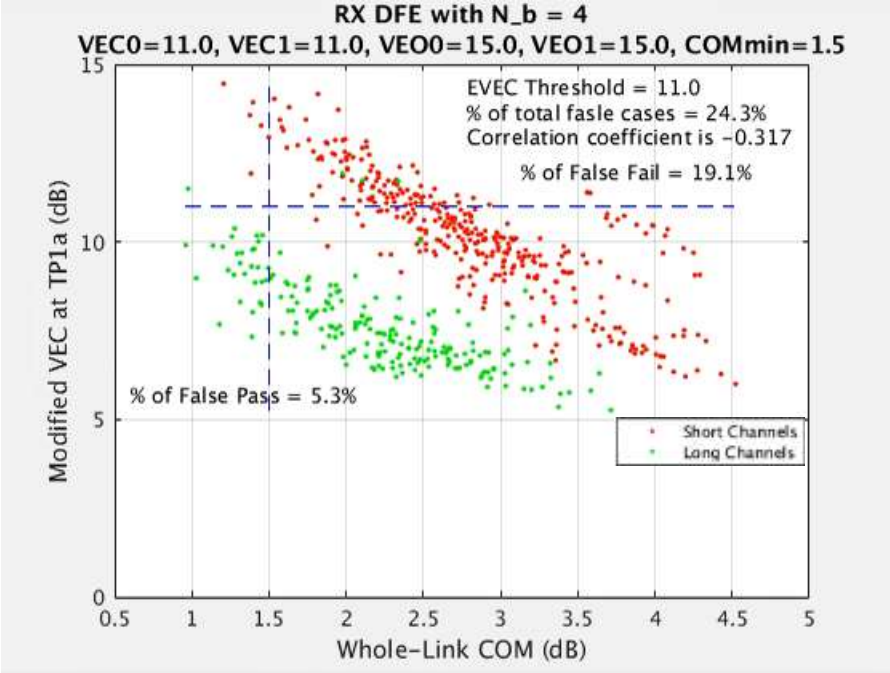




- 3dB minimum COM limit topic had been explored in healey_3ck_01_0319
  - 3dB for RX noise, sampling clock jitter, approximation errors, …
- A lot of C2M short channels fail 3dB COM for several TX package lengths
  - wu_3ck_01a_0919
- Add 2mV RX noise in whole-link analysis
  - Set COM results as ECOM
  - Delta of COM = COM(2mV) – COM(0mV)
- COM loss due to RX noise
  - 0.5 ~ 1.0 dB for short channels, 1.5 ~ 2.5 dB for long channels
  - COM loss is also correlated to VEO
- COM_{min} = 3.0 dB for short channel may be too pessimistic
  - $ECOM_{min}$ = 1.5 dB shall be OK
  - Apply EVEC at TP1a & make sure it's correlated to ECOM
  - C2M short channel issue is NOT severe as we previously thought

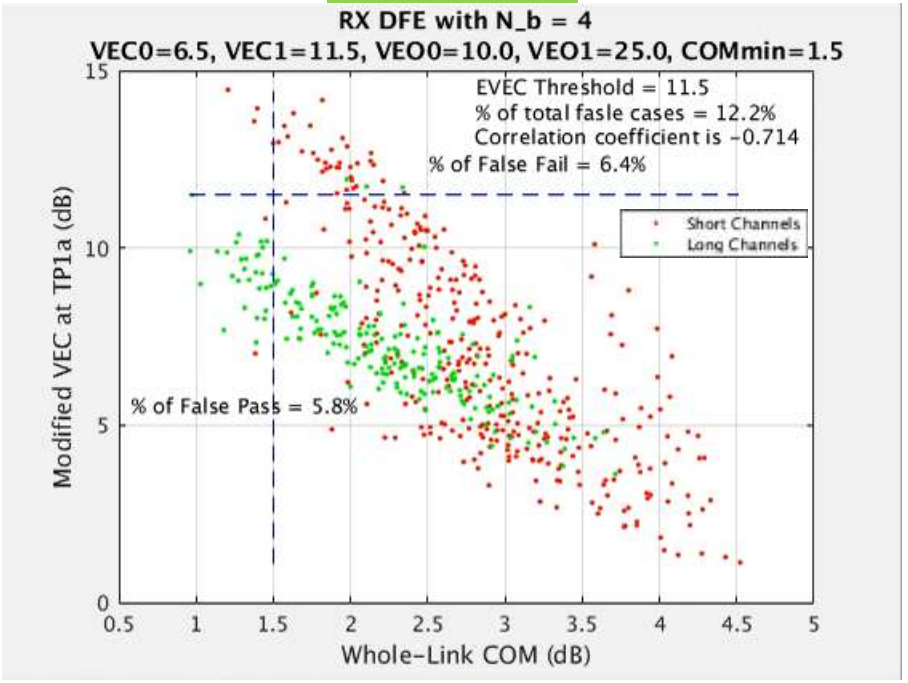
EVEC Improves Correlation to COM

No EVEC



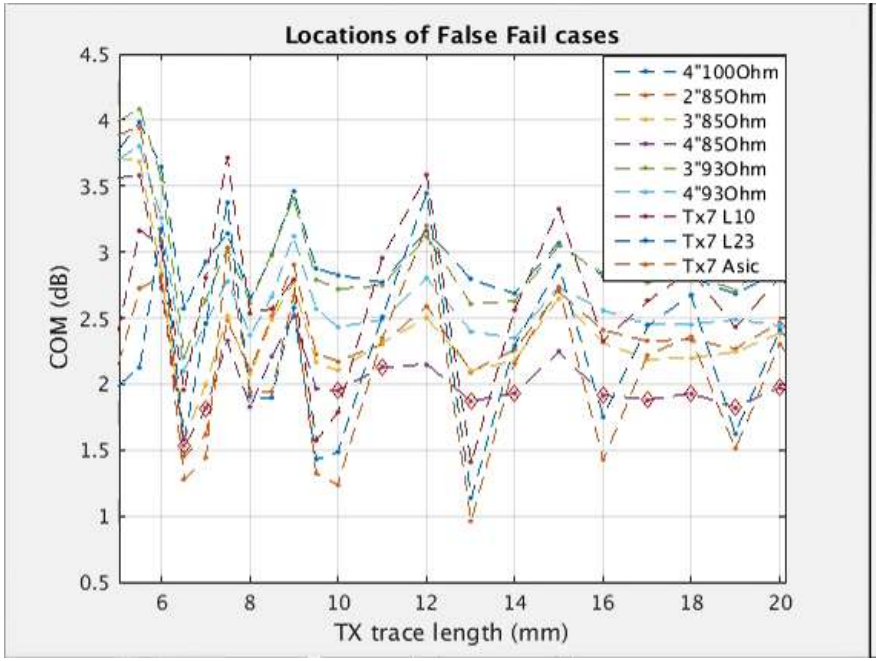
- Short and long channels are grouped obviously
  - but correlation coefficient (CC) is low (-0.317)
- Difficult to set VEC_{max}
  - VECmax = 11 dB, % of False case = 24.3%
  - False Fail: majorly 'short channels'

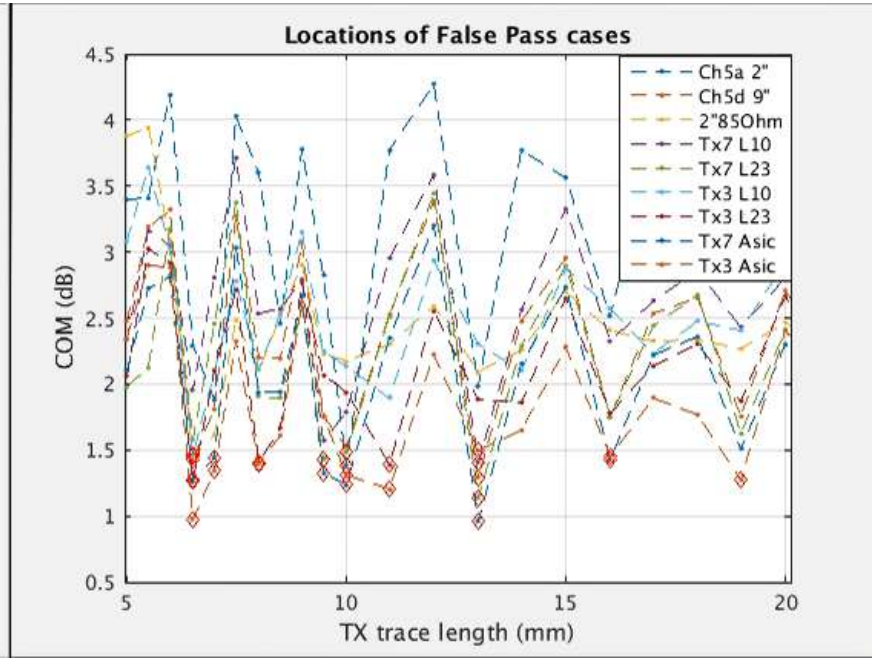
Proposal



- Correlation has improved a lot
  - -0.317 → -0.714
- False %: improve from 24.3% to 12.2%
  - Most on False Fail
  - Little on False Pass

False Pass and False Fail Cases





$$\mathrm{EVEC}(i) = \begin{cases} VEC(i), & if\ VEO(i) < 10mV \\ VEC(i) - 0.3333 \times (VEO(i) - 10)dB, & if 10mV \le VEO(i) < 25mV \\ VEC(i) - 5dB & otherwise \end{cases}$$

C2M ERL Spec

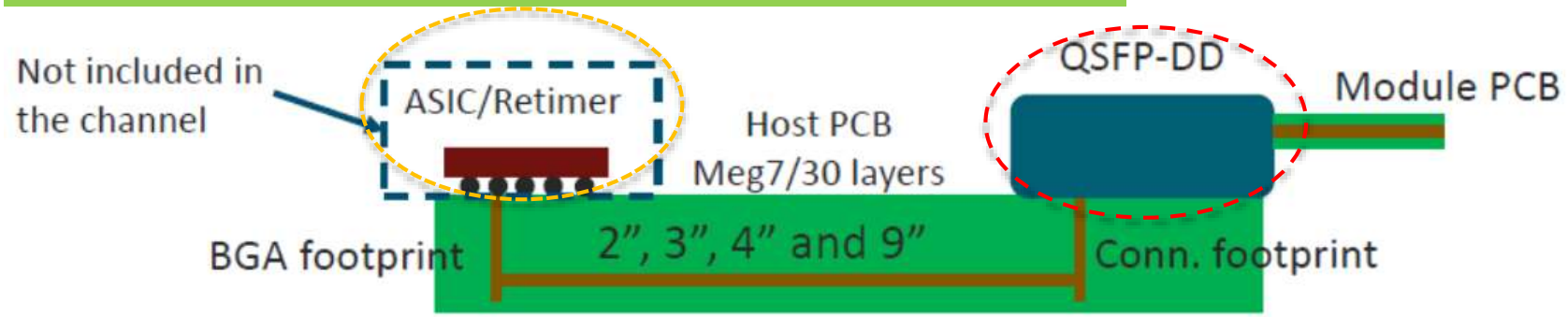
136.9.3.4 Transmitter effective return loss (ERL)

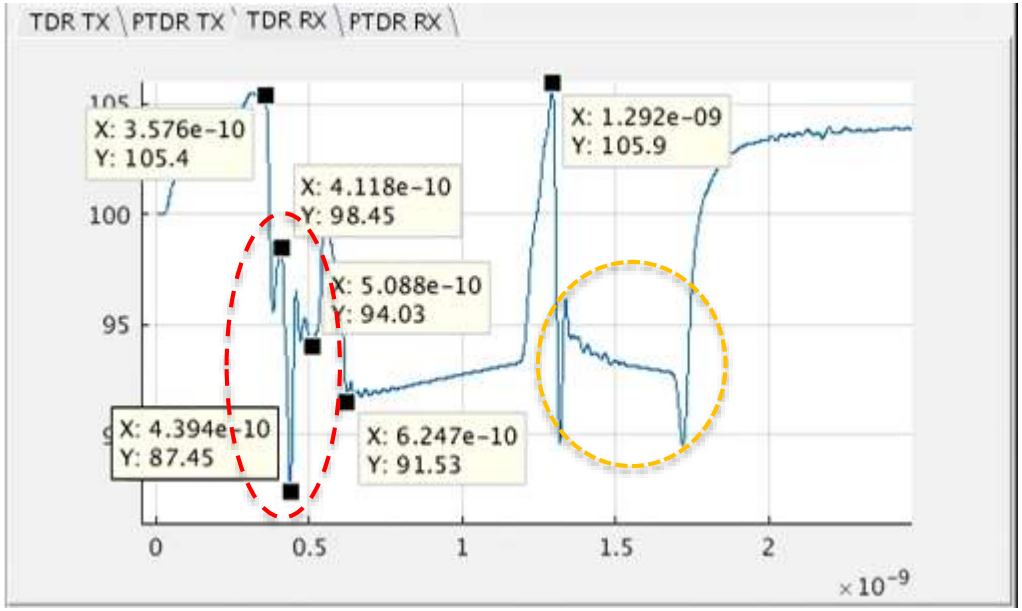
ERL of the transmitter at TP2 is computed using the procedure in 93A.5 with the values in Table 136–13. Parameters that do not appear in Table 136–13 take values from Table 136–18. The value of T_{fx} is twice the delay associated with the TP2 test fixture being used. N_{bx} is set to the value of N_b in Table 136–18.

- Idea: leverage 50G-CR ERL & change TP2 to TP1a?
  - TX ERL is sensitive to T_{fx} and we shall define clearly the meaning of '*twice the delay associated with the TP1a test fixture being used*'
- Is it straight forward?
- Suggestion
  - To have more specific definitions of T_{fx}

What's T_{fx}?

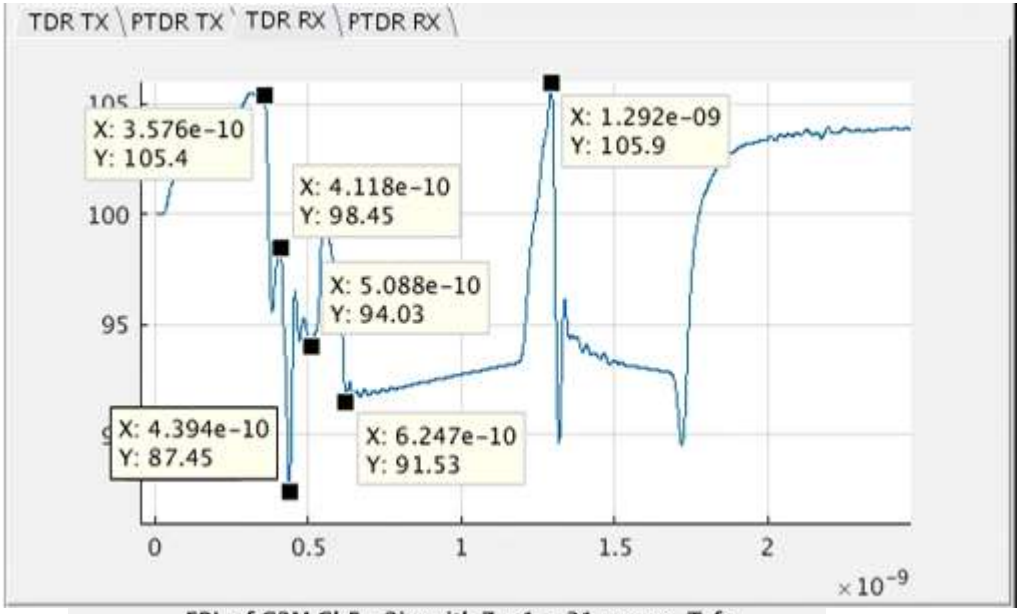
Lim's C2M short channels, lim_3ck_adhoc_01_073119

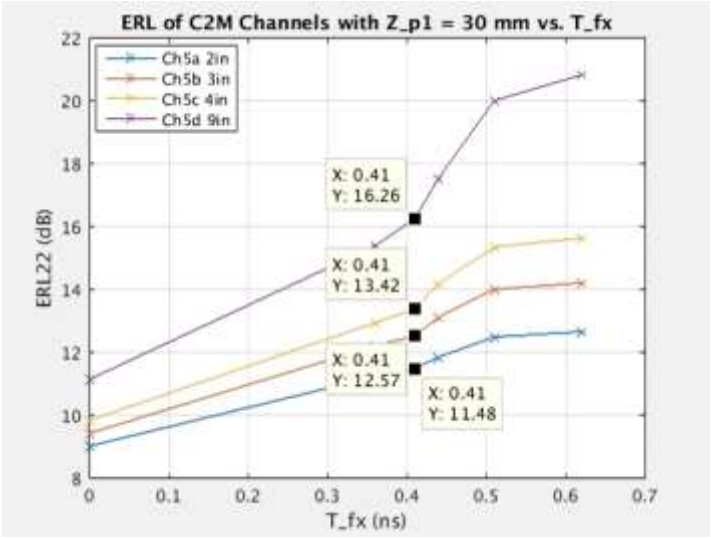


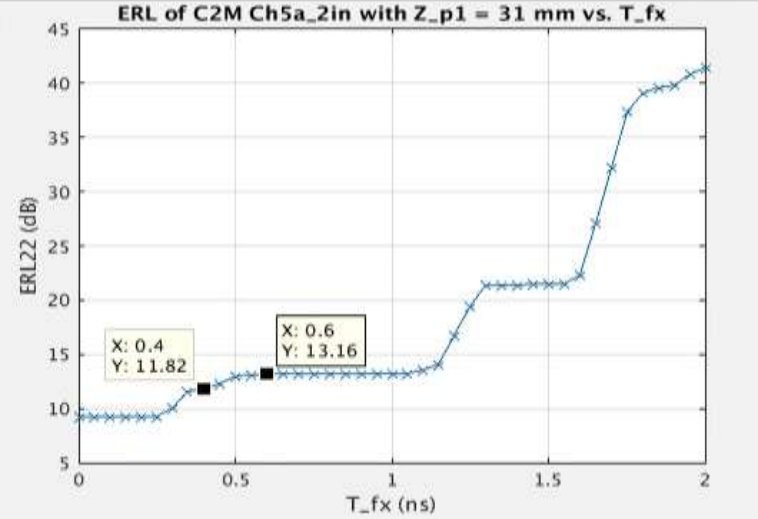


- Where is the TP1a point? T_{fx} = ?
  - 3.58e-10, 4.12e-10, … or 6.25e-10
- Shall include QSFP-DD?
  - Take 4.1e-10
- ERL22 is sensitive to T_{fx}
  - Shall we have more specific definitions for T_{fx}?

ERL Sensitivity to T_{fx}







- ERL22 is sensitive to T_{fx} = ?
  - Yes
  - Be careful to exclude 'TP1a test fixture', while include QSFP-DD or OSFP
- ERL22 of Jane Lim's C2M short channels (by T_{fx} = 0.41ns)

Channel	2in	3in	4in	9in
ERL22 (dB)	11.48	12.57	13.42	16.26

Summary

- By DFE reference receiver, 4-tap DFE has good correlation for TP1a EVEC vs. whole-link COM plus RX noise
  - With total false ratio = 12.2% with -0.71 correlation
  - Propose the following EVEC parameters

$$\mathrm{EVEC}(i) = \begin{cases} VEC(i), & if\ VEO(i) < 10mV \\ VEC(i) - 0.3333 \times (VEO(i) - 10)dB, & if 10mV \le VEO(i) < 25mV \\ VEC(i) - 5dB & otherwise \end{cases}$$

- C2M TP1a ERL is sensitive to T_{fx}
  - Suggest to have more specific definition of TP1a test fixture and T_{fx} accordingly

everyday genius

C2M Channels for Analysis

Contribution	Zip files	Channel	SxP Files
lim_3ck_01a_0319	lim_3ck_01_0319_c2m.zip	Tx7_L10	112G_16dB_(QSFPDD+module card)_TX7_L10
		Tx7_L23	112G_16dB_(QSFPDD+module card)_TX7_L23
		Tx3_L10	112G_16dB_(QSFPDD+module card)_TX3_L10
		Tx3_L23	112G_16dB_(QSFPDD+module card)_TX3_L23
		Tx7_Asic	112G_16dB_(QSFPDD+module card)_TX7_Asic
		Tx3_Asic	112G_16dB_(QSFPDD+module card)_TX3_Asic
lim_3ck_adhoc_01_073119	lim_3ck_adhoc_02_073119.zip	Ch5a_2"	Channel5a_Smaller_Pad_2inch_trace
		Ch5b_3"	Channel5b_Smaller_Pad_3inch_trace
		Ch5c_4"	Channel5c_Smaller_Pad_4inch_trace
		Ch5d_9"	Channel5d_Smaller_Pad_9inch_trace
akinwale_3ck_adhoc_01a_08282019	akinwale_3ck_C2M_channels_TP0a_100ohms_08222019.zip	2''100Ohm	C2M_2p0in_100Ohm_thru1.s4p
		3''100Ohm	C2M_3p0in_100Ohm_thru1.s4p
		4''100Ohm	C2M_4p0in_100Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_85ohms_08222019.zip	2''85Ohm	C2M_2p0in_85Ohm_thru1.s4p
		3''85Ohm	C2M_3p0in_85Ohm_thru1.s4p
		4''85Ohm	C2M_4p0in_85Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_93Ohms_08222019.zip	2''93Ohm	C2M_2p0in_93Ohm_thru1.s4p
		3''93Ohm	C2M_3p0in_93Ohm_thru1.s4p
		4''93Ohm	C2M_4p0in_93Ohm_thru1.s4p

COM Settings – Whole Link

Table 93A-1 parameters					I/O control				Table 93A3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_KR_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0.85e-4]	nF	[TX RX]		SAVE_FIGURES	1	logical				
L_s	[0.12, 0.12]	nH	[TX RX]		Port Order	[2 1 4 3]			Table 92E2 parameters 5.2dB at 26.56GHz		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	KR_eval_			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 5; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	102.7	mm
z_p (RX)	[2 5; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	102.7	mm
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	102.7	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	102.7	mm
R_d	[50 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.39	V	vp/vf=.694		TDR and ERL options						
A_fe	0.39	V	vp/vf=.694		TDR	1	logical		Floating Tap Control		
A_ne	0.578	V			ERL	1	logical		N_bg	0	0 1 2 or 3 groups
L	4				ERL_ONLY	0	logical		N_bf	0	taps per group
M	32				TR_TDR	0.01	ns		N_f	40	UI span for floating taps
filter and Eq					N	3000			bmaxg	0.2	max DFE value for floating taps
f_r	0.75	*fb			beta_x	2.53E+09					
c(0)	0.54		min		rho_x	0.25					
c(-1)	[-0.26:0.02:0]		[min:step:max]		fixture delay time	0	s				
c(-2)	[0:0.02:0.10]		[min:step:max]		TDR_W_TXPKG	1					
c(-3)	[-0.04:0.02:0]		[min:step:max]		N_bx	24	UI		yellow indicates WIP		
c(1)	[-0.2:0.05:0]		[min:step:max]		Receiver testing						
N_b	4	UI			RX_CALIBRATION	0	logical				
b_max(1)	0.5				Sigma BBN step	5.00E-03	V				
b_max(2..N_b)	0.2				Noise, jitter						
g_DC	[-14:1:0]	dB	[min:step:max]		sigma_RJ	0.01	UI				
f_z	21.25	GHz			A_DD	0.02	UI				
f_p1	21.25	GHz			eta_0	8.20E-09	V^2/GHz				
f_p2	53.125	GHz			SNR_TX	33	dB				
g_DC_HP	[-3:1:0]		[min:step:max]		R_LM	0.95					
f_HP_PZ	0.6640625	GHz									

PS: Ran for test case 2 only

COM Settings – TP1a

Table 93A-1 parameters					I/O control				Table 93A~~3~~ parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_KR_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	1	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[2 1 4 3]			Table 92~~1~~2 parameters 5.2dB at 26.56GHz		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	KR_eval_			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	102.7	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	102.7	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	102.7	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	102.7	mm
R_d	[50 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.39	V	vp/vf=.694		TDR and ERL options						
A_fe	0.39	V	vp/vf=.694		TDR	1	logical		Floating Tap Control		
A_ne	0.578	V			ERL	1	logical		N_bg	0	0 1 2 or 3 groups
L	4				ERL_ONLY	0	logical		N_bf	0	taps per group
M	32				TR_TDR	0.01	ns		N_f	40	UI span for floating taps
filter and Eq					N	3000			bmaxg	0.2	max DFE value for floating taps
f_r	0.75	*fb			beta_x	2.53E+09					
c(0)	0.54		min		rho_x	0.25					
c(-1)	[-0.26:0.02:0]		[min:step:max]		fixture delay time	0	s				
c(-2)	[0:0.02:0.10]		[min:step:max]		TDR_W_TXPKG	1					
c(-3)	[-0.04:0.02:0]		[min:step:max]		N_bx	24	UI		yellow indicates WIP		
c(1)	[-0.2:0.05:0]		[min:step:max]		Receiver testing						
N_b	4	UI			RX_CALIBRATION	0	logical				
b_max(1)	0.5				Sigma BBN step	5.00E-03	V				
b_max(2..N_b)	0.2				Noise, jitter						
g_DC	[-14:1:0]	dB	[min:step:max]		sigma_RJ	0.01	UI				
f_z	21.25	GHz			A_DD	0.02	UI				
f_p1	21.25	GHz			eta_0	8.20E-09	V^2/GHz				
f_p2	53.125	GHz			SNR_TX	33	dB				
g_DC_HP	[-3:1:0]		[min:step:max]		R_LM	0.95					
f_HP_PZ	0.6640625	GHz									

PS: Ran for test case 2 only

COM Settings – ERL Calculation

able 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.26:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.10]		[min:step:max]
c(-3)	[-0.04:0.02:0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	4	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[2 1 4 3]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	1	logical
TR_TDR	0.01	ns
N	2000	
beta_x	2.34E+09	
rho_x	**0.3**	
fixture delay time	0	s
TDR_W_TXPKG	1	
N_bx	4	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A? parameterss		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92?2 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

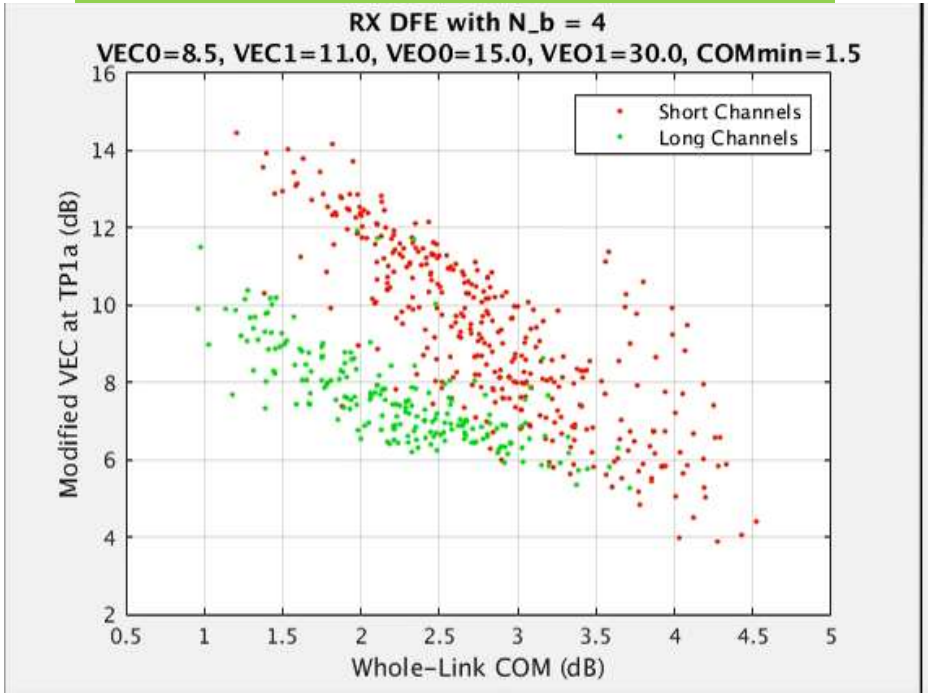
Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
N_f	40	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps

yellow indicates WIP

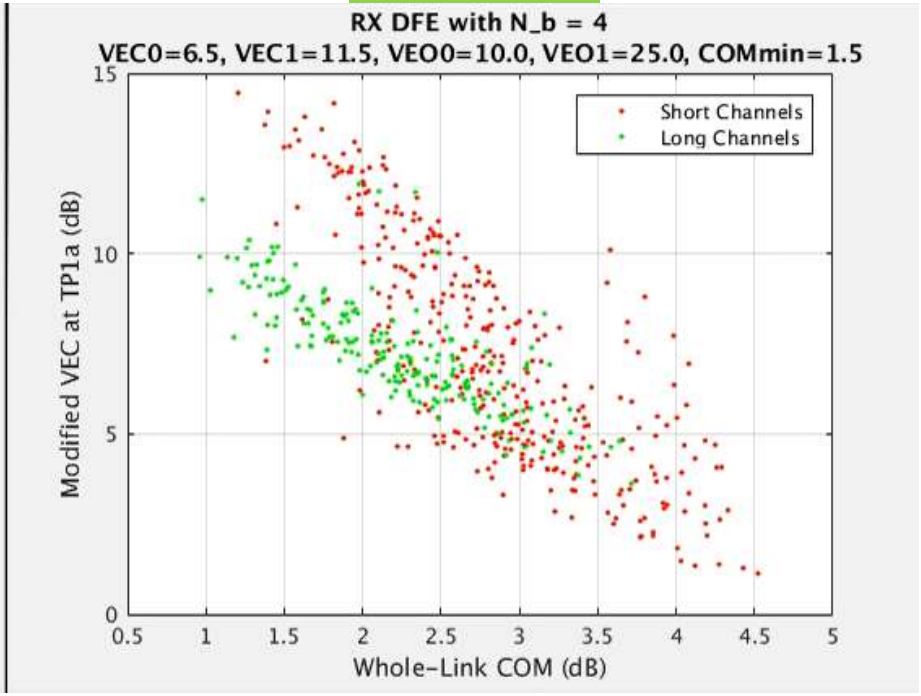
PS: Ran for test case 2 only

EVEC Parameters Comparison: Distribution

sun_3ck_adhoc_02_103019

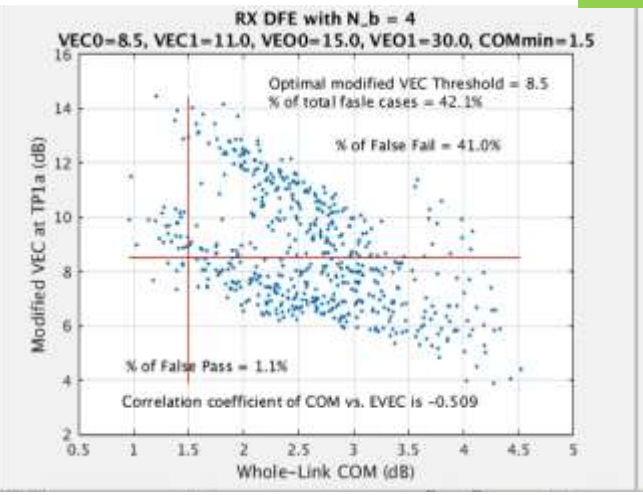


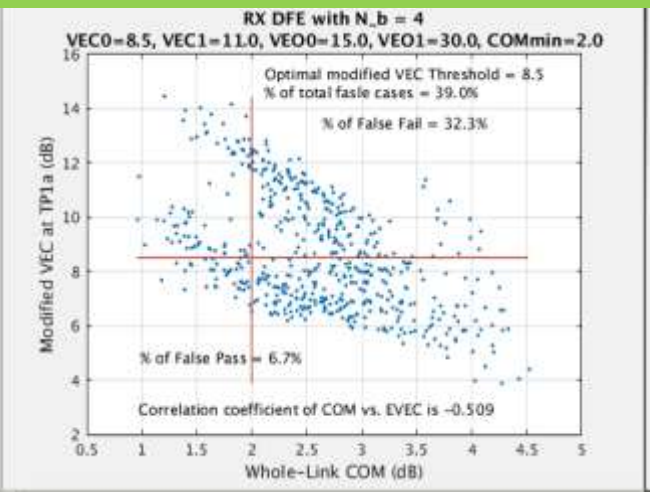
Proposal

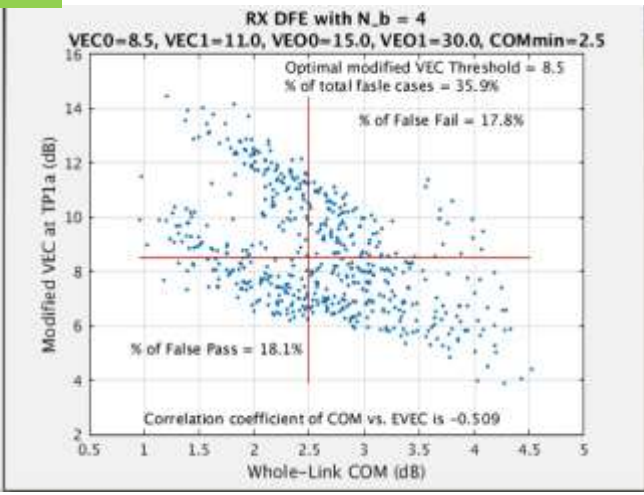


EVEC Parameters Comparison: False % & CC

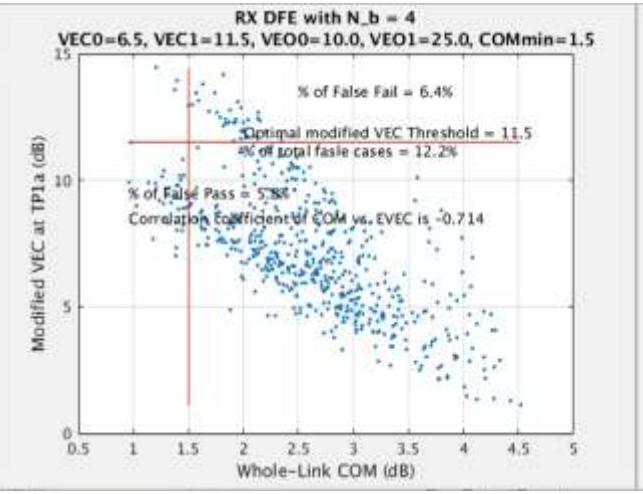
sun_3ck_adhoc_02_103019

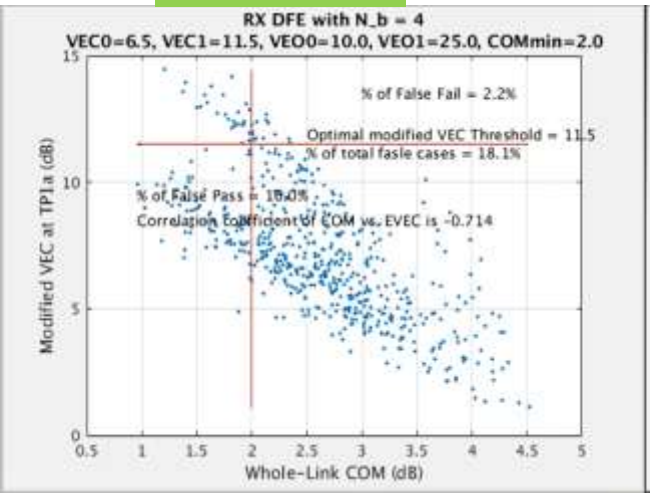


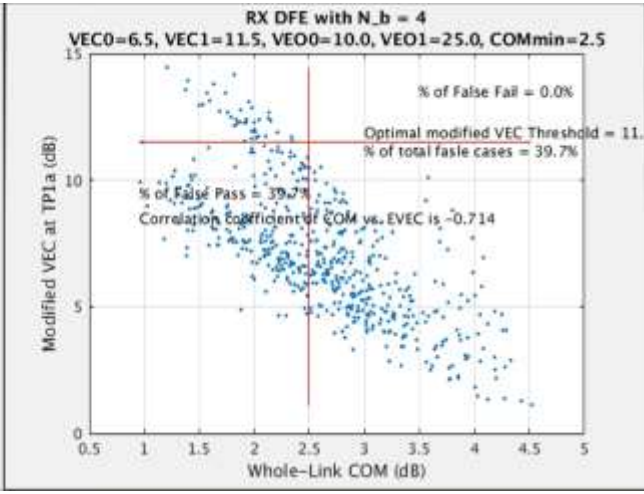




Proposal







ERL is NOT sensitive to Z_p1