Study of KR ERL Test Spec

Mau-Lin Wu, Po-Hsiang Huang
MediaTek

IEEE 802.3ck Task Force

Contributors

- Pei-Rong Li, MediaTek

Outline

- Backgrounds and motivations
- Channel and COM settings
- ERL analysis with TP0a test fixture
- ERL sensitivity
- Summary

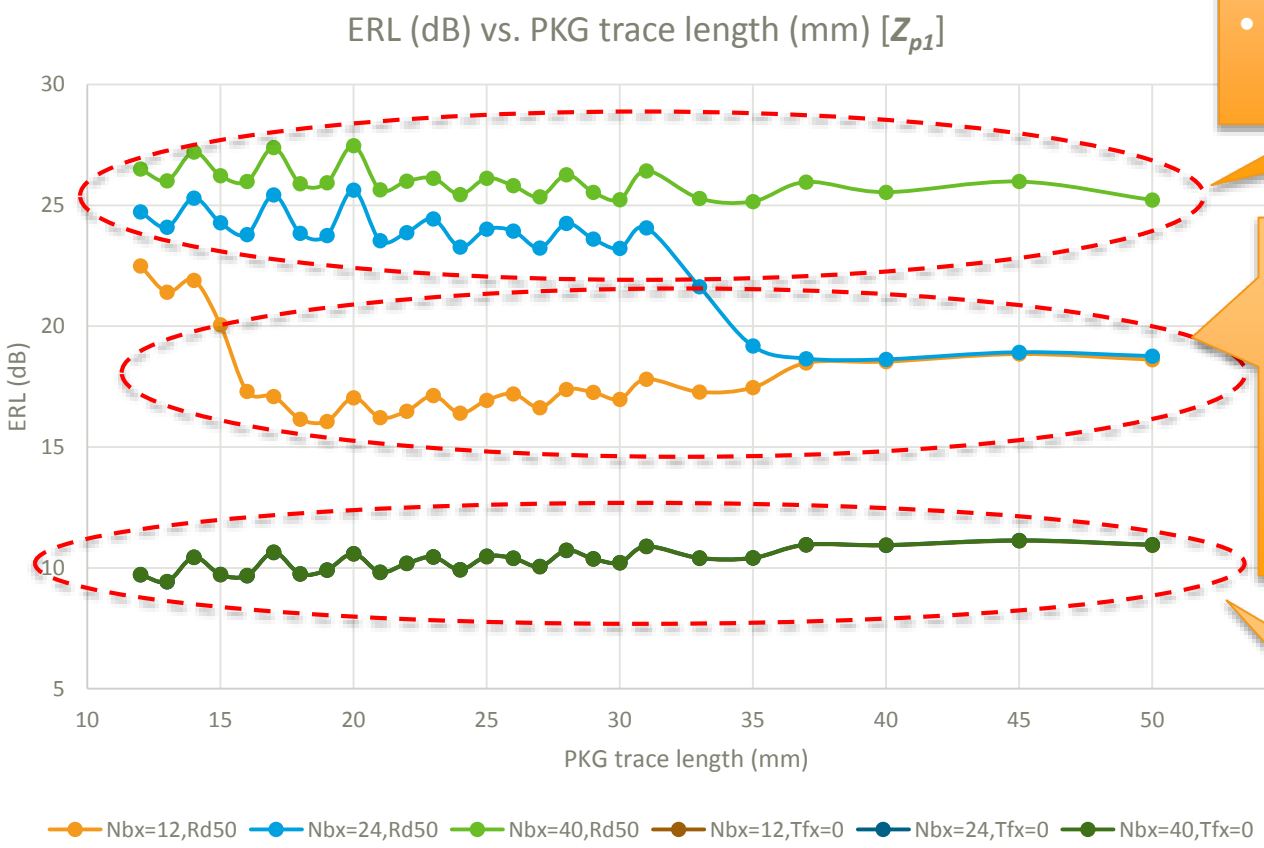
Backgrounds and Motivations

- Effective Return Loss (ERL) had been adopted in IEEE 802.3cd for 50G-KR of TX and RX test specs
  - $\mathbf{ERL_{min}}$ = 15 dB
  - T_{fx} is twice the delay from TP0 to TP0a
  - $N_{bx} = N_b$
- Q: how can we set N_{bx} with floating-tap DFE
  - 12 fixed-tap with 3 banks of 3-tap per bank to span up to 40 UI
    - There is max limit on floating-tap coefficients, while ERL doesn't
  - Exploring 3 options: 12, 24, 40
- We explored KR ERL spec by
  - COM ERL calculation by measured TP0 to TP0a test fixture
  - ERL sensitivity to DUT related impedances
- Observations
  - Appropriate $\mathbf{ERL_{min}}$ spec depends on N_{bx} we set
- Suggestions
  - Requires correlation to set N_{bx} and $\mathbf{ERL_{min}}$

Channel and COM Settings

- DUT
  - COM KR on-die & PKG model
- Measured TP0a test fixture
  - 1.7 dB IL at Nyquist
  - T_{fx} = 1.56 ns
- COM parameter settings [details in appendix]
  - COM 2.75 with parameters in D0p3
- Experiments
  - Sweep N_{bx} = [12 24 40]
  - Sweeping R_d, Z_{p1}, Z_{c1}, Z_{c2}
  - Observing ERL22 sensitivity by different TX PKG trace length (mm)
    - From 12 up to 50

KR ERL Analysis with TP0a test fixture

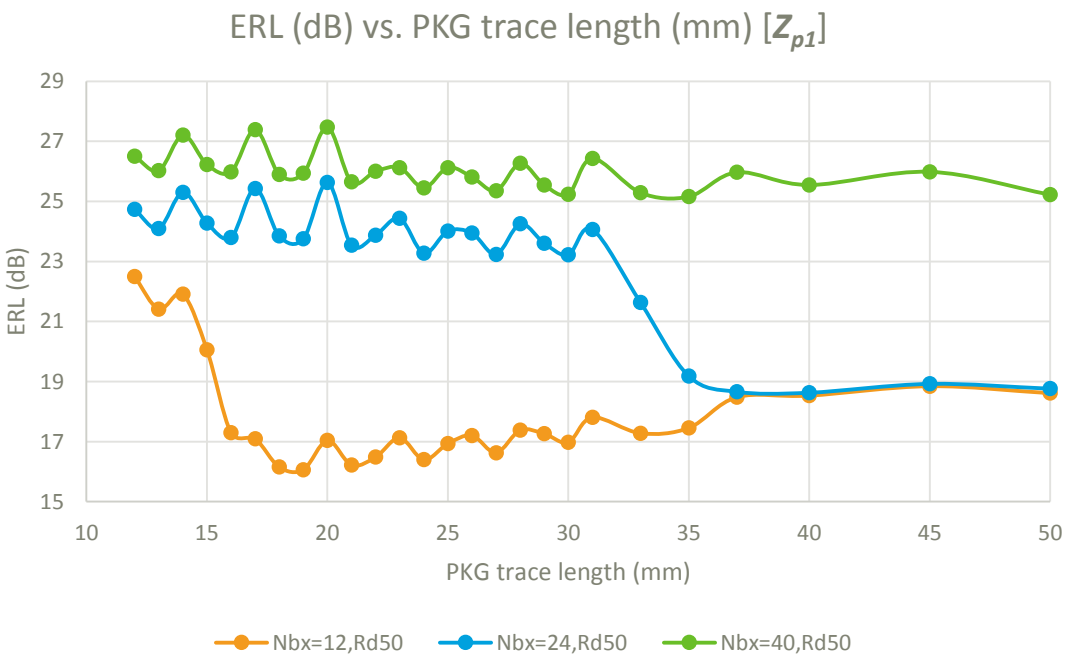


N_{bx}=40 or
N_{bx}=24 & Zp1 <= 31 mm
- can't reflect DUT impedance discontinuities

N_{bx}=12 & Z_{p1} >= 16 mm
- reflects impedance discontinuities
- may 'False Fail' cases with strong reflection covering by floating-tap DFE

T_{fx}=0: TP0a test fixture domains ERL!

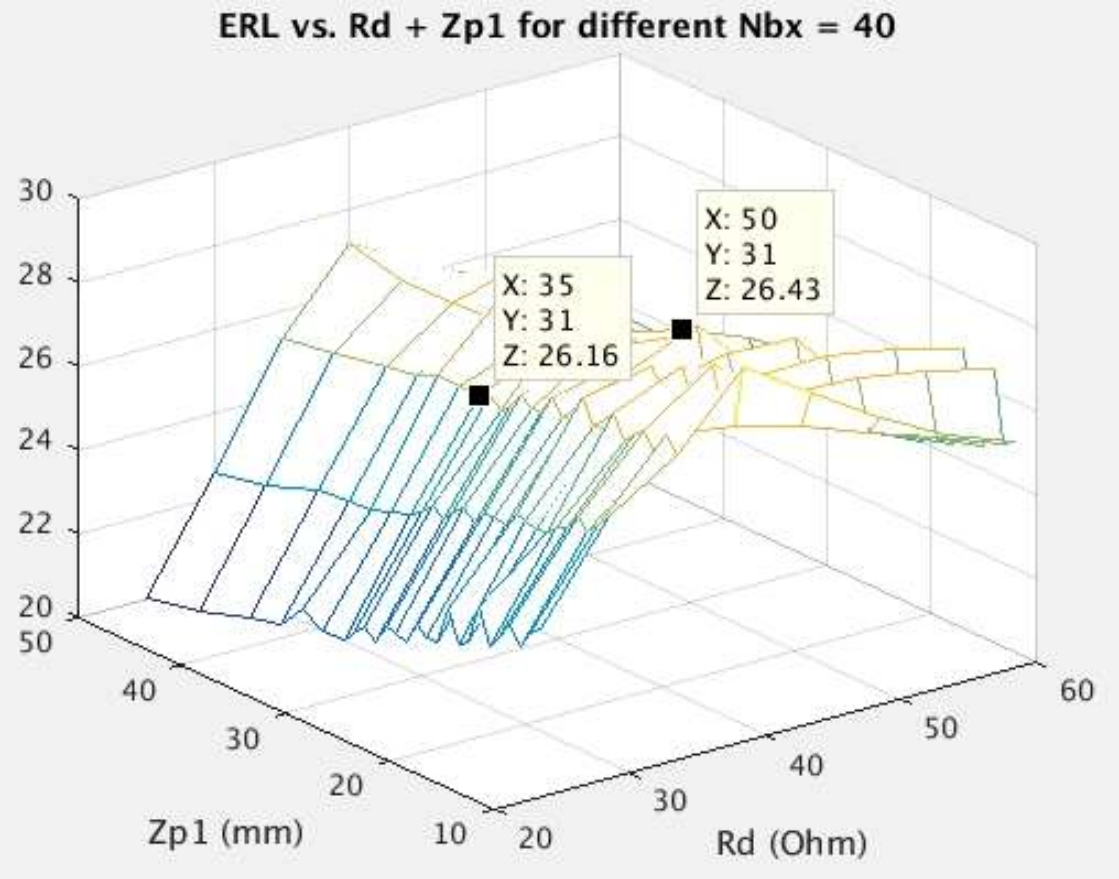
KR ERLmin Options – PKG > 31 mm



- Possible **ERL_{min}** options
  - By averaging ERL among valid PKG trace lengths = mean(ERL)
  - Set **ERL_{min}** = mean(ERL) – 3 dB
- Option 1: Zp1 = 12 ~ 31 mm
  - **ERL_{min}** = 14, 20.5, 22.5 dB for ***N_{bx}*** = 12, 24, 40
- Option 2: Zp1 = 12 ~ 50 mm
  - Cover the very large PKG scenario
  - **ERL_{min}** = 14, 15.5, 22.5 dB for ***N_{bx}*** = 12, 24, 40

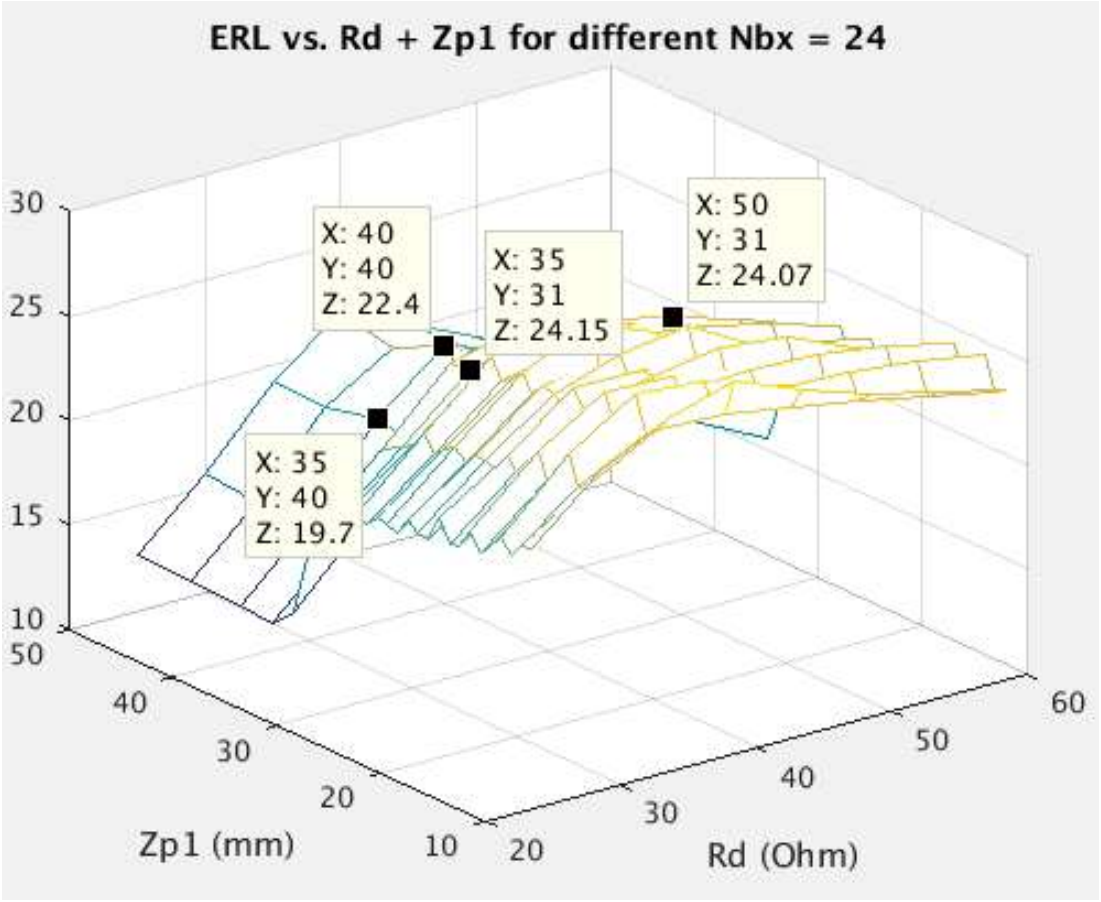
ERLmin / N_{bx}	12	24	40
Option 1	14 dB	20.5 dB	22.5 dB
Option 2	14 dB	15.5 dB	22.5 dB

ERL Sensitivity with N_{bx} = 40 – R_d



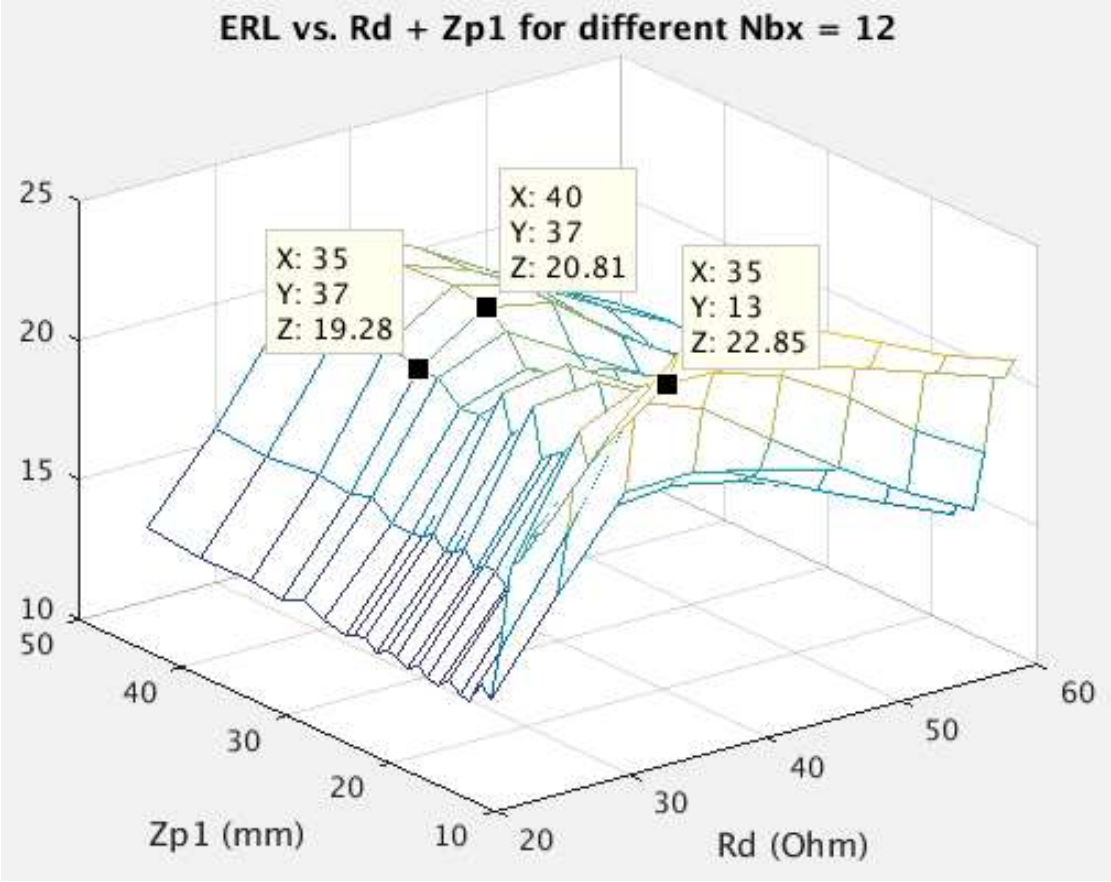
- N_{bx} = 40 & $\mathbf{ERL_{min}}$ = 22.5 dB
  - Not sensitive to Rd, even 30% variation
- Similar observations for sweeping Z_{c1} & Z_{c2}

ERL Sensitivity with N_{bx}= 24 – R_d



- ERL is sensitive to PKG length
- Option 1: **ERL_{min}** = 20.5 dB
  - For Z_{p1} <= 31 mm: not sensitive to Rd, even 30% variation
  - For Z_{p1} > 31 mm: easy to have False Fail case
- Option 2: **ERL_{min}** = 15.5 dB
  - May easily to have False Pass cases even impedance discontinuity is large
- Similar observations for sweeping Z_{c1} & Z_{c2}

ERL Sensitivity with N_{bx}= 12 – R_d



- **ERL_{min}** = 14 dB
  - For Z_{p1} <= 15 mm: doesn't reflects capability of floating-tap
  - For Z_{p1} > 15 mm: sensitive to Rd variation
- Similar observations for sweeping Z_{c1} & Z_{c2}

Summary

- There are pros & cons for the following 3 N_{bx} settings

Nbx	ERLmin (dB)	Pros	Cons
12	14 dB	• Sensitive to imp.	• Ignore 'floating-tap'
24	Opt. 1: 20.5 dB	• Consider 'floating-tap'	• Not sensitive to imp. • Not cover long PKG > 31 mm
	Opt. 2: 15.5 dB		• False pass risk
40	22.5 dB	• Consider 'floating-tap'	• Not sensitive to imp. • False pass risk • ERL sensitive to test fixture variation

- Next step
  - Correlation COM vs. TP0 ERL specs
  - Check sensitivity of ERL to impedance mismatch
  - Check ERL reflects floating-tap capability

everyday genius

COM Settings – ERL Calculation

able 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02:0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[2 1 4 3]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	2000	
beta_x	2.34E+09	
rho_x	**0.3**	
fixture delay time	1.56E-09	s
TDR_W_TXPKG	1	
N_bx	12	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A? parameterss		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92?2 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**3**	**0 1 2 or 3 groups**
N_bf	*3*	taps per group
N_f	40	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps

yellow indicates WIP