3ck Mini-Agenda

IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force

Kent Lusted, Vice-Chair
Employed by and Affiliated with Intel Corporation

November 11-13, 2019 Waikoloa Village, HI, USA

Notes

- In case of a conflict, the schedule in the main agenda deck takes precedence.
- This contribution was prepared for convenience.
- Schedule subject to change.

Presentations – Monday

Topic	Time	Author(s)	Affiliation(s)	Title	Duration
	1:00:00 PM	Kent Lusted	Intel	Agenda	0:45
	1:45:00 PM	Matt Brown	Huawei	Editors report	0:15:00
FEC	2:00:00 PM	Mark Gustlin	Cisco	Performance Improvements due to FEC Interleaving on a 100G Link	0:30:00
FEC	2:30:00 PM	Mark Gustlin	Cisco	100GBASE-KR1/CR1 FEC Thoughts	0:20:00
FEC	2:50:00 PM	Mark Gustlin	Cisco	**LATE** Performance Improvements due to FEC Interleaving	0:20:00
	3:10:00 PM	Break			0:20:00
	3:30:00 PM	Discussions & Straw Polls			0:30:00
CR	4:00:00 PM	Rich Mellitz	Samtec	Synthesized 2 m QSFP CR Channels: End to End IL 28.5 dB and Cable Assembly and IL	0:20:00
CR	4:20:00 PM	Jane Lim	Cisco	100G CR End-to-End Channel Analysis Update (III)	0:15:00
CR	4:35:00 PM	Tom Palkert	Molex	QSFP-DD TP1-TP4 Channel Simulations	0:15:00
CR	4:50:00 PM	Ali Ghiasi	Ghiasi Quantum/I	Choosing an optimum CR Equalizer	0:25:00
CR	5:15:00 PM	Rich Mellitz	Samtec	CR ERLmin Proposal	0:15:00
CR	5:30:00 PM	Sam Kocsis	Amphenol	**LATE** 100G CR Analysis Cu Cable Channels, OSFP	0:15:00
	5:45:00 PM	Break for the Day			0:0

Note –Times listed are subject to change.

Presentations – Tuesday

Topic	Time	Author(s)	Affiliation(s)	Title	Duration	
	8:00:00 AM	Kent Lusted	Intel	Opening remarks	0:05	
CR	8:05:00 AM	Chris Diminico	MC Communicatic	**LATE** Baseline Proposal Cable assembly, Host, MTF, and Channel Insertion Loss	0:30:00	
	8:35:00 AM	Discussions and straw polls			0:45:00	
C2M	9:20:00 AM	Phil Sun	Credo	Baseline Proposal for 100GAUI-1/200GAUI-2/400GAUI-4 C2M Reference Receiver	0:20:00	20
C2M	9:40:00 AM	Ali Ghiasi	Ghiasi Quantum/I	Completing C2M Baseline Proposal TBDs	0:30:00	30
	10:10:00 AM	Break			0:20:00	
C2M	10:30:00 AM	Mike Li	Intel	Comparison of CTLE+DFE vs TDECQ/FFE Reference Receivers for 802.3ck TP1a/TP4 Cc	0:15:00	15
C2M	10:45:00 AM	Phil Sun	Credo	C2M simulation with proposed reference receivers	0:30:00	30
C2M	11:15:00 AM	Tom Palkert	MACOM	RX Reference Receiver Power requirements	0:20:00	20
C2M	11:35:00 AM	Tom Palkert	MACOM	RX Reference Receiver	0:20:00	20
	11:55:00 AM	Lunch			1:00:00	
C2M	12:55:00 PM	Ali Ghiasi	Ghiasi Quantum/I	C2M Link Analysis at Host and Module Output	0:25:00	25
C2M	1:20:00 PM	Mike Dudek	Marvell	Comparison of C2M performance at TP1a with whole channel performance	0:25:00	25
C2M	1:45:00 PM	Mau-Lin Wu	MediaTek	C2M TP1a VEC and ERL Test Specs	0:30:00	30
C2M	2:15:00 PM	Mike Li	Intel	802.3ck Chip-to-Module TP1a/TP4 Compliance Test Measurement Methodology	0:25:00	25
C2M	2:40:00 PM	Rich Mellitz	Samtec	C2M ERLmin Proposal	0:20:00	20
	3:00:00 PM	Break			0:30:00	
C2M	3:30:00 PM	Nathan Tracy	TE	**LATE** New chip to module channel simulation and analysis	0:15:00	15
C2M	3:45:00 PM	Mark Kimber	Semtech	**LATE** Further analysis of synthesized 100G C2M short channels	0:20:00	20
	4:05:00 PM	Discussions and straw polls			1:45:00	
	5:50:00 PM	Break for the Day				

Note –Times listed are subject to change.

Presentations - Wednesday

Topic	Time	Author(s)	Affiliation(s)	Title	Duration
	8:00:00 AM	Kent Lusted	Intel	Agenda	0:05
KR	8:05:00 AM	Athos Kasapi	Cadence	A tap weight refinement to the KR (receive) Reference Equalizer Model	0:30:00
KR	8:35:00 AM	Rich Mellitz	Samtec	KR ERLmin Proposal	0:25:00
KR	9:00:00 AM	Mau-Lin Wu	MediaTek	Study of KR ERL test specs	0:20:00
KR	9:20:00 AM	Tom Palkert	Molex	**LATE** BP OD channel analysis	0:20:00
	9:40:00 AM	Discussions and Straw Polls			0:45:00
	10:25:00 AM	Break			0:20:00
	10:45:00 AM	Motions and closing business			1:15:00
	12:00:00 PM	Meeting Adjorn			

Note –Times listed are subject to change.