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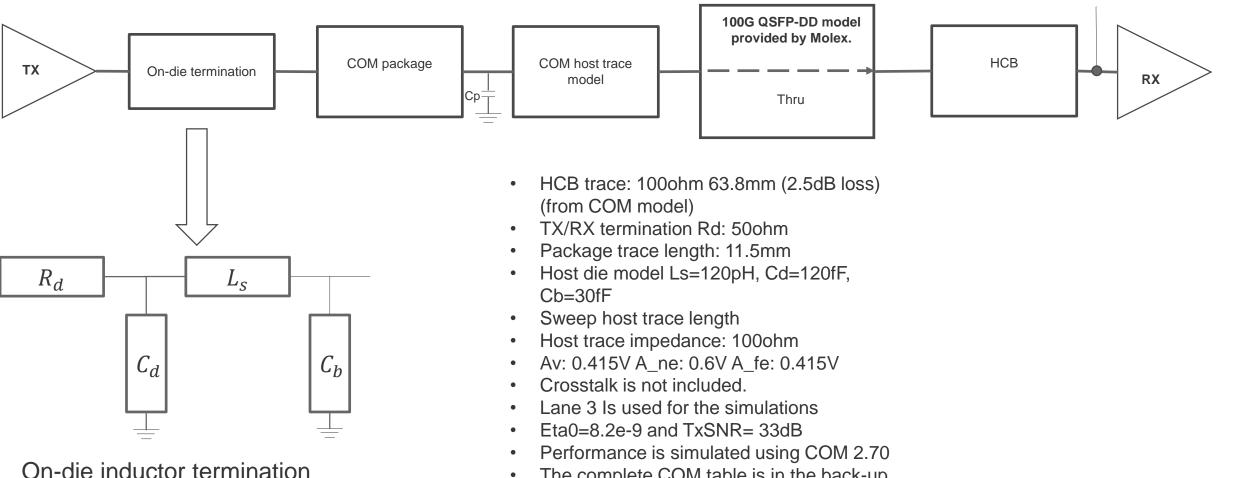
Comparison of C2M performance at TP1a with whole channel performance.

Mike Dudek Tao Hu 11/11/2019 Presented at November 2019 Plenary.

Introduction

- Dudek_3ck_01_0719 explored the effect of host trace length on C2M TP1a performance with different die models, package lengths and some host impairments. It showed significant degradations and resonances at shorter host trace lengths and that the system needs to be designed to cope with the bad resonances.
- Dudek_3ck_01_0919 presented simulations of the whole channel performance, showed that a significantly stronger equalizer than the 5 tap FFE equalizer is required for adequate whole channel performance and provided some initial correlation between the VEC performance at TP1a and the whole channel performance.
- This presentation explores the correlation between VEC (and EVEC) at TP1a measured with the 4 tap DFE and 5 tap FFE reference equalizers used by the proposed baselines and whole channel performance where the module receiver has either 4 tap, 7 tap or 12 tap DFE or 5 tap or 10 tap FFE.

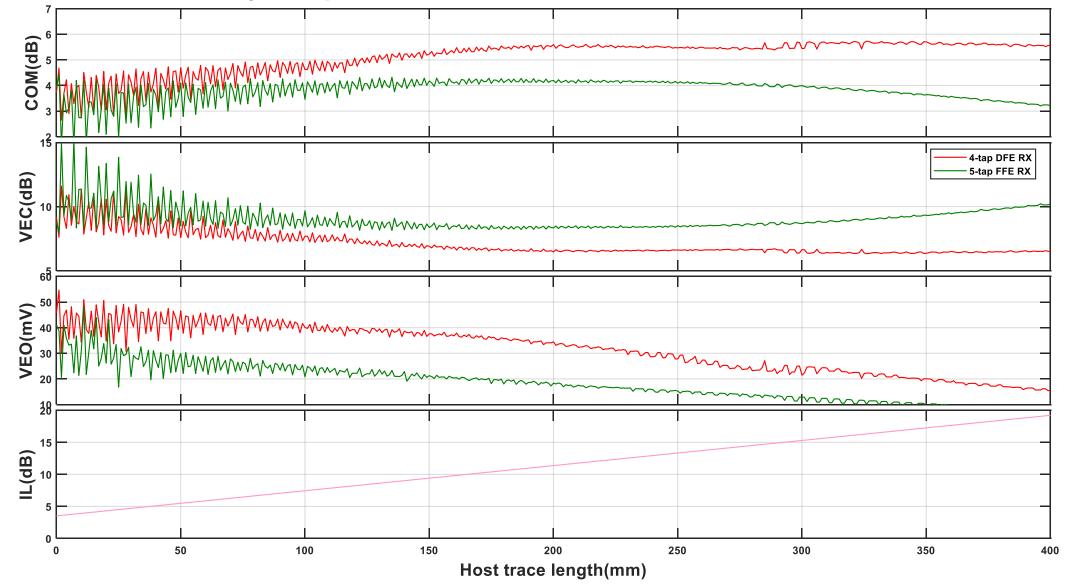
Chip to module block diagram for TP1a performance TP1a



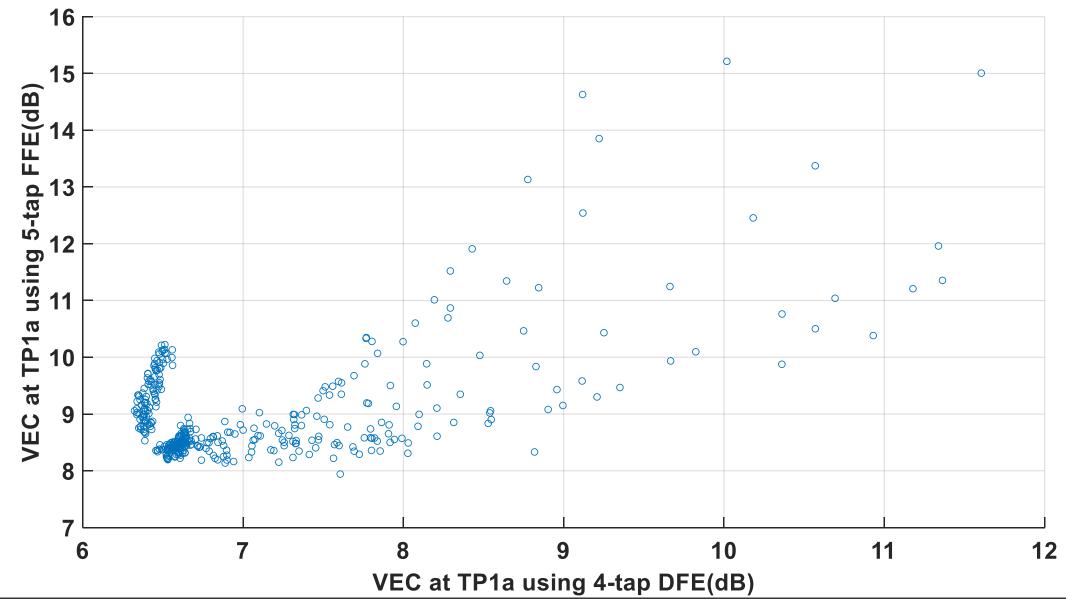
The complete COM table is in the back-up

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TP1a results by equalization

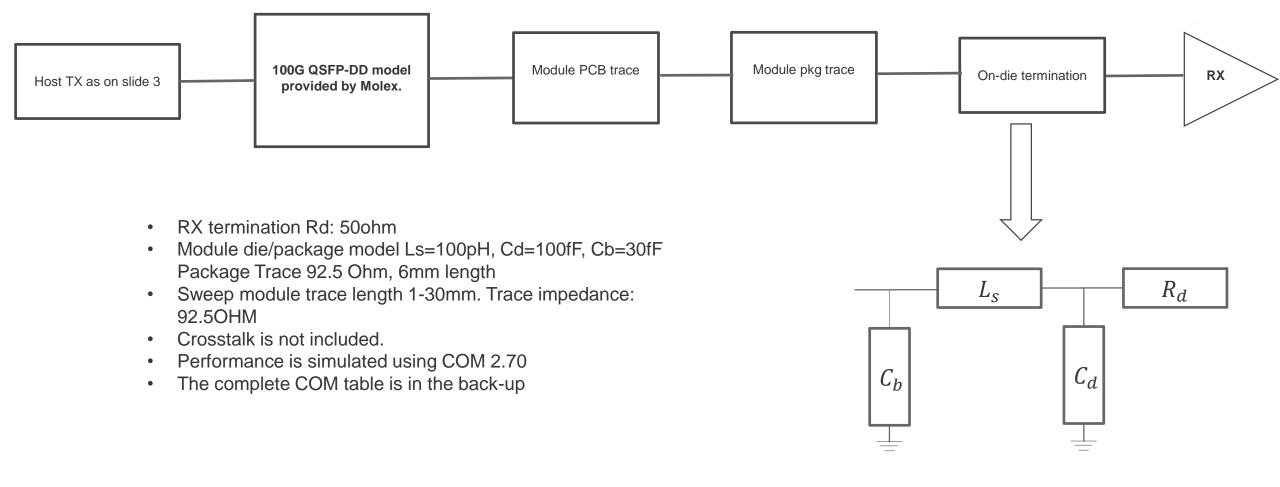


VEC at TP1a 5tap FFE vs. VEC at TP1a 4tap DFE



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Chip to module block diagram for end to end performance

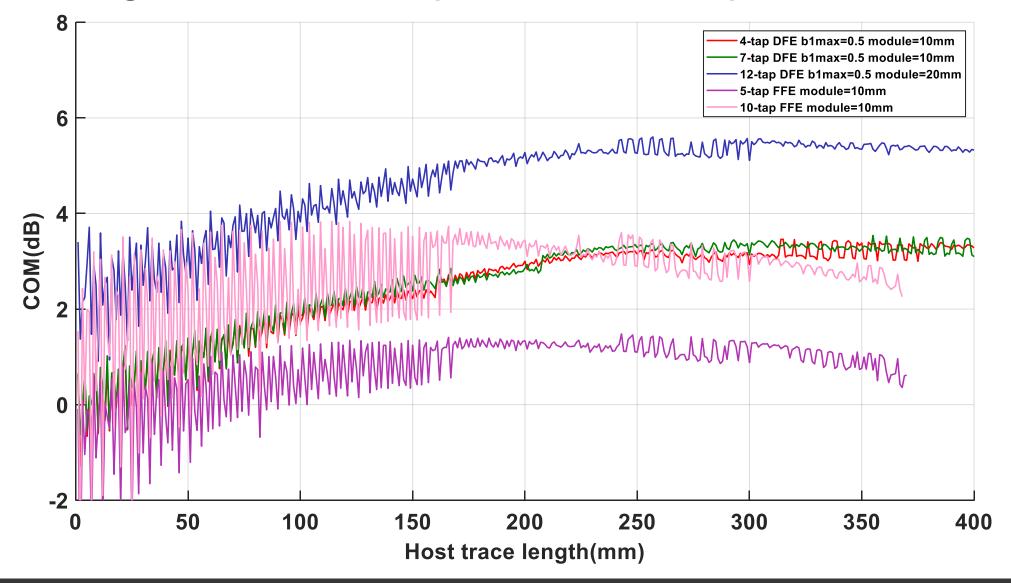


On-die inductor termination

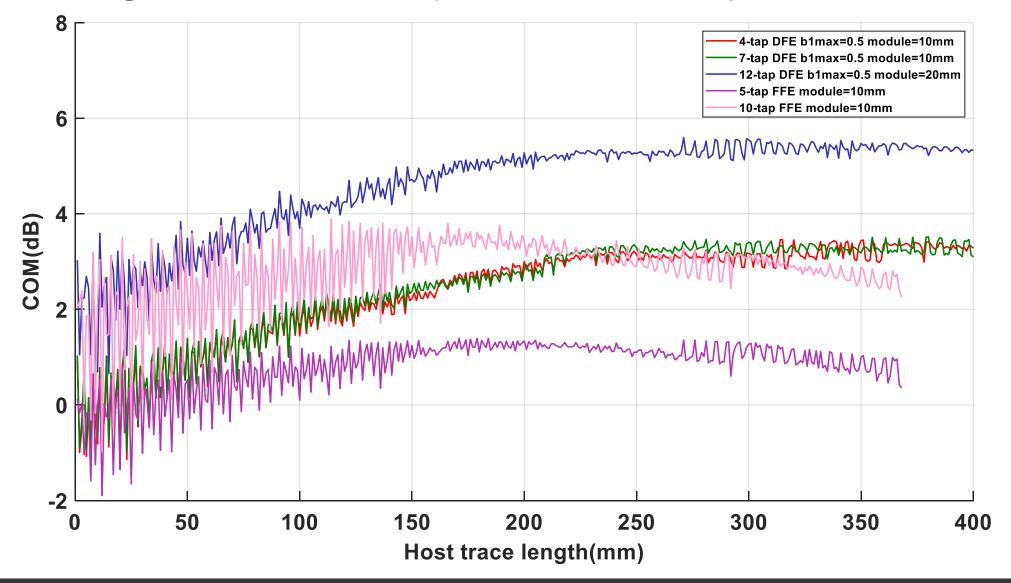
Details of module model.

- The following equalizers were used
 - 4 tap DFE
 - 7 tap DFE
 - 12 tap DFE
 - 5 tap FFE
 - 10 tap FFE
 - In all cases the Tx FIR was optimized for the VEC at TP1a using the chosen reference equalizer and then the tap weights were frozen for measuring the end to end performance with the various module receivers.

End to end COM examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a



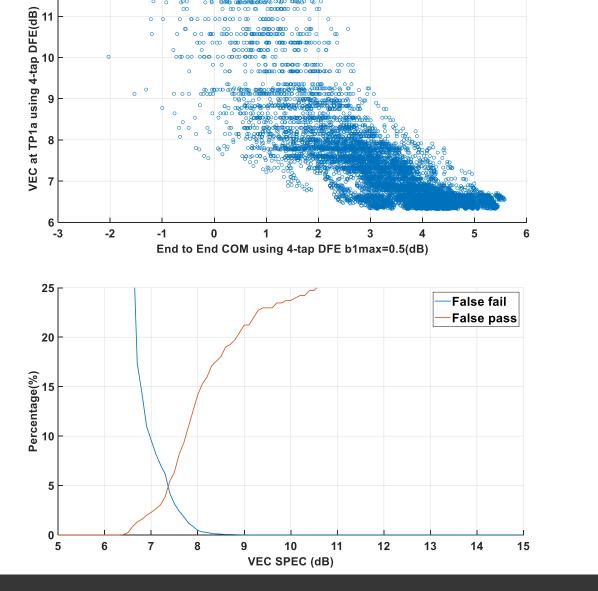
End to end COM examples with approximate worst case module length and TX FIR optimized for 5 tap FFE at TP1a



Conclusions from these results.

- With these module package and die models a stronger equalizer is needed in the module to provide adequate performance for the critical 50mm to 160mm host trace lengths where the host could also be used for the CR specification.
- Note that there are other impairments that have not been explored in this presentation. In particular the effect of vias in the host and module.

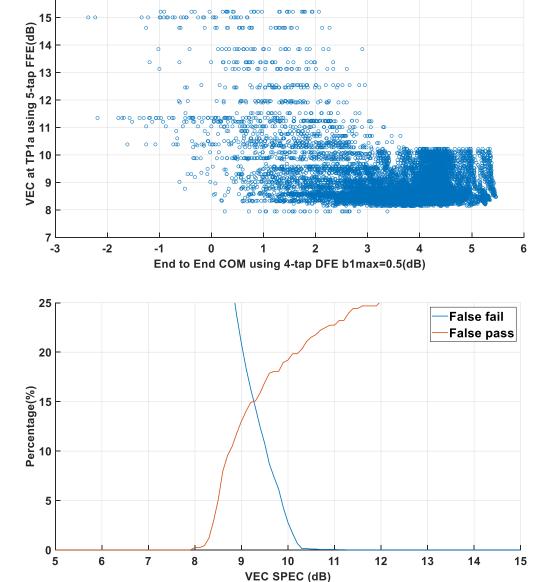
Module receiver: 4-tap DFE



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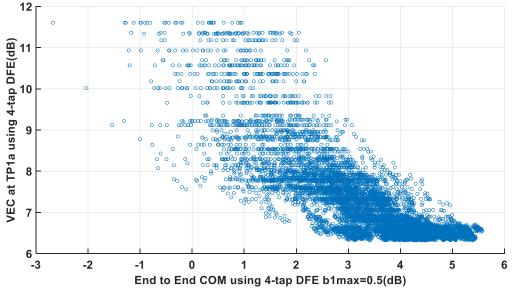
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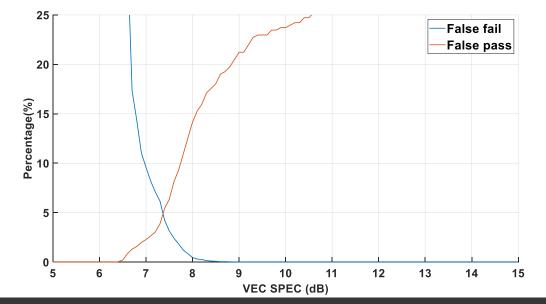
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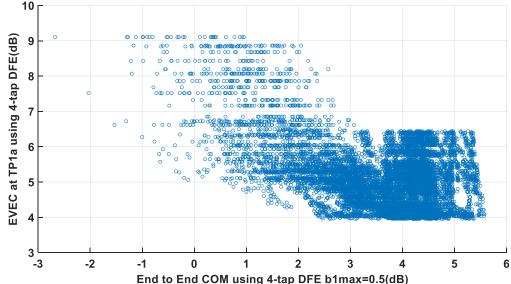


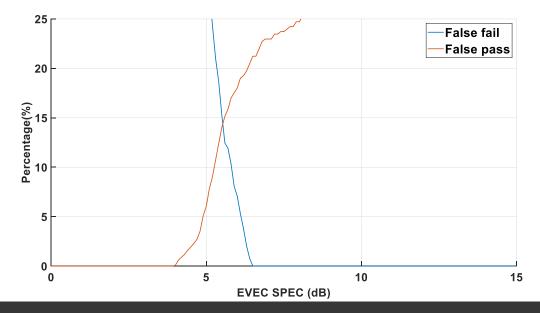


VEC/EVEC at TP1a (DFE4) vs. End to End COM (DFE4)









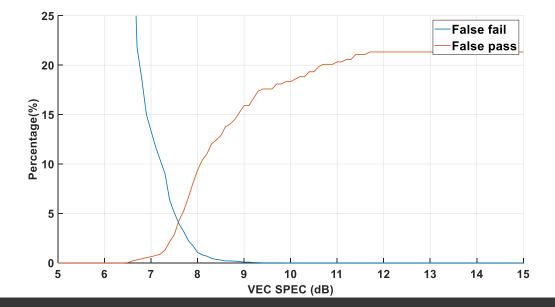
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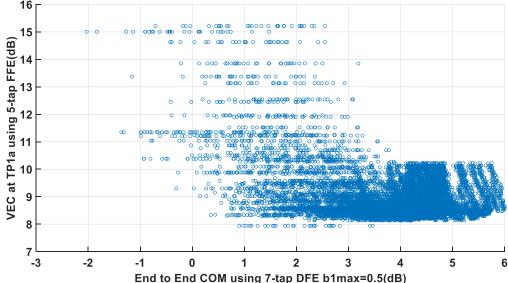
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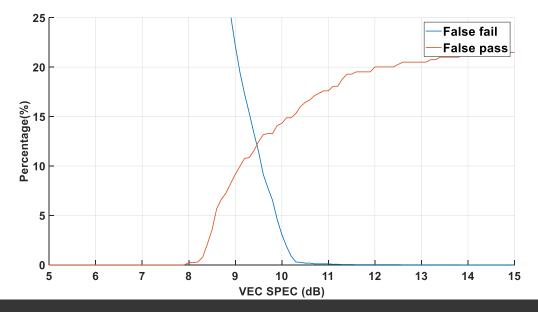
Module receiver: 7-tap DFE





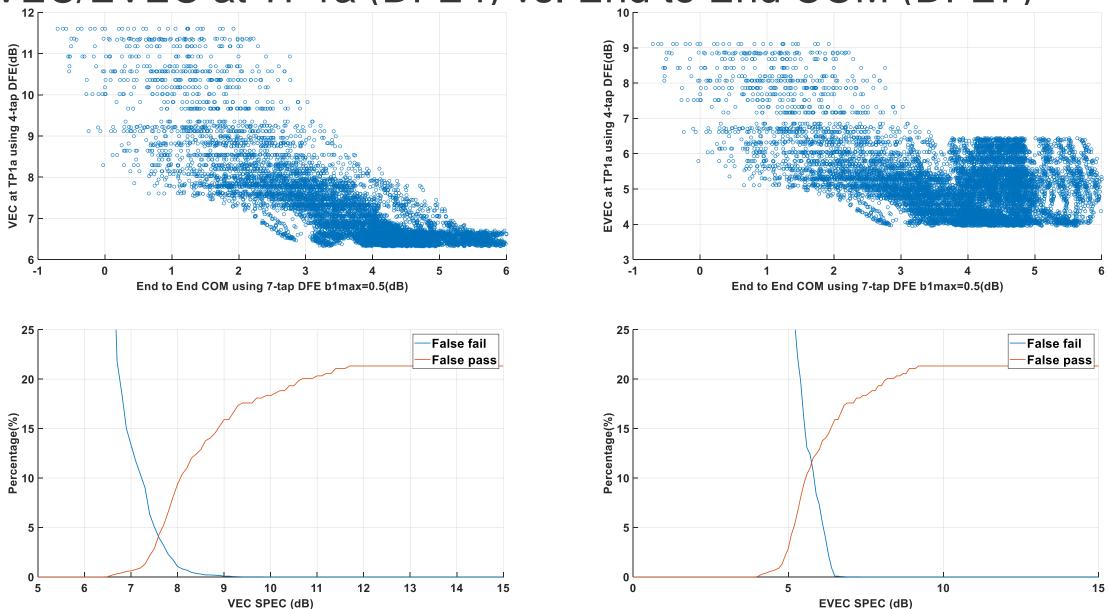






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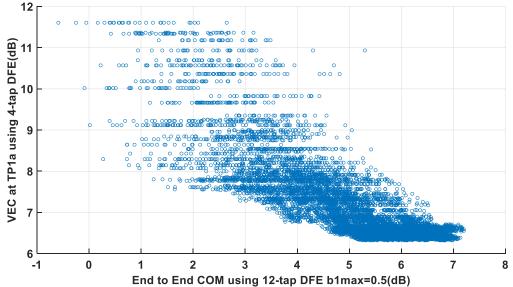
VEC/EVEC at TP1a (DFE4) vs. End to End COM (DFE7)

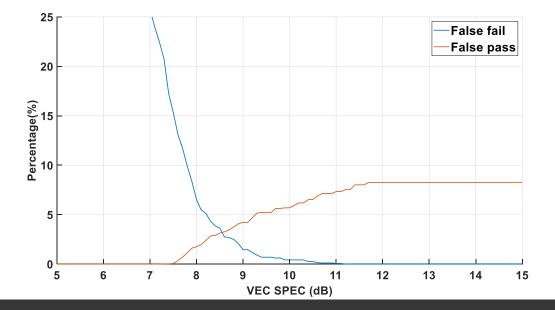
M A R V E L L[®]

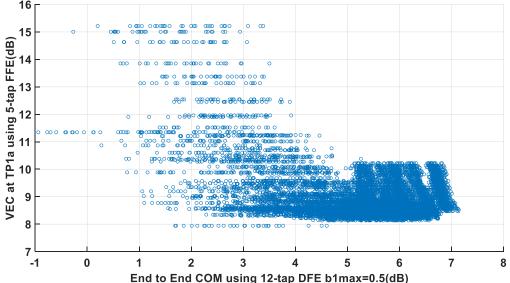
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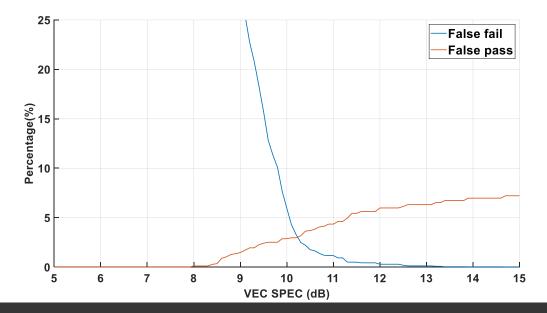
Module receiver: 12-tap DFE



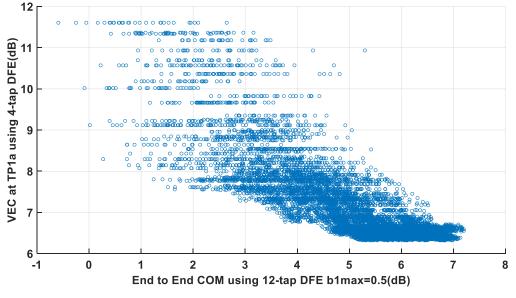


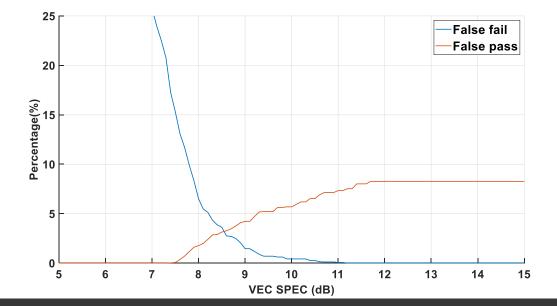


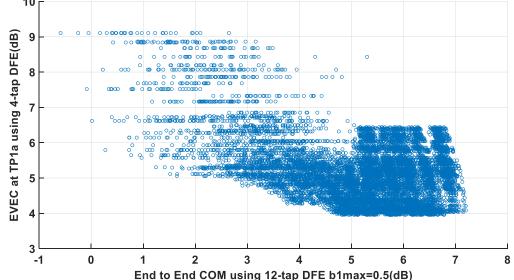


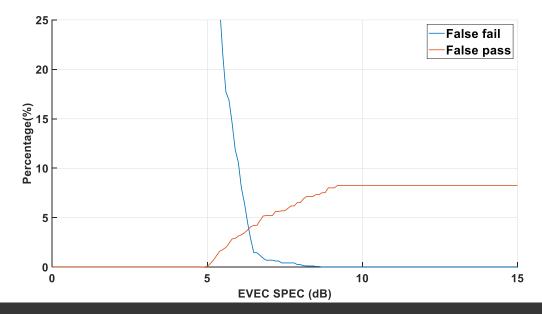


VEC/EVEC at TP1a(DFE4) vs. End to End COM (DFE12)





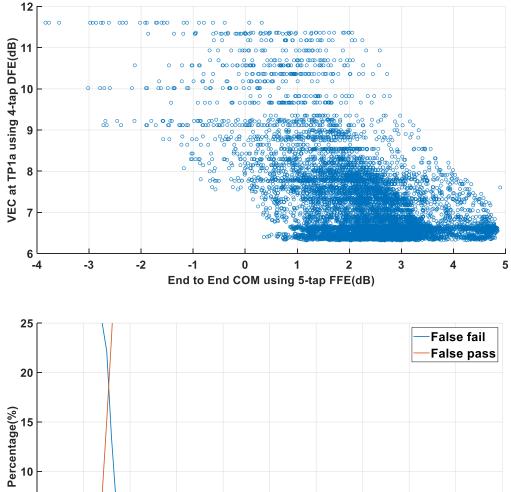


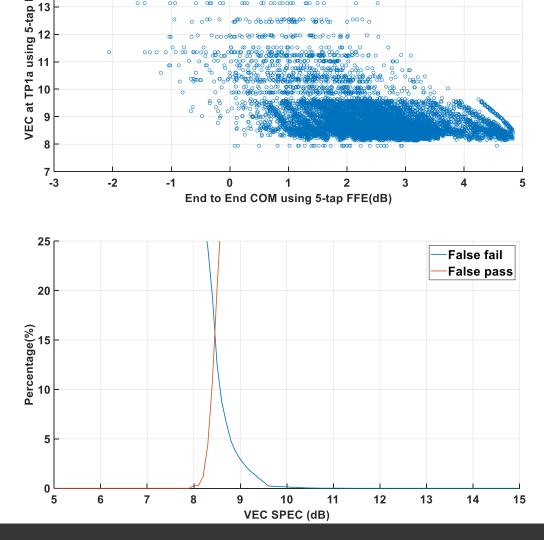


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Module receiver: 5-tap FFE

VEC at TP1a(DFE4/FFE5) vs. End to End COM (FFE5)





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VEC SPEC (dB)

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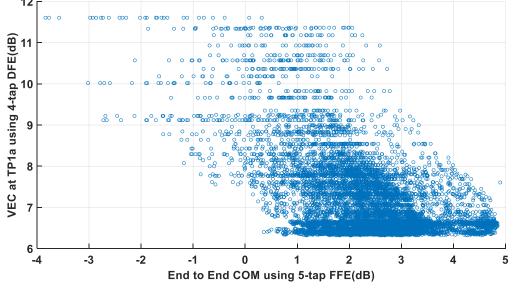
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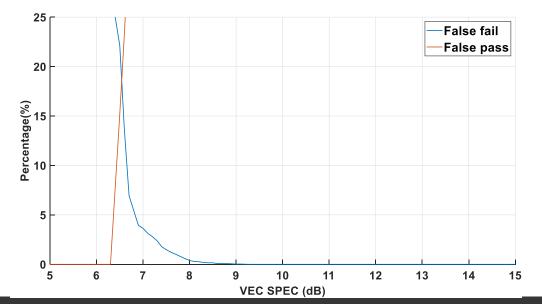
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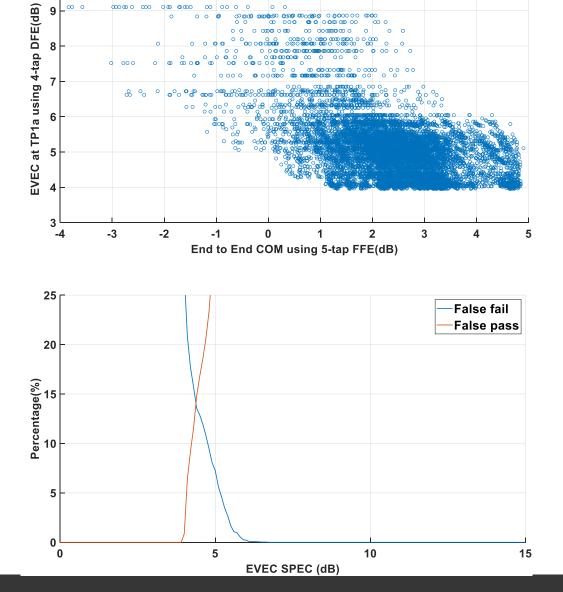
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VEC/EVEC at TP1a(DFE4) vs. End to End COM (FFE5)







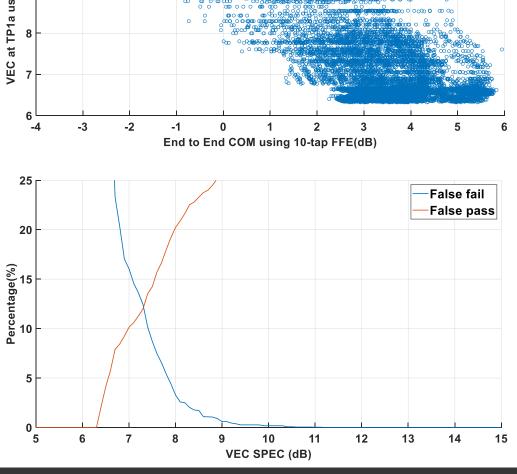
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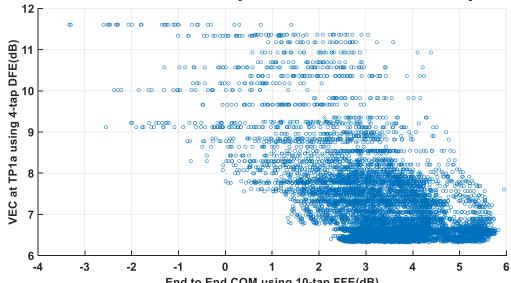
Module receiver: 10-tap FFE

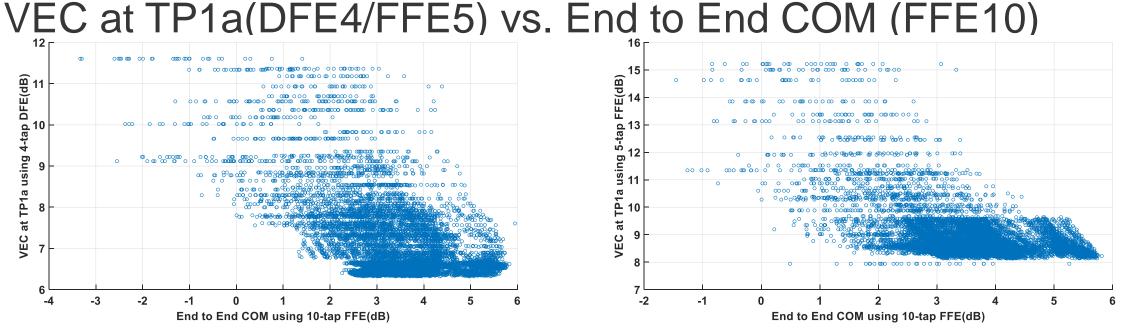
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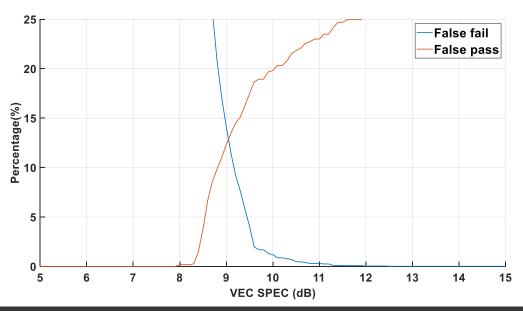
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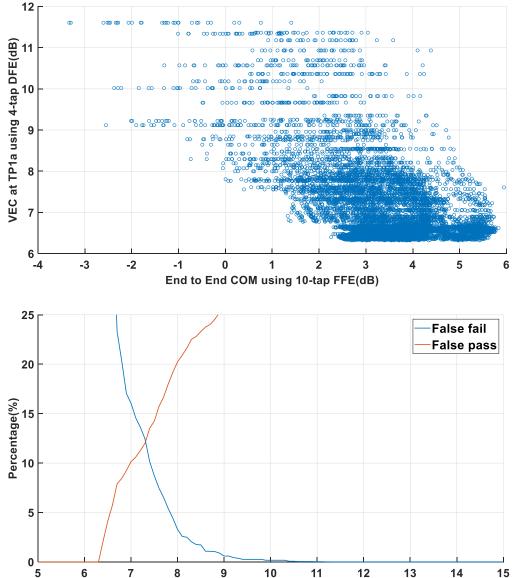




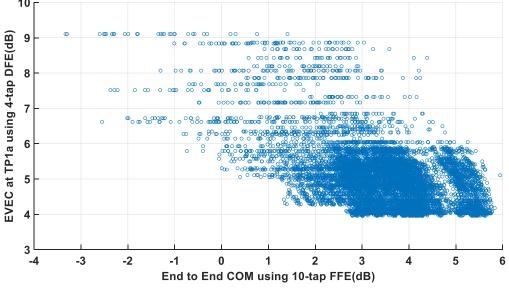


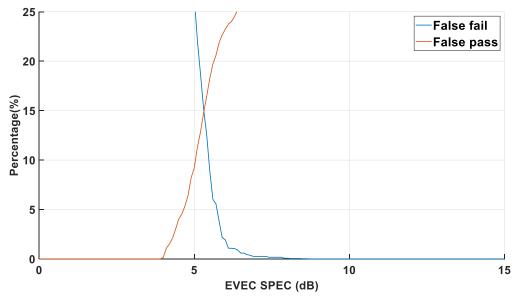


VEC/EVEC at TP1a(DFE4) vs. End to End COM (FFE10)



VEC SPEC (dB)





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Conclusions.

- The correlation between performance at TP1a and whole link performance is better with the 4 tap DFE reference receivers with the DFE module receivers and very similar to the correlation of the 5 tap FFE reference receiver for the whole link performance with the FFE module receivers.
- Using EVEC instead of VEC with the 4 tap DFE makes the correlation worse.
- The 4 tap DFE should be chosen as the reference equalizer and VEC as the chief performance metric. (with an eye amplitude specification just to ensure that very high loss channels don't pass).
- The specification value in the proposed baselines of 8.5dB EVEC in sun_3ck_adhoc_01_103019 would result in many false passes even if a very strong module equalizer is used.
- The recommended specification value is 7.5dB VEC with the 4 tap DFE but this will require a strong module equalizer.

Back-up

TP1a COM spreadsheet w/ 4-tap DFE RX

Table 93A-1 parameters				I/O control		Table 93A–3 parameters			
Parameter	Setting	Units	Information	DIAGNOSTICS	0	logical	Parameter	Setting	Units
f_b	53.125	GBd		DISPLAY_WINDOW	0	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f min	0.05	GHz		CSV_REPORT	1	logical	package_tl_tau	6.1400E-03	ns/mm
 Delta_f	0.01	GHz		RESULT DIR	\results\100GEL_WG_{da		package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
 C_d	[1.2e-40]	nF	[TX RX]	SAVE_FIGURES	0	logical			
L_s	[0.12, 0]	nH	[TX RX]	Port Order	[1324]			Table 92–12 parameters	
Сь	[0.3e-4 0]	nF	[TX RX]	RUNTAG	C2M_1218		Parameter	Setting	
z_p select	[1]		[test cases to run]	COM_CONTRIBUTION	0	logical	board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[11.5 11.5; 1.8 1.8]	mm	[test cases]		Operational		board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[00; 00]	mm	[test cases]	COM Pass threshold	3	dB	board_Z_c	[100 100]	Ohm
z_p (FEXT)	[11.5 11.5; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10.5	dB	z_bp (TX)	1:400	mm
z_p (RX)	[00; 00]	mm	[test cases]	DER_0	1.00E-05		z_bp (NEXT)	0	mm
C_p	[0.87e-40]	nF	[TX RX]	T_r	6.16E-03	ns	z_bp (FEXT)	0	mm
R_0	50	Ohm		FORCE_TR	1	logical	z_bp (RX)	63.8	mm
R_d	[50 50]	Ohm	[TX RX]						
A_v	0.415	V		TDR	and ERL options				
A_fe	0.415	V		TDR	0	logical			
A_ne	0.6	V		ERL	0	logical			
L	4			ERL_ONLY	0	logical			
М	32			TR_TDR	0.01	ns			
	filter and Eq			N	300				
f_r	0.75	*fb		TDR_Butterworth	1	logical			
c(0)	0.6		min	beta_x	1.70E+09				
c(-1)	[-0.3:0.02:0]		[min:step:max]	rho_x	0.3				
c(-2)	[0:.02:0.1]		[min:step:max]	fixture delay time	0				
c(1)	[-0.1:0.05:0]		[min:step:max]		ceiver testing				
N_b	4	UI		RX_CALIBRATION	0	logical			
b_max(1)	0.5			Sigma BBN step	5.00E-03	V			
b_max(2N_b)	0.2								
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter				
f_z	12.58	GHz		sigma_RJ	0.01	UI			
f_p1	20	GHz		A_DD	0.02	UI			
f_p2	28	GHz		eta_0	8.20E-09	V^2/GHz			
g_DC_HP	[-3:1:0]		[min:step:max]	SNR_TX	33	dB			
f_HP_PZ	1.328125	GHz		R_LM	0.95				
ffe_pre_tap_len	0	UI							
ffe_post_tap_len	0	UI		TDR_W_TXPKG	1				
Include PCB	1	logical							
ffe_tap_step_size	0								
ffe_main_cursor_min	0.7								
ffe_pre_tap1_max	0.3								
ffe_post_tap1_max	0.3								
ffe_tapn_max	0.125								
ffe_backoff	0								

TP1a COM spreadsheet w/ 5-tap FFE RX

Table 93A-1 parameters			I/O control			Table 93A–3 parameters			
Parameter	Setting	Units	Information	DIAGNOSTICS	0	logical	Parameter	Setting	Units
f_b	53.125	GBd		DISPLAY WINDOW	0	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
 f_min	0.05	GHz		CSV_REPORT	1	logical	package_tl_tau	6.1400E-03	ns/mm
 Delta_f	0.01	GHz		RESULT DIR	\results\100GEL_WG_{d		package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-40]	nF	[TX RX]	SAVE_FIGURES	0	logical			
L_s	[0.12, 0]	nH	[TX RX]	Port Order	[1324]			Table 92–12 parameters	
Сь	[0.3e-40]	nF	[TX RX]	RUNTAG	C2M 1218		Parameter	Setting	
z_p select	[1]		[test cases to run]	COM_CONTRIBUTION	0	logical	board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[11.5 11.5; 1.8 1.8]	mm	[test cases]		Operational		board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[00; 00]	mm	[test cases]	COM Pass threshold	3	dB	board_Z_c	[100 100]	Ohm
z_p (FEXT)	[11.5 11.5; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10.5	dB	z_bp (TX)	1:400	mm
z_p (RX)	[00; 00]	mm	[test cases]	DER_0	1.00E-05		z_bp (NEXT)	0	mm
C_p	[0.87e-40]	nF	[TX RX]	T_r	6.16E-03	ns	z_bp (FEXT)	0	mm
R_0	50	Ohm		FORCE_TR	1	logical	z_bp (RX)	63.8	mm
R_d	[50 50]	Ohm	[TX RX]			_			
A_v	0.415	V		TDR	and ERL options				
A_fe	0.415	V		TDR	0	logical			
A_ne	0.6	V		ERL	0	logical			
L	4			ERL_ONLY	0	logical			
м	32			TR_TDR	0.01	ns			
	filter and Eq			N	300				
fjr	0.75	*fb		TDR_Butterworth	1	logical			
c(0)	0.6		min	beta_x	1.70E+09				
c(-1)	[-0.3:0.02:0]		[min:step:max]	rho_x	0.3				
c(-2)	[0:.02:0.1]		[min:step:max]	fixture delay time	0				
c(1)	[-0.1:0.05:0]		[min:step:max]	Re	ceiver testing				
N_b	0	UI		RX_CALIBRATION	0	logical			
b_max(1)	0			Sigma BBN step	5.00E-03	V			
b_max(2N_b)	0								
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter				
f_z	18.88	GHz		sigma_RJ	0.01	UI			
f_p1	28	GHz		A_DD	0.02	UI			
f_p2	53.125	GHz		eta_0	8.20E-09	V^2/GHz			
g_DC_HP	[-3:1:0]		[min:step:max]	SNR_TX	33	dB			
f_HP_PZ	0.00025	GHz		R_LM	0.95				
ffe_pre_tap_len	0	UI							
ffe_post_tap_len	4	UI		TDR_W_TXPKG	1				
Include PCB	1	logical							
ffe_tap_step_size	0	-							
ffe_main_cursor_min	0.7								
ffe_pre_tap1_max	0.3								
ffe_post_tap1_max	0.3								
ffe_tapn_max	0.125								
ffe_backoff	0								
	-								

End to end COM spreadsheet w/ n-tap DFE RX

L_s C_b Z_p select Z_p (TX) [11 Z_p (NEXT) Z_p (FEXT) [11 Z_p (RX)		Bd Hz Hz [TX RX] H [TX RX] IF [TX RX] IF [TX RX] If [test cases to run] [test cases] Im [TX RX] IM [TX RX]	COM Pass threshold ERL Pass threshold DER_O T_r FORCE_TR	0 0 1 \results\100GEL_WG_{dat 0 [1 3 2 4] C2M_1218 0 Operational 3 10.5 1.00E-05 6.16E-03 1 and ERL options	logical logical logical te}\ logical logical dB dB dB ns logical	Parameter package_tl_gamma0_a1_a2 package_tl_tau package_Z_c Parameter board_tl_gamma0_a1_a2 board_tl_tau board_tl_tau board_tc_c z_bp (TX) z_bp (FEXT) z_bp (RX)	Setting [0 0.0009909 0.0002772] 6.1400E-03 [87.5 92.5 ; 92.5 92.5] Table 92-12 parameters Setting [0 3.8206e-04 9.5909e-05] 5.790E-03 [100 92.5] 1:400 0 0 1:30	Units ns/mm Ohm ns/mm Ohm mm mm mm mm
f_min Delta_f C_d L_s C_b z_p select z_p (TX) [11] z_p (RXT) z_p (FEXT) C_p R_0 R_d A_fe A_ne	0.05 GH 0.01 GH [1.2e-4 1.0e-4] ni [0.12, 0.1] nH [0.3e-4 0.3e-4] ni [1] 11.5 [1.5 11.5; 1.8 1.8] mi [00; 00] mi [15 11.5; 1.8 1.8] mi [6 6; 00] mi [0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	Hz Hz Hz Hz F [TX RX] H [TX RX] [Est cases to run] m [test cases] F [TX RX] m [TX RX] V V	CSV_REPORT RESULT_DIR SAVE_FIGURES Port Order RUNTAG COM_CONTRIBUTION COM Pass threshold ERL Pass threshold DER_0 T_r FORCE_TR	1 \results\100GEL_WG_{dat 0 [1 3 2 4] C2M_1218 0 Operational 3 10.5 1.00E-05 6.16E-03 1	logical logical logical logical dB dB dB ns	package_tl_tau package_Z_c Parameter board_tl_gamma0_a1_a2 board_tl_tau board_Z_c z_bp (TX) z_bp (NEXT) z_bp (FEXT)	6.1400E-03 [87.5 92.5 ; 92.5 92.5] Table 92–12 parameters Setting [0 3.8206e-04 9.5909e-05] 5.790E-03 [100 92.5] 1:400 0 0	Ohm ns/mm Ohm mm mm mm
Delta_f C_d L_s C_b z_p select z_p (TX) [11] z_p (RXT) z_p (FEXT) C_p C_p R_0 R_d A_fe A_ne	0.01 GH [1.2e-4 1.0e-4] ni [0.12, 0.1] nH [0.3e-4 0.3e-4] ni [1] 11.5 [1.5 11.5; 1.8 1.8] mi [00; 00] mi [15 11.5; 1.8 1.8] mi [6 6; 00] mi [0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	Hz F F TX RX H TX RX F TX RX [test cases to run] m [test cases] m [text cases] m [text cases] f [TX RX] m TX RX] V V V V	RESULT_DIR SAVE_FIGURES Port Order RUNTAG COM_CONTRIBUTION COM Pass threshold ERL Pass threshold DER_0 T_r FORCE_TR	\results\100GEL_WG_{dat 0 [1 3 2 4] C2M_1218 0 Operational 3 10.5 1.00E-05 6.16E-03 1	logical logical logical dB dB ns	package_Z_c Parameter board_tl_gamma0_a1_a2 board_tl_tau board_Z_c z_bp (TX) z_bp (NEXT) z_bp (FEXT)	[87.5 92.5 ; 92.5 92.5] Table 92–12 parameters Setting [0 3.8206e-04 9.5909e-05] 5.790E-03 [100 92.5] 1:400 0 0	Ohm ns/mm Ohm mm mm mm
C_d L_s C_b z_p select z_p (TX) z_p (RXT) z_p (FEXT) C_p C_p R_0 R_d A_fe A_ne	[1.2e-4 1.0e-4] ni [0.12, 0.1] ni [0.3e-4 0.3e-4] ni [1] 11.5 (1.5 11.5; 1.8 1.8] mi [00; 00] mi (1.5 11.5; 1.8 1.8] mi [66; 00] mi [0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	F [TX RX] H [TX RX] IF [TX RX] [test cases to run] Im [test cases] IM [TX RX] IM [TX RX]	SAVE_FIGURES Port Order RUNTAG COM_CONTRIBUTION COM Pass threshold ERL Pass threshold DER_0 T_r FORCE_TR	0 [1324] C2M_1218 0 Operational 3 10.5 1.00E-05 6.16E-03 1	logical logical dB dB ns	Parameter board_tl_gamma0_a1_a2 board_tl_tau board_Z_c z_bp (TX) z_bp (NEXT) z_bp (FEXT)	Table 92-12 parameters Setting [0 3.8206e-04 9.5909e-05] 5.790E-03 [100 92.5] 1:400 0 0 0	ns/mm Ohm mm mm mm
L_s C_b z_p select z_p (TX) [11] z_p (NEXT) z_p (FEXT) [11] z_p (RX) C_p R_0 R_d A_fe A_ne	[0.12, 0.1] nH [0.3e-4 0.3e-4] nl [1] nl [15 11.5; 1.8 1.8] mt [00; 00] mt [15 11.5; 1.8 1.8] mt [6 6; 00] mt [0.87e-4 0.87e-4] nl 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	H [TX RX] IF [TX RX] [test cases to run] Im [test cases] Im [TX RX] Im [TX RX] V V	Port Order RUNTAG COM_CONTRIBUTION COM Pass threshold ERL Pass threshold DER_0 T_r FORCE_TR	[1 3 2 4] C2M_1218 0 Operational 3 10.5 1.00E-05 6.16E-03 1	dB dB ns	board_tl_gamma0_a1_a2 board_tl_tau board_Z_c z_bp (TX) z_bp (NEXT) z_bp (FEXT)	Setting [0 3.8206e-04 9.5909e-05] 5.790E-03 [100 92.5] 1:400 0 0	Ohm mm mm mm
C_b z_p select z_p (TX) z_p (NEXT) z_p (FEXT) z_p (RX) C_p R_0 R_d A_fe A_ne	[0.3e-4 0.3e-4] ni [1] [1.5 [1.5 11.5; 1.81.8] [00; 00] mi [1.5 11.5; 1.81.8] [00; 00] mi [1.5 11.5; 1.81.8] [66; 00] mi [0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	F [TX RX] [test cases to run] [m im [test cases] im [TX RX] imm [TX RX] v v	RUNTAG COM_CONTRIBUTION COM Pass threshold ERL Pass threshold DER_0 T_r FORCE_TR TDR	C2M_1218 0 Operational 3 10.5 1.00E-05 6.16E-03 1	dB dB ns	board_tl_gamma0_a1_a2 board_tl_tau board_Z_c z_bp (TX) z_bp (NEXT) z_bp (FEXT)	Setting [0 3.8206e-04 9.5909e-05] 5.790E-03 [100 92.5] 1:400 0 0	Ohm mm mm mm
z_p select z_p (TX) [11 z_p (NEXT) [11 z_p (FEXT) [11 z_p (RX) [11 C_p [0 R_0 [0 R_d [11 A_fe [12	[1] 1.5 11.5; 1.8 1.8] mr [00; 00] mr 1.5 11.5; 1.8 1.8] mr [6 6; 00] mr [0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	[test cases to run] im [test cases] im [test cases] im [test cases] im [test cases] if [TX RX] im [TX RX] v	COM_CONTRIBUTION COM Pass threshold ERL Pass threshold DER_0 T_r FORCE_TR TDR	0 Operational 3 10.5 1.00E-05 6.16E-03 1	dB dB ns	board_tl_gamma0_a1_a2 board_tl_tau board_Z_c z_bp (TX) z_bp (NEXT) z_bp (FEXT)	[0 3.8206e-04 9.5909e-05] 5.790E-03 [100 92.5] 1:400 0 0	Ohm mm mm mm
z_p (TX) [11 z_p (NEXT) [11 z_p (FEXT) [11 z_p (RX) [11 C_p [0 R_0 [0 R_d [11 A_fe [11 A_ne [11	11.5 11.5; 1.81.8] mi [00; 00] mi 11.5 11.5; 1.81.8] mi [66; 00] mi [0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.415 V	Imm [test cases] imm [test cases] imm [test cases] imm [test cases] iF [TX RX] imm [TX RX] imm [TX RX]	COM Pass threshold ERL Pass threshold DER_0 T_r FORCE_TR TDR	Operational 3 10.5 1.00E-05 6.16E-03 1	dB dB ns	board_tl_tau board_Z_c z_bp(TX) z_bp(NEXT) z_bp(FEXT)	5.790E-03 [100 92.5] 1:400 0 0	Ohm mm mm mm
z_p (NEXT) [11 z_p (FEXT) [11 z_p (RX) [0 C_p [0 R_0 [0 R_d [0 A_re [1	[00;00] mi (1.5,11.5;1.81.8] mi [66;00] mi [0.87e-40.87e-4] ni 50 Oh [5050] Oh 0.415 V 0.415 V 0.6 V	m [test cases] m [test cases] m [test cases] F [TX RX] nm [TX RX] V	COM Pass threshold ERL Pass threshold DER_O T_r FORCE_TR TDR	3 10.5 1.00E-05 6.16E-03 1	dB ns	board_Z_c z_bp (TX) z_bp (NEXT) z_bp (FEXT)	[100 92.5] 1:400 0 0	Ohm mm mm mm
z_p (FEXT) [11 z_p (RX)	I.1.511.5; 1.81.8] mi [66; 00] mi [0.87e-40.87e-4] ni 50 Oh [5050] Oh 0.415 V 0.415 V 0.6 V	m [test cases] m [test cases] F [TX RX] nm [TX RX] V	ERL Pass threshold DER_0 T_r FORCE_TR TDR	10.5 1.00E-05 6.16E-03 1	dB ns	z_bp (TX) z_bp (NEXT) z_bp (FEXT)	1:400 0 0	mm mm mm
z_p (RX) C_p [0 R_0 R_d A_v A_fe A_ne	[6 6; 0 0] mm [0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	m [test cases] F [TX RX] nm [TX RX] V [V]	DER_0 T_r FORCE_TR TDR	1.00E-05 6.16E-03 1	ns	z_bp (NEXT) z_bp (FEXT)	0 0	mm mm
C_p [0 R_0 R_d A_v A_fe A_ne	[0.87e-4 0.87e-4] ni 50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	IF [TX RX] hm [TX RX] V [TX RX]	T_r FORCE_TR TDR	6.16E-03 1		z_bp (FEXT)	0	mm
R_0 R_d A_v A_fe A_ne	50 Oh [50 50] Oh 0.415 V 0.415 V 0.6 V	1m [TX RX] V V	FORCE_TR	1				-
R_d A_v A_fe A_ne	[50 50] Oh 0.415 V 0.415 V 0.6 V	nm [TX RX] V V	TDR		logical	z bp(RX)	1:30	mm
A_v A_fe A_ne	0.415 V 0.415 V 0.6 V	v v		and ERL options				
A_fe A_ne	0.415 V 0.6 V	V		and ERL options				
A_ne	0.6 V	-	TDR					
		v		0	logical			
	4		ERL	0	logical			
L	1 (C)		ERL_ONLY	0	logical			
M	32		TR_TDR	0.01	ns			
	filter and Eq		N	300				
f_r	0.75 *f	fb	TDR_Butterworth	1	logical			
c(0)	0.6	min	beta_x	1.70E+09				
c(-1)	[-0.3:0.02:0]	[min:step:max]	rho_x	0.3				
c(-2)	[0:.02:0.1]	[min:step:max]	fixture delay time	0				
c(1)	[-0.1:0.05:0]	[min:step:max]	Re	eceiver testing				
N_b	4/7/12 U	JI	RX_CALIBRATION	0	logical			
b_max(1)	0.5		Sigma BBN step	5.00E-03	V			
b_max(2N_b)	0.2							
g_DC	[-14:1:-3] di	IB [min:step:max]		Noise, jitter				
f_z	12.58 GH	Hz	sigma_RJ	0.01	UI			
f_p1	20 GF	Hz	A_DD	0.02	UI			
f_p2	28 GF	Hz	eta_0	8.20E-09	V^2/GHz			
g_DC_HP	[-3:1:0]	[min:step:max]	SNR_TX	33	dB			
f_HP_PZ	1.328125 GF	Hz	R_LM	0.95				
ffe_pre_tap_len	0 U	JI						
ffe_post_tap_len	0 U	JI	TDR_W_TXPKG	1				
Include PCB	1 logi	ical						
ffe_tap_step_size	0							
ffe_main_cursor_min	0.7							
ffe_pre_tap1_max	0.3							
ffe_post_tap1_max	0.3							
ffe_tapn_max	0.125							
ffe_backoff	0							

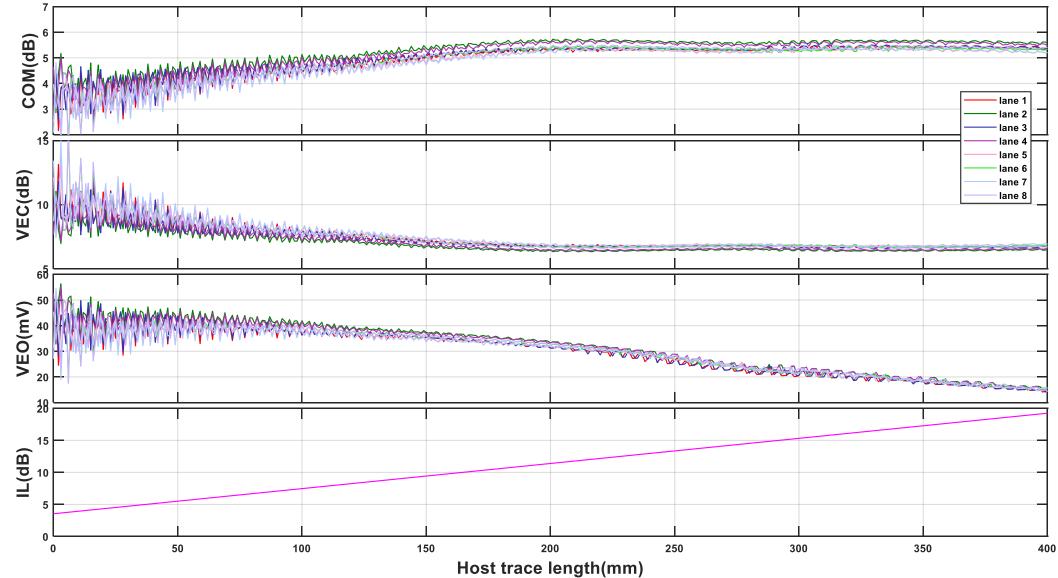
End to end COM spreadsheet w/ 5-tap and 10-tap FFE

Parameter	Table 93A-1 parameters				I/O control			Table 93A-3 parameters	
	Setting	Units	Information	DIAGNOSTICS	0	logical	Parameter	Setting	Units
f_b	53.125	GBd		DISPLAY_WINDOW	0	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f min	0.05	GHz		CSV_REPORT	1	logical	package_tl_tau	6.1400E-03	ns/mm
Delta f	0.01	GHz		RESULT_DIR	\results\100GEL_WG_{dat	te}\	package_Z_c	[87.5 92.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 1.0e-4]	nF	[TX RX]	SAVE_FIGURES	0	logical			
L_s	[0.12, 0.1]	nH	[TX RX]	Port Order	[1324]			Table 92–12 parameters	
С_Ь	[0.3e-4 0.3e-4]	nF	[TX RX]	RUNTAG	C2M_1218		Parameter	Setting	
z_p select	[1]		[test cases to run]	COM_CONTRIBUTION	0	logical	board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[11.5 11.5; 1.8 1.8]	mm	[test cases]		Operational		board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[00; 00]	mm	[test cases]	COM Pass threshold	3	dB	board_Z_c	[100 92.5]	Ohm
z_p (FEXT)	[11.5 11.5; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10.5	dB	z_bp (TX)	1:400	mm
z_p (RX)	[66;00]	mm	[test cases]	DER_0	1.00E-05		z_bp (NEXT)	0	mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	T_r	6.16E-03	ns	z_bp (FEXT)	0	mm
R_0	50	Ohm		FORCE_TR	1	logical	z_bp (RX)	1:30	mm
R_d	[50 50]	Ohm	[TX RX]						
A_v	0.415	V			and ERL options				
A_fe	0.415	V		TDR	0	logical			
A_ne	0.6	V		ERL	0	logical			
L	4			ERL_ONLY	0	logical			
M	32			TR_TDR	0.01	ns			
	filter and Eq			N	300				
f_r	0.75	*fb		TDR_Butterworth	1	logical			
c(0)	0.6		min	beta_x	1.70E+09				
c(-1)	[-0.3:0.02:0]		[min:step:max]	rho_x	0.3				
c(-2)	[0:.02:0.1]		[min:step:max]	fixture delay time	0				
c(1)	[-0.1:0.05:0]		[min:step:max]		eceiver testing				
N_b	0	UI		RX_CALIBRATION	0	logical			
b_max(1)	0			Sigma BBN step	5.00E-03	V			
b_max(2N_b)	0								
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter				
f_z	18.88	GHz		sigma_RJ	0.01	UI			
f_p1	28	GHz		A_DD	0.02	UI			
f_p2	53.125	GHz		eta_0	8.20E-09	V^2/GHz			
g_DC_HP	[-3:1:0]		[min:step:max]	SNR_TX	33	dB			
f_HP_PZ	0.00025	GHz		R_LM	0.95				
ffe_pre_tap_len	0	UI							
ffe_post_tap_len	4/9	UI		TDR_W_TXPKG	1				
Include PCB	1	logical							
ffe_tap_step_size	0								
ffe_main_cursor_min	0.7								
ffe_pre_tap1_max	0.3								
ffe_post_tap1_max	0.3								
ffe_tapn_max	0.125								
ffe_backoff	0								

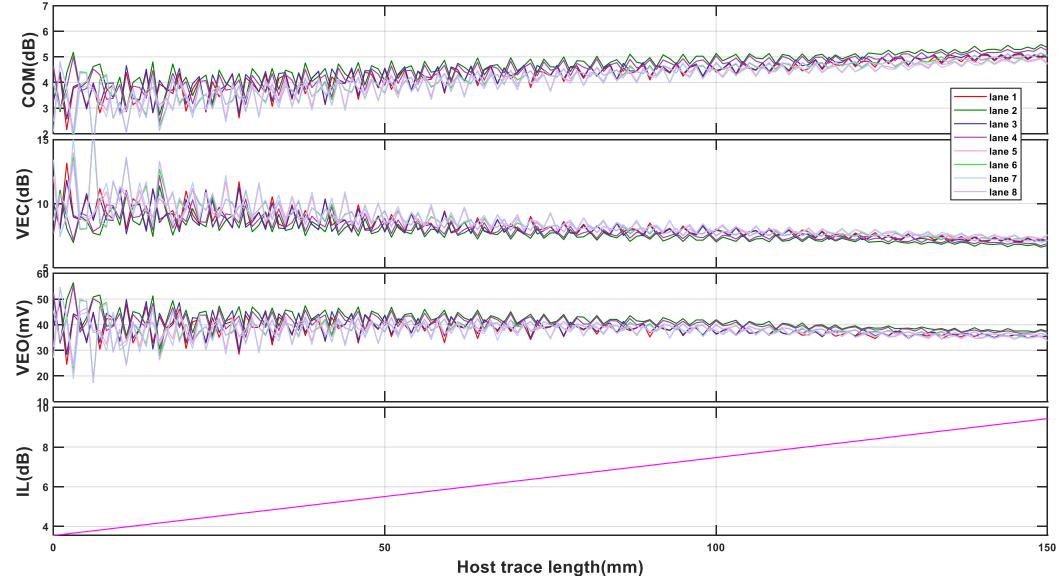
COM PCB and package loss information

- PCB loss at 26.56GHz: ~0.04dB/mm, ~1dB/in. (58mm is equivalent to the 2.3dB MCB loss being proposed in the cable small group).
- Package loss at 26.56GHz: 0.1dB/mm
- Insertion loss plotted in this presentation includes host, HCB and connector, but not package.

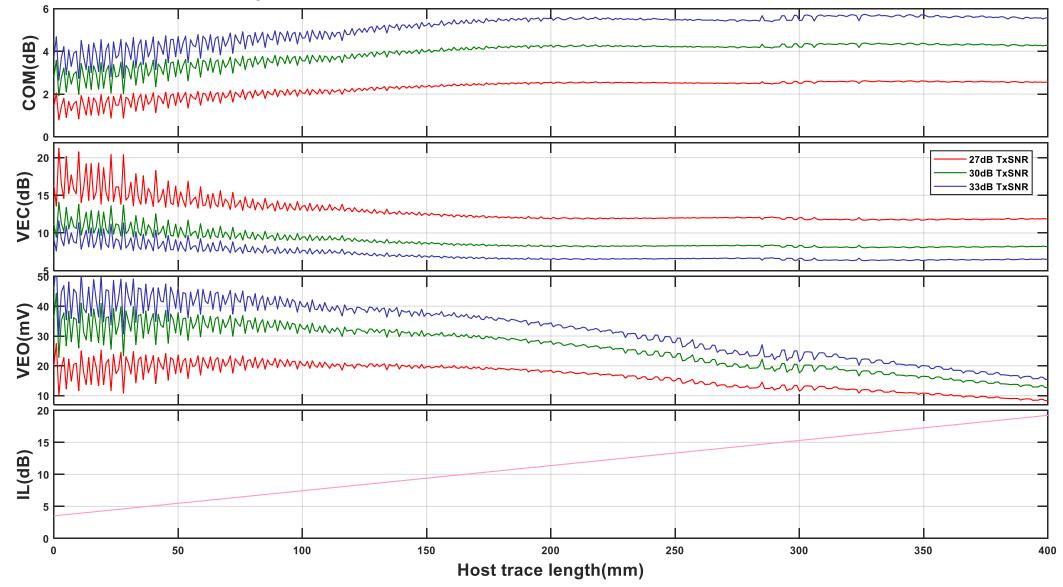
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



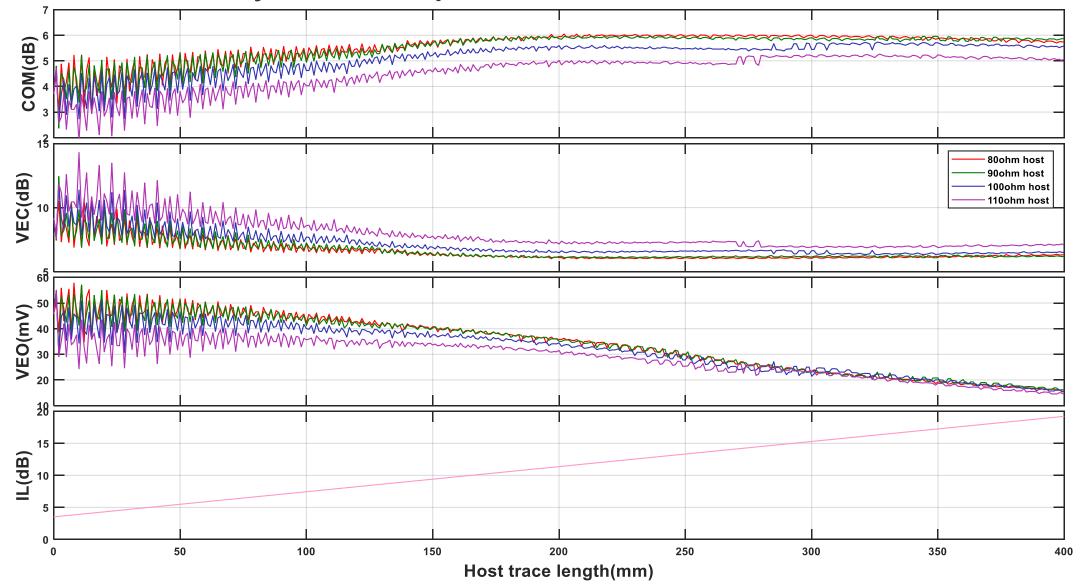
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



TP1a results by TxSNR

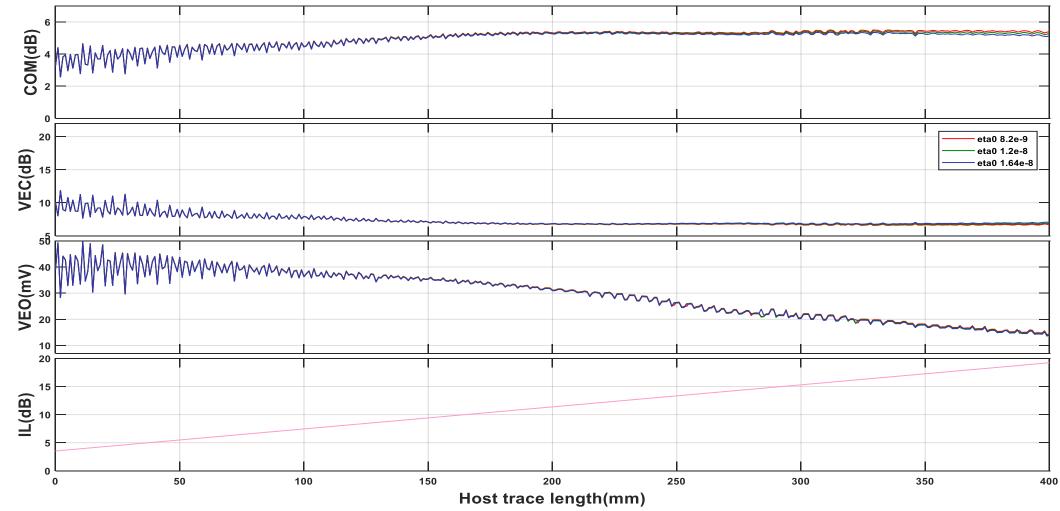


TP1a results by host impedance



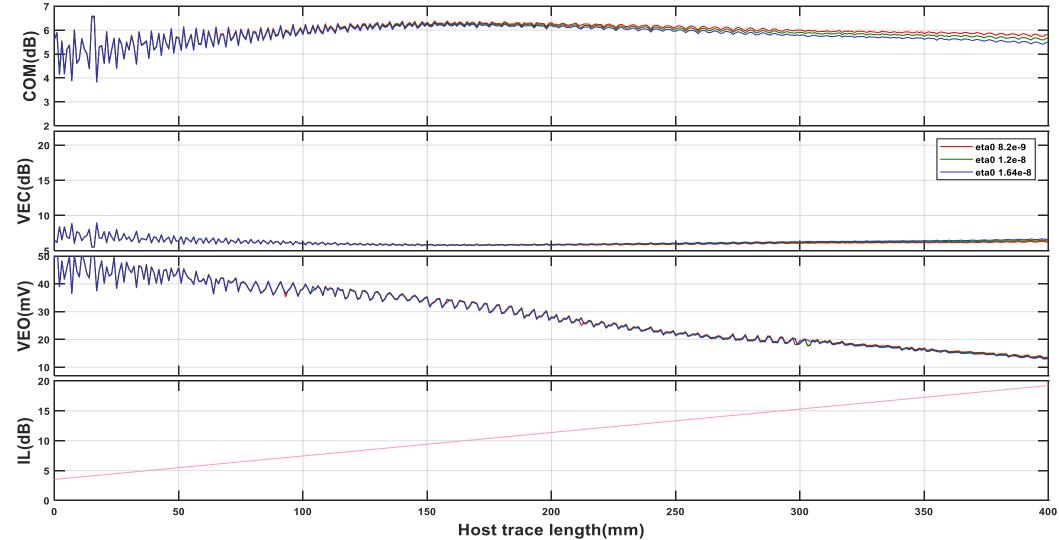
Effect of Eta0

Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



For the short package there is little effect in changing eta_0 in this range. However the required value for eta_0 to represent break-in needs to be evaluated.

Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host



For the longer package changing eta0 in the range evaluated is still not significant even for the higher loss hosts

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