

C2M ERL_{min} Proposal

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ToC

- ❑ Experiment with Rich Set of Cases
- ❑ Keys for Parameters, Scatter Plots, and Histograms
- ❑ Pass-fail Definitions
- ❑ Data Culling Process
- ❑ Recommendations

Experiment with Rich Set of Cases

Use posted channels to create a rich set of “pass/fail” cases using transmitter length swept between 11 mm and 32 mm in steps of 1 mm

There are 1408 cases considered here

Using COM configurations in sun_3ck_02_1119

“Pass” will be considered a COM > 3 dB using in the module die

Called this “COM full system”

COM run without crosstalk to sensitize experiment to reflections.

Measure at Tp1a

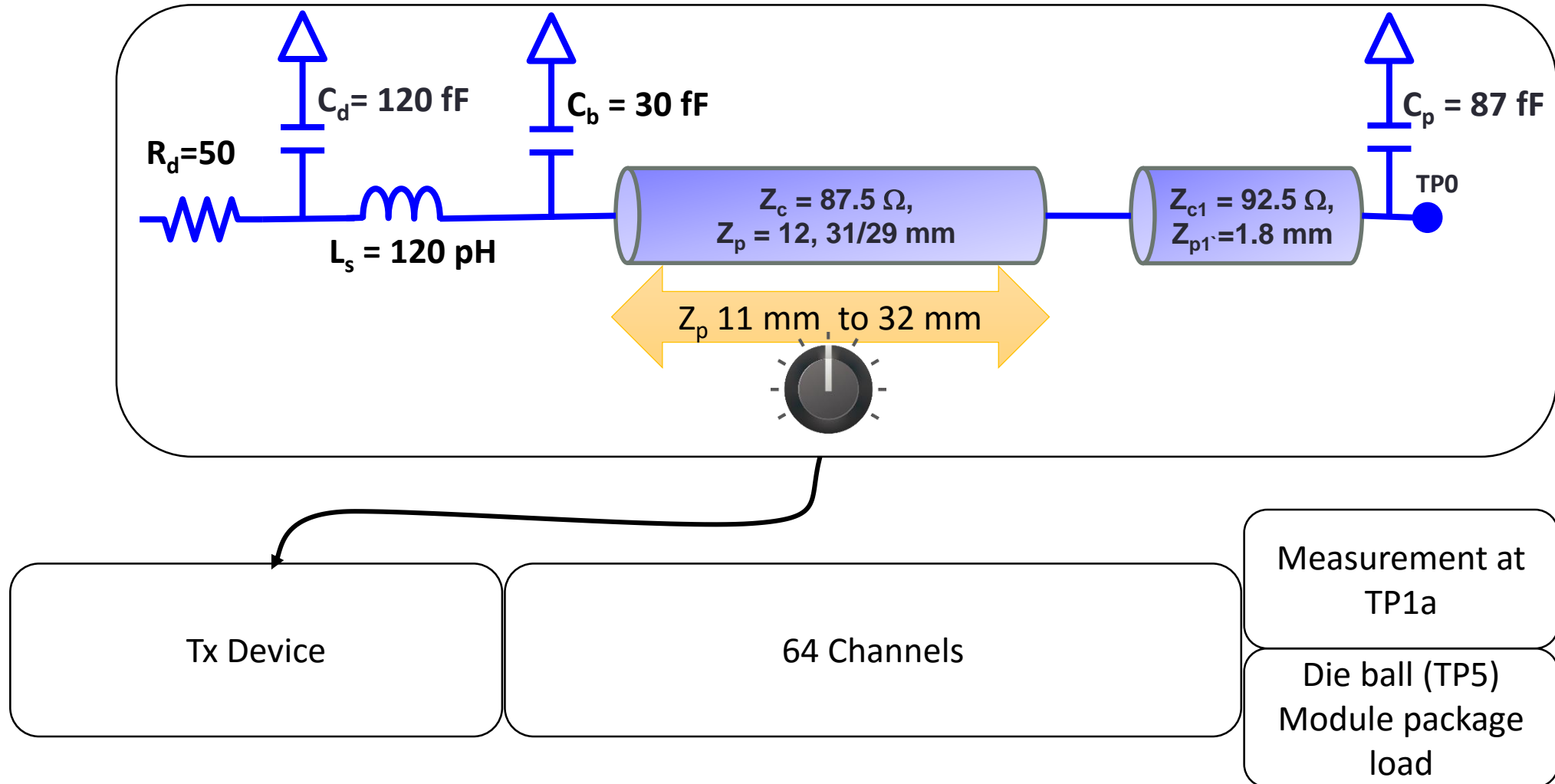
EVEC (sun_3ck_02_1119)

P_{\max}/v_f using $N_p=200$ (mellitz_3ck_01a_0919)

EH (mV)

ERL with ($N_{bx}=4$)

Sweep package length between 12 mm and 32 mm to produce ERL device variability

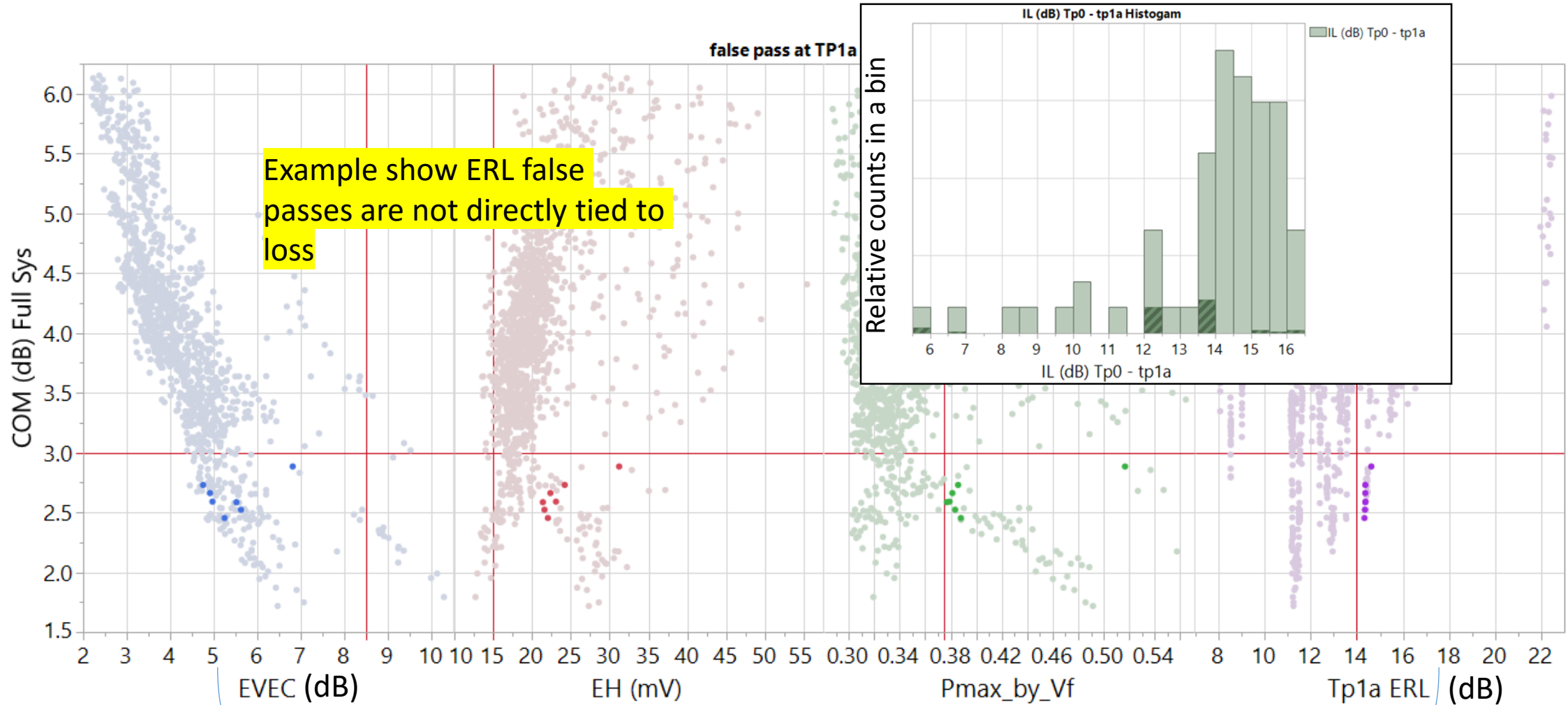


Parameter Key

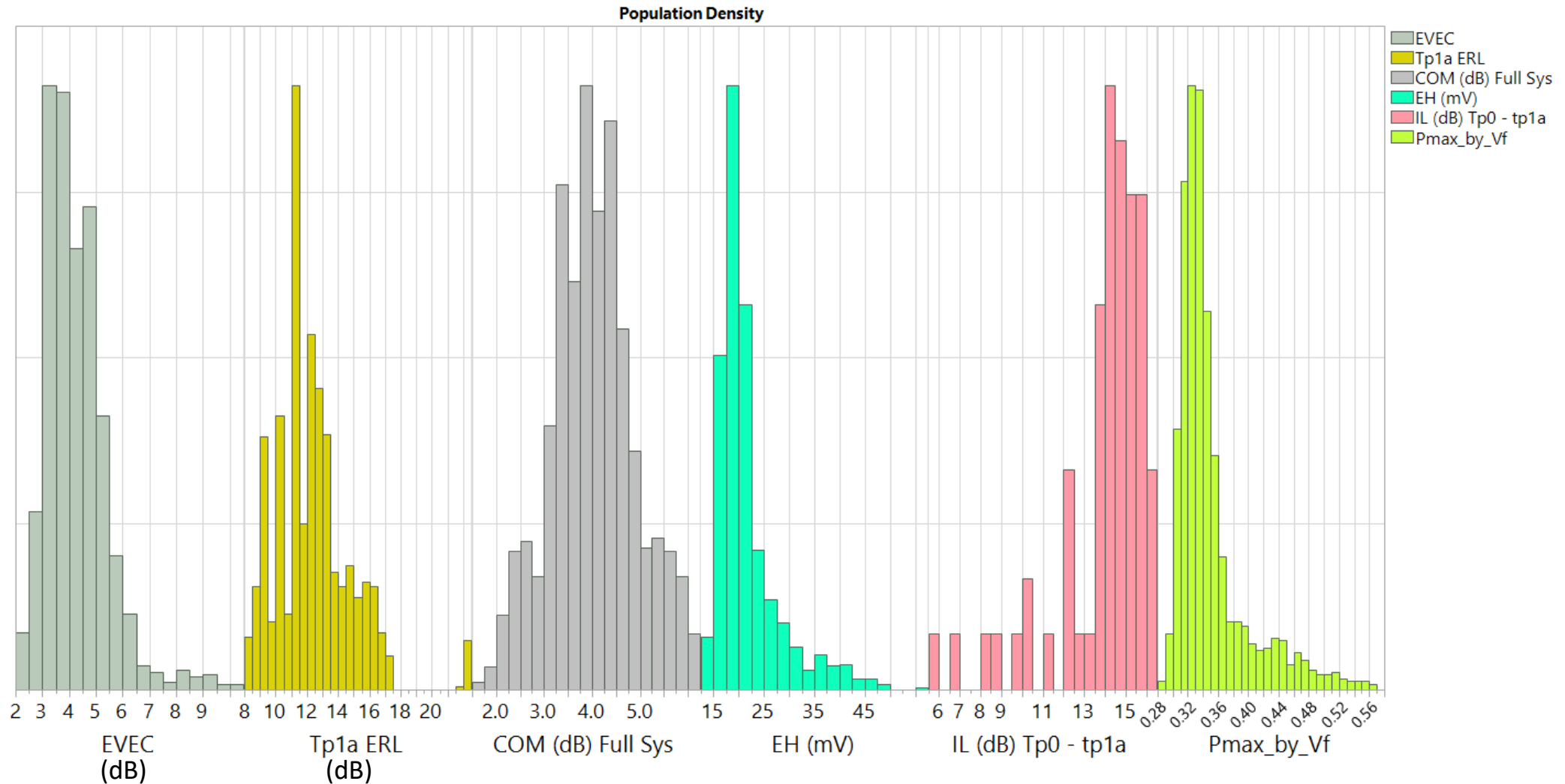
- *EVEC* (dB): from sun_3ck_02_1119
- *Pmax_by_Vf* (mv): from mellitz_3ck_01a_0919
 - $N_p=200$
- *Tp1a ERL* (dB): Annex 93A.5
 - T_{fx} adjusted per channel evaluated
- *COM* (dB): Annex 93A.1
- *EH* (mV): VEO from healey_3bs_01a_0317

Key for scatter plots and histograms

Darker colors are associated selected data



Just Information: Population density of parameters for 1408 channels simulations suggest a reasonable population



Pass-fail definitions for ERL specification

❑ False ERL pass (due to ERL only)

- COM full system fail
- EVEC pass
- EH pass
- ERL pass
 - Explore P_{\max}/v_f dependence
 - Called Pmax_by Vf in the slides

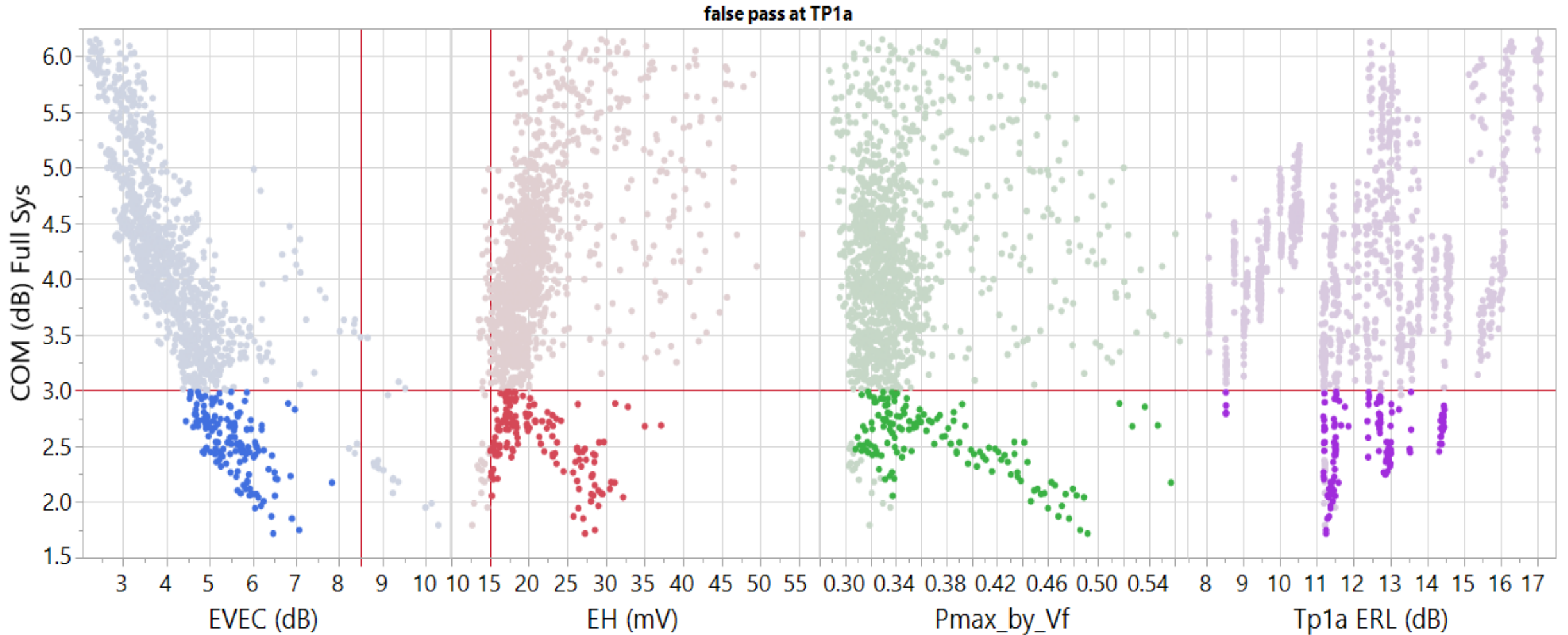
❑ False ERL fail (due to ERL only)

- COM full system pass
- EVEC pass
- EH pass
- ERL fail
 - Explore P_{\max}/v_f dependence
 - Called Pmax_by Vf in the slides

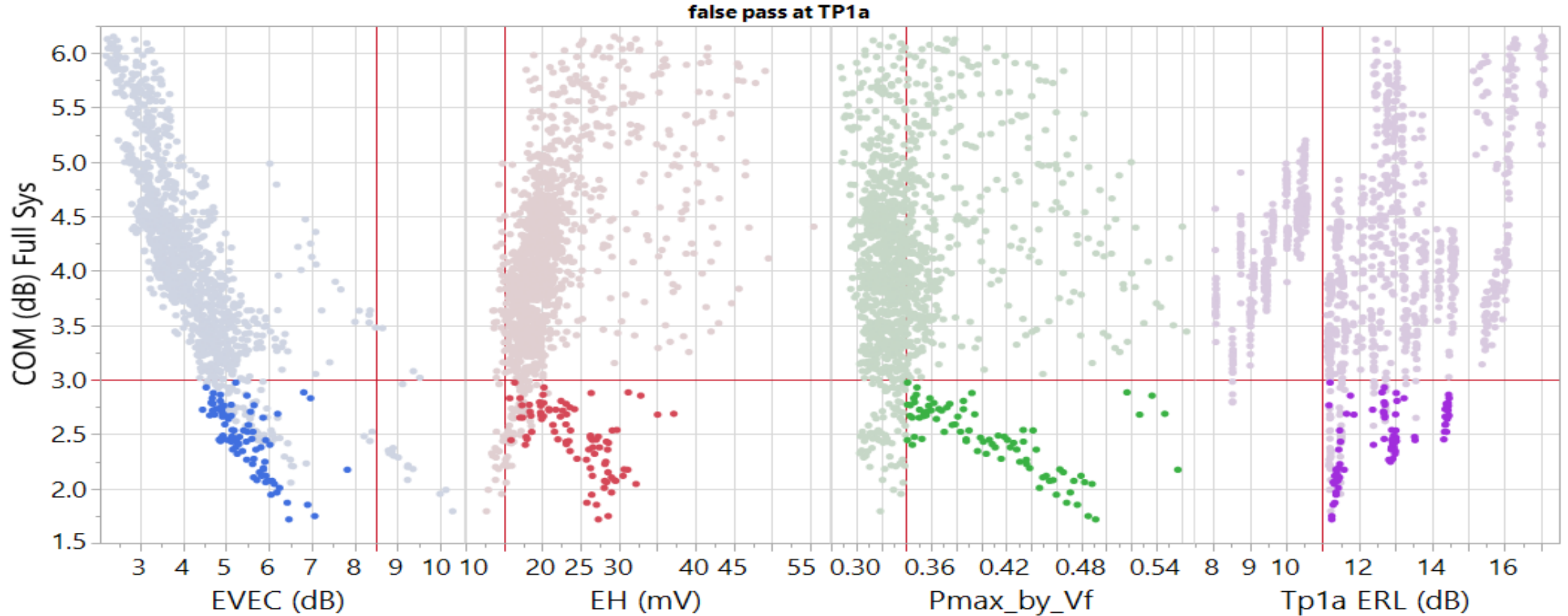
Example: Data Culling Process Follows

- ❑ The data culling process is extensive
- ❑ Only one path is shown as an example

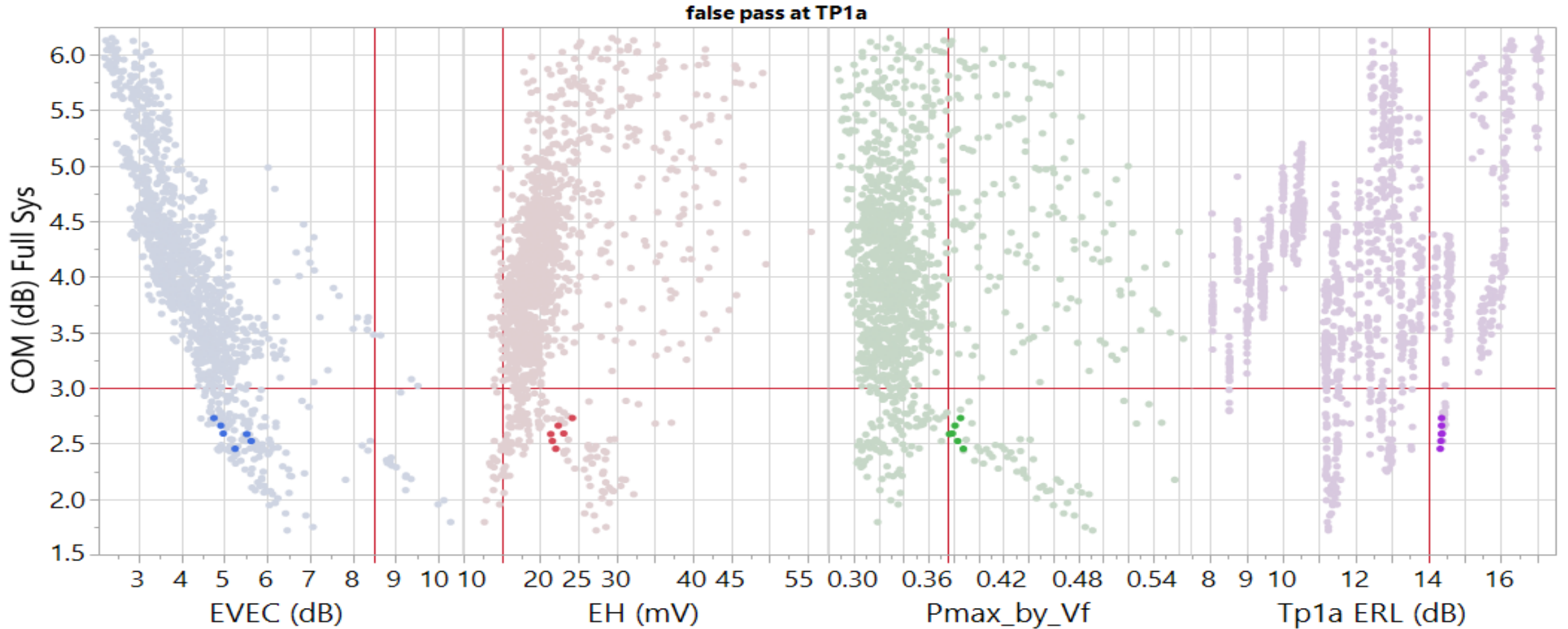
Example: False Pass using VEC and EH criteria (red lines)



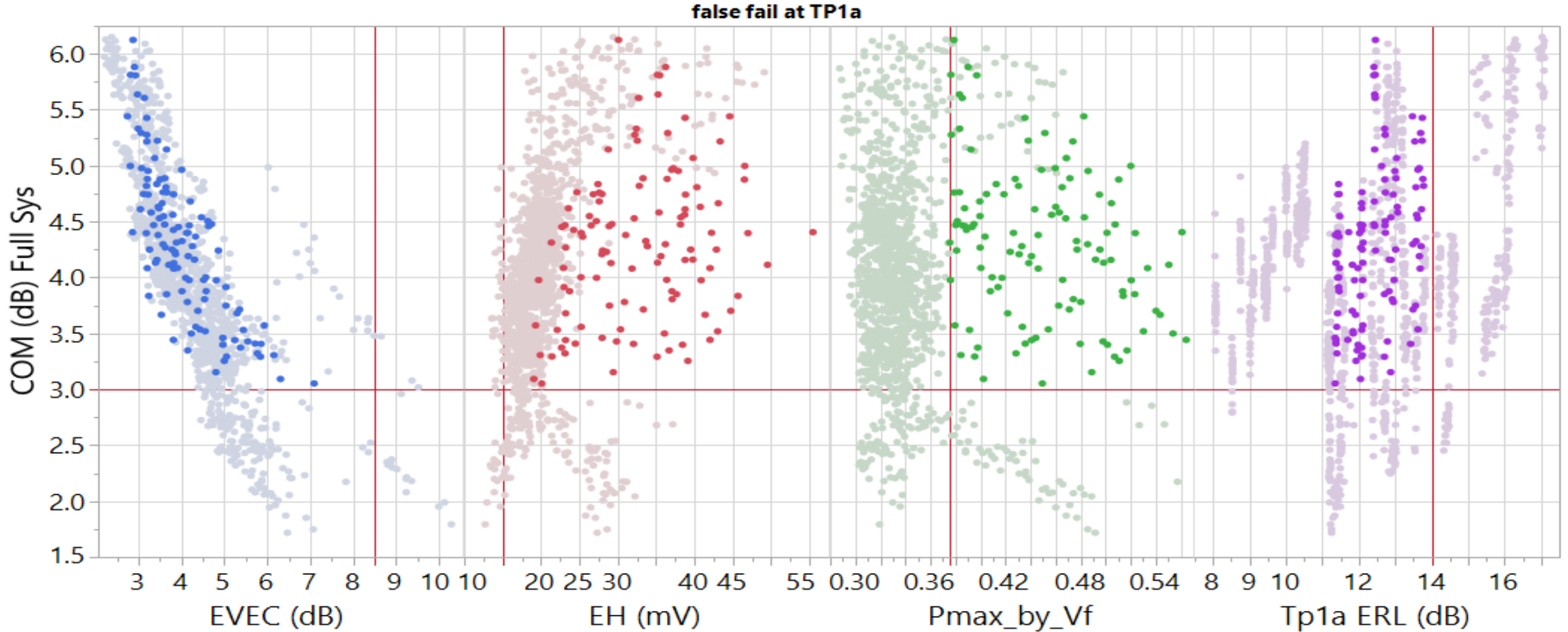
Example: False Pass using VEC and EH but adding Pmax_by Vf min (0.34) and ERL (11 dB)



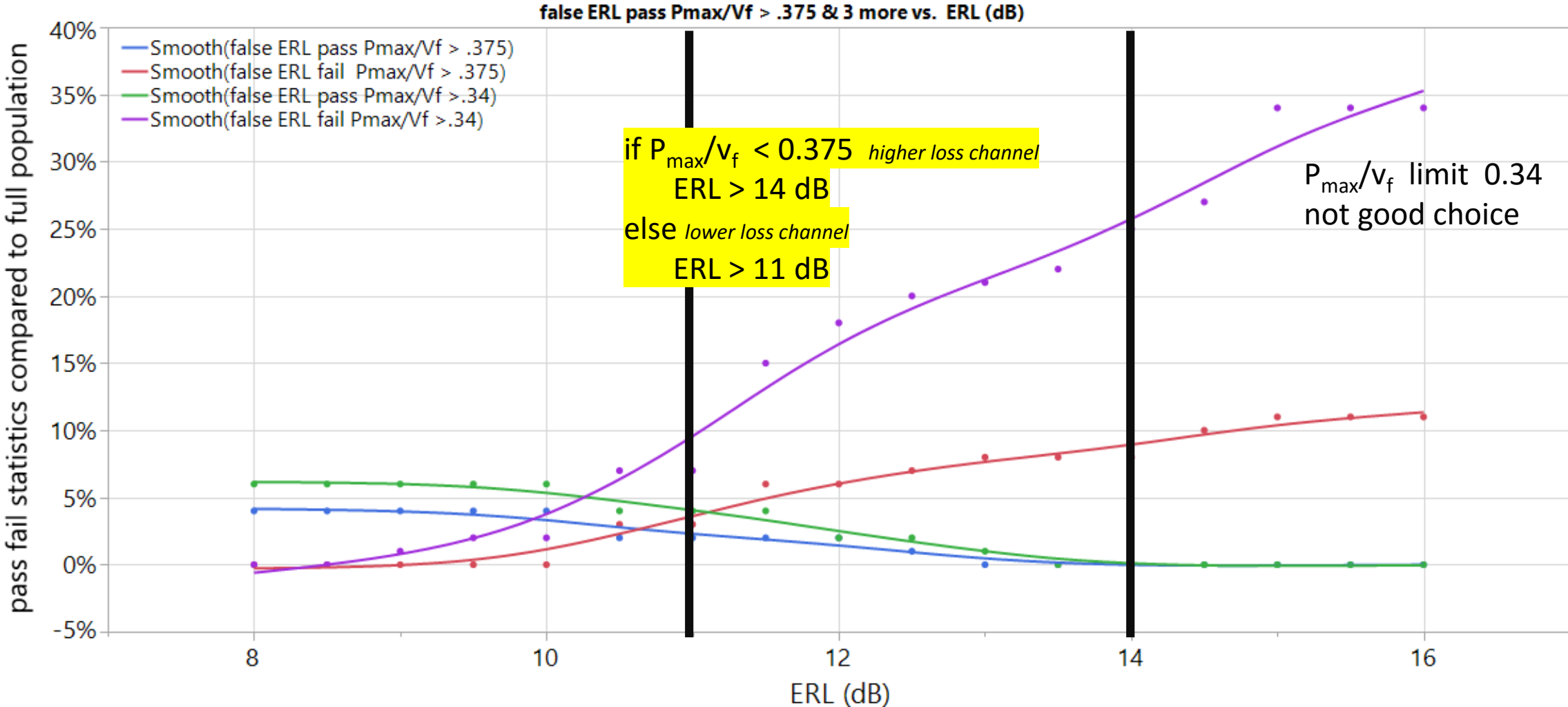
False Pass with VEC and EH Pmax_by Vf min (0.375 v) and ERL_{min} (14 dB)



Example: False fail (pass COM, EH, EVEC) fail ERL and Pmax/Vf min 0.375



PASS Fail Charts for ERL



ERL and Parameter recommendations for C2M

Host

- ❑ $\rho_x = 0.30$
- ❑ $\beta_x = 2.34$ GHz
- ❑ $T_r = 10$ ps
- ❑ $N = 1000$
- ❑ $N_{bx} = 4$
- ❑ $ERL_{min} = 11$ dB for host input
- ❑ ERL_{min} host output
 - $ERL_{min} = 14$ dB if $P_{max}/v_f < 0.375$
 - higher loss channel
 - $ERL_{min} = 11$ dB if $P_{max}/v_f > 0.375$
 - low loss channel

Module

- ❑ $\rho_x = 0.30$
- ❑ $\beta_x = 2.34$ GHz
- ❑ $T_r = 10$ ps
- ❑ $N = 200$
- ❑ $N_{bx} = 4$
- ❑ $ERL_{min} = 11$ dB
- ❑ $V_f min = 0.68$

Thank You!

Backup data COM parameters

TP1a COM Spread Sheet from sun_3ck_02_1119

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information				Parameter	Setting	Units
f_b	53.125	Gbd		DIAGNOSTICS	1	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz		DISPLAY_WINDOW	1	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz		CSV_REPORT	1	logical	package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4, 0]	nF	[TX RX]	RESULT_DIR	.\TestCaseFloatingBank\				
L_s	[0.12, 0]	nH	[TX RX]	SAVE_FIGURES	0	logical			
C_b	[0.3e-4 0]	nF	[TX RX]	Port Order	[1 3 2 4]				
z_p select	[1]		[test cases to run]	RUNTAG	C2M TP1a				
z_p (TX)	[13 30; 1.8 1.8]	mm	[test cases]	COM_CONTRIBUTION	0	logical	Table 92-12 parameters		
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]	Operational			Parameter	Setting	
z_p (FEXT)	[13 30; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB	board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (RX)	[0 0; 0 0]	mm	[test cases]	ERL Pass threshold	10.5	dB	board_tl_tau	5.790E-03	ns/mm
C_p	[0.87e-4 0]	nF	[TX RX]	DER_0	1.00E-05		board_Z_c	90	Ohm
R_0	50	Ohm		T_r	6.16E-03	ns	z_bp (TX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]	FORCE_TR	1	logical	z_bp (NEXT)	119	mm
A_v	0.391	V	vp/vf=.694	Include PCB	0	logical	z_bp (FEXT)	119	mm
A_fe	0.391	V	vp/vf=.694	TDR and ERL options			z_bp (RX)	119	mm
A_ne	0.489	V		TDR	1	logical			
L	4			ERL	1	logical			
M	32			ERL_ONLY	0	logical			
filter and Eq				TR_TDR	0.01	ns			
f_r	0.75	*fb		N	400				
c(0)	0.6		min	TDR_Butterworth	1	logical			
c(-1)	[-0.3:0.02:0]		[min:step:max]	beta_x	0.00E+00				
c(-2)	[0:.02:0.1]		[min:step:max]	rho_x	0.32				
c(-3)	[-0.04:.02:0.0]		[min:step:max]	fixture delay time	0	enter sec			
c(1)	[-0.1:0.05:0]		[min:step:max]	TDR_W_TXPKG	1				
N_b	4	UI		N_bx	4	UI			
b_max(1)	0.5			Receiver testing					
b_max(2..N_b)	0.2			RX_CALIBRATION	0	logical			
g_DC	[-14:1:-3]	dB	[min:step:max]	Sigma BBN step	5.00E-03	V			
f_z	12.58	GHz		Noise, jitter					
f_p1	20	GHz		sigma_RJ	0.01	UI			
f_p2	28	GHz		A_DD	0.02	UI			
g_DC_HP	[-3:1:0]		[min:step:max]	eta_0	8.20E-09	V^2/GHz			
f_HP_PZ	1.328125	GHz		SNR_TX	33	dB			
ffe_pre_tap_len	0	UI		R_LM	0.95				
ffe_post_tap_len	0	UI							
ffe_tap_step_size	0								
ffe_main_cursor_min	0.7								
ffe_pre_tap1_max	0.3								
ffe_post_tap1_max	0.3								
ffe_tapn_max	0.125								
ffe_backoff	0								
Floating Tap Control									
N_bg	0		0 1 2 or 3 groups						
N_bf	0		taps per group						
N_f	40		UI span for floating taps						
bmaxg	0.05		max DFE value for floating taps						

Whole-link COM Spread Sheet from sun_3ck_02_1119

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information	DIAGNOSTICS	0	logical	Parameter	Setting	Units
f_b	53.125	GBd		DISPLAY_WINDOW	0	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz		CSV_REPORT	1	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz		RESULT_DIR	.\TestCaseFloatingBank\		package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 , 0.85e-4]	nF	[TX RX]	SAVE_FIGURES	0	logical	Table 92-12 parameters		
L_s	[0.12, 0.12]	nH	[TX RX]	Port Order	[1 3 2 4]		Parameter	Setting	
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	RUNTAG	C2M end-to-end		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p select	[1]		[test cases to run]	COM_CONTRIBUTION	0	logical	board_tl_tau	5.790E-03	ns/mm
z_p (TX)	[13 30; 1.8 1.8]	mm	[test cases]	Operational			board_Z_c	90	Ohm
z_p (NEXT)	[6 2; 0 0]	mm	[test cases]	COM Pass threshold	3	dB	z_bp (TX)	119	mm
z_p (FEXT)	[13 30; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10.5	dB	z_bp (NEXT)	119	mm
z_p (RX)	[6 2; 0 0]	mm	[test cases]	DER_0	1.00E-05		z_bp (FEXT)	119	mm
C_p	[0.87e-4 0.75e-4]	nF	[TX RX]	T_r	6.16E-03	ns	z_bp (RX)	119	mm
R_0	50	Ohm		FORCE_TR	1	logical			
R_d	[45, 50]	Ohm	[TX RX]	Include PCB	0	logical			
A_v	0.391	V	vp/vf= .694	TDR and ERL options					
A_fe	0.391	V	vp/vf= .694	TDR	1	logical			
A_ne	0.489	V		ERL	1	logical			
L	4			ERL_ONLY	0	logical			
M	32			TR_TDR	0.01	ns			
filter and Eq				N	400				
f_r	0.75	*fb		TDR_Butterworth	1	logical			
c(0)	0.6		min	beta_x	0.00E+00				
c(-1)	[-0.3:0.02:0]		[min:step:max]	rho_x	0.32				
c(-2)	[0:.02:0.1]		[min:step:max]	fixture delay time	0	enter sec			
c(-3)	[-0.04:.02:0.0]		[min:step:max]	TDR_W_TXPKG	1				
c(1)	[-0.1:0.05:0]		[min:step:max]	N_bx	4	UI			
N_b	4	UI		Receiver testing					
b_max(1)	0.5			RX_CALIBRATION	0	logical			
b_max(2..N_b)	0.2			Sigma BBN step	5.00E-03	V			
g_DC	[-14:1:-3]	dB	[min:step:max]	Noise, jitter					
f_z	12.58	GHz		sigma_RJ	0.01	UI			
f_p1	20	GHz		A_DD	0.02	UI			
f_p2	28	GHz		eta_0	8.20E-09	V^2/GHz			
g_DC_HP	[-3:1:0]		[min:step:max]	SNR_TX	33	dB			
f_HP_PZ	1.328125	GHz		R_LM	0.95				
ffe_pre_tap_len	0	UI							
ffe_post_tap_len	0	UI							
ffe_tap_step_size	0								
ffe_main_cursor_min	0.7								
ffe_pre_tap1_max	0.3								
ffe_post_tap1_max	0.3								
ffe_tapn_max	0.125								
ffe_backoff	0								
Floating Tap Control									
N_bg	0		0 1 2 or 3 groups						
N_bf	4		taps per group						
N_f	40		UI span for floating taps						
bmaxg	0.05		max DFE value for floating taps						