Study of KR ERL Test Spec

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Outline

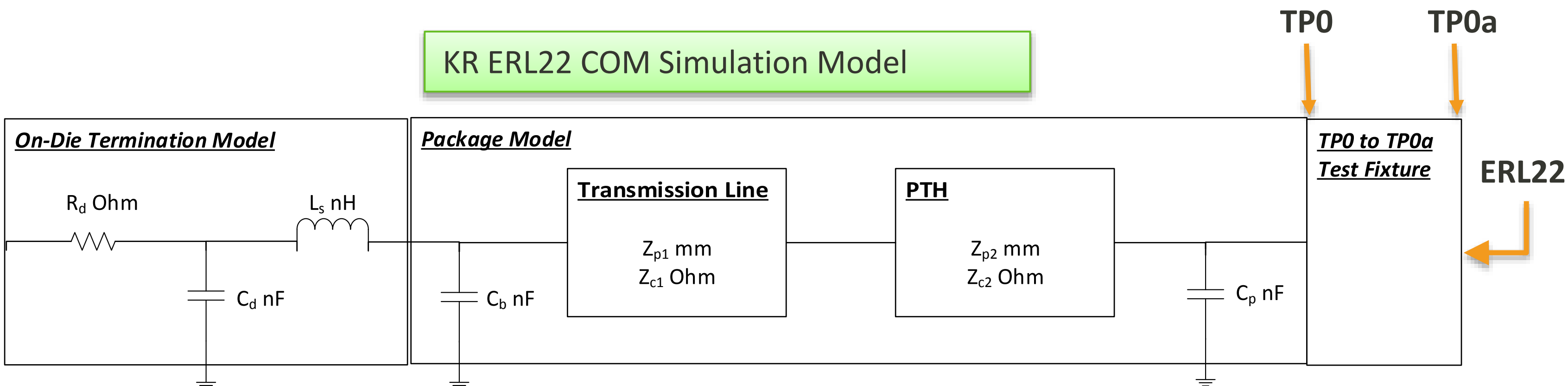
- Backgrounds and motivations
- Channel and COM settings
- COM and ERL vs Package Trace Length
- Summary

Backgrounds and Motivations

- Effective Return Loss (ERL) had been adopted in IEEE 802.3cd for 50G-KR of TX and RX test specs
  - To replace frequency-domain RL mask by considering the capability of reference RX
  - $\mathbf{ERL_{min}}$ = 15 dB
  - T_{fx} is twice the delay from TP0 to TP0a
  - $N_{bx} = N_b$
- Observations
  - Check COM and ERL sensitivities to TX package length
  - **Issue**: ERL is very sensitive across N_{bx} boundary
- Suggestion
  - Study more of ERL before deciding $\mathbf{ERL_{min}}$ specs

Channel and COM Settings

- We explored KR ERL spec by
  - COM ERL22 calculation by measured TP0 to TP0a test fixture
  - Sweep N_{bx} = [12 24 40]
  - Sweeping R_d, Z_{p1}, Z_{c1}, Z_{c2}
- COM parameter settings [details in appendix]
  - COM 2.75 with parameters in D0p4



- DUT: COM KR on-die & Package (PKG) models
- Measured TP0a test fixture
  - 1.8 dB IL at Nyquist
  - T_{fx} = 1.56 ns

KR ERL_{min} Options – PKG >= 35 mm

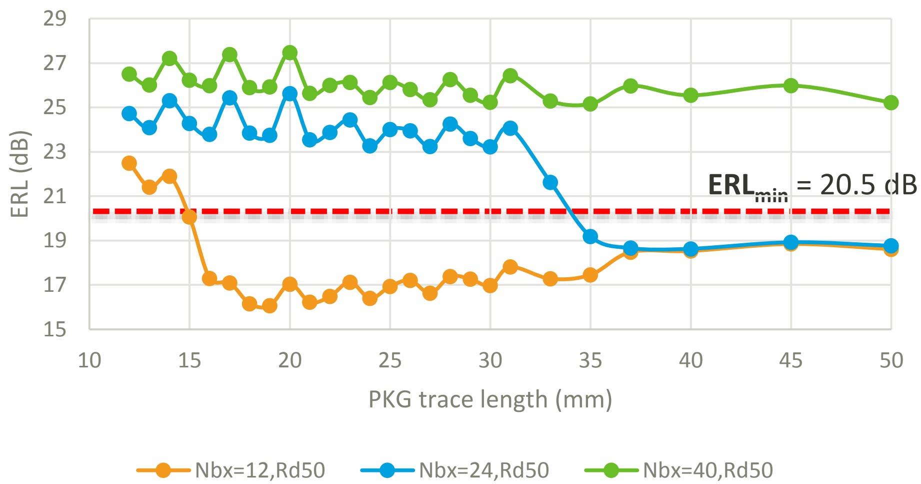
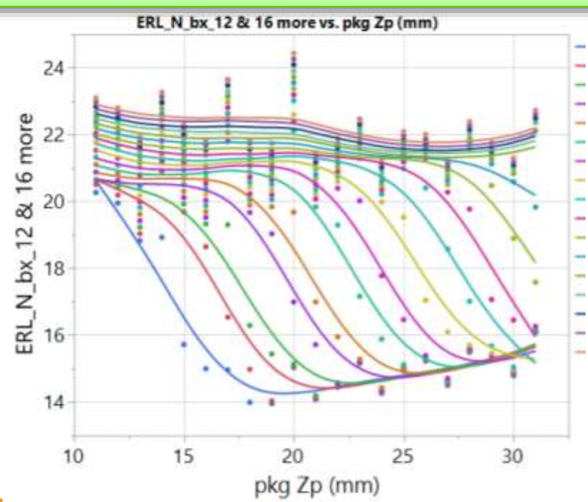


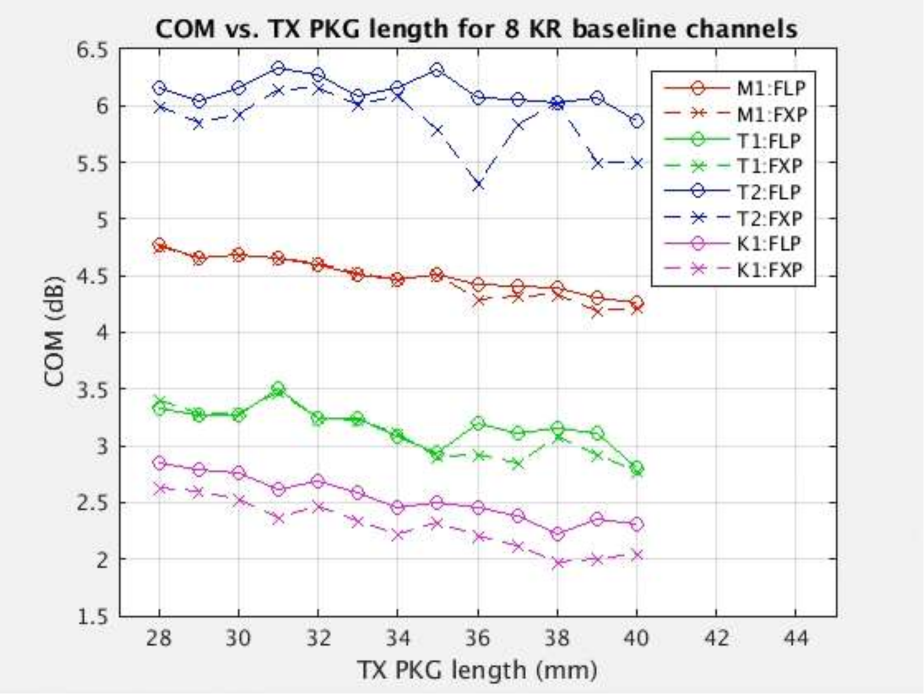
Figure of mellitz_3ck_adhoc_02_100219



- ❑ In mellitz_3ck_adhoc_02_100219, Rich proposed Z_{p1} sweep analysis with 108 KR channels to proposed the following spec
  - ○ N_{bx} = 24, **ERL_{min}** = 20.5 dB
- ❑ Similar "**Hockey stick**" found as Rich's contribution
  - ○ N_{bx} = 24 covers up to Z_{p1} <= 31mm
  - ○ However, **ERL_{min}** = 20.5 dB spec fails COM on-die + PKG model with Z_{p1} >= 35 mm → *Is that true?*
- ❑ Explore Device A vs. Device B
  - ○ **Device A**(Z_{p1}=31mm): ERL = **24.1 dB**
  - ○ **Device B**(Z_{p1}=35mm): ERL = **19.2 dB**
  - ○ "Floating-tap" span up to 40 UI can cover "reflection" due to Z_{p1}=35mm

COM of KR Baseline Channels 28 to 40 mm TX PKG length

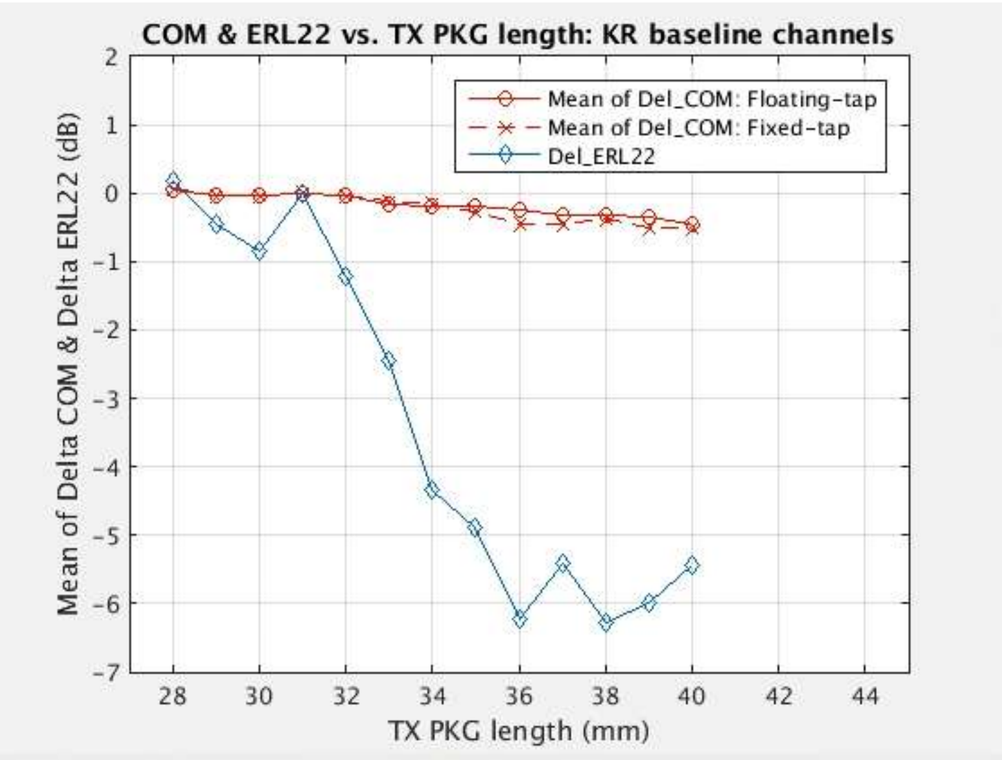
- 8 KR baseline channels, heck_3ck_01b_0719
- KR baseline floating-tap DFE vs. 24-tap DFE
  - FLP = KR baseline floating-tap DFE
  - FXP = 24-tap DFE



- ❑ COM decreases when PKG length increases
  - ○ Longer length has larger IL
- ❑ Observe Del_COM
  - ○ Device A (31mm) as baseline
  - ○ Del_COM(Zp1) = COM(Zp1) – COM(31mm)
- ❑ Observe Del_ERL
  - ○ Del_ERL(Zp1) = ERL(Zp1) – ERL(31mm)
- ❑ Check sensitivity to TX PKG length

ERL Sensitivity vs. COM Sensitivity

- Checking sensitivity by mean of Del_COM & Del_ERL



- ERL is too sensitive during Zp1 = 32 ~ 36 mm
  - 6 dB drop
  - COM is much less sensitive < 0.5 dB drop
  - Reflection of 32 mm is at boundary of N_{bx} = 24
- <u>**Issue**</u>: ERL is very sensitive across N_{bx} boundary
  - Root causes?

Summary

- ERL is very sensitive around N_{bx} = 24 boundary

- Suggestions
  - Study more of ERL before deciding $\mathbf{ERL_{min}}$ specs

- Next steps
  - Check root causes
  - Check ERL reflects floating-tap capability

everyday genius

COM Settings – ERL Calculation

able 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02:0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[2 1 4 3]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	2000	
beta_x	2.34E+09	
rho_x	**0.3**	
fixture delay time	1.56E-09	s
TDR_W_TXPKG	1	
N_bx	12	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A? parameterss		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92?2 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**3**	**0 1 2 or 3 groups**
N_bf	*3*	taps per group
N_f	40	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps

yellow indicates WIP

COM of KR Baseline Channels 28 to 40 mm TX PKG length